ISDN & DATACOM PRODUCTS

DATABOOK

1st EDITION

AUGUST 1992

USE IN LIFE SUPPORT DEVICES OR SYSTEMS MUST BE EXPRESSLY AUTHORIZED

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1. Life support devices or systems are those which (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided with the product, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can reasonably be expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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ISDN: THE SGS-THOMSON SOLUTION

In the world there are about 800,000,000 kilometers of copper wire connections between telephone subscribers and the local exchange office. This is the largest asset of telephone network operators. By using Integrated Services Digital Network (ISDN) techniques this costly asset can continue to serve as the final subscriber link in a completely digital worldwide network that brings users new services.

What makes the ISDN revolution possible is the availability of affordable integrated circuits that perform highly complex functions, allowing the transmission of two 64kbits/s voice/data channels over a standard telephone wire.

A leading supplier of telecom ICs, SGS-THOMSON has been active in the research and study of ISDN circuits for many years, and has invested five years of effort in the development of a family of ICs covering all of the key functions and all of the major markets.

These circuits include "U" interface devices for both 2B1Q and 4B3T line codes, an "S" interface, a HDCL & GCI controller, and ISDN power supply and a programmable ISDN audio front end. These ICs are designed to operate with both the GCI and Microwire chip interconnect bus standards.

Because of the high complexity of ISDN circuits the technology used to fabricate them becomes critical. Armed with advanced R&D and production facilities, SGS-THOMSON is at the forefront of CMOS technology development, guaranteeing continual improvements in litthography. Today the circuits described in this book are fabricated with 1.2u CMOS technologies -- some with a pure digital version, others with a mixed analog/digital variant. Future generations will use finer lithography to permit a further increase in the integration level as functions are brought together on single dice.

This volume contains a tutorial introduction and datasheets for all of the SGS-THOMSON dedicated ISDN integrated circuits.

DATACOM: MAKING THE DESIGNERS' JOB EASIER

This book includes key devices for datacom Link Layer Controller applications, a family of reliable high performance devices manufactured using SGS-THOMSON's advanced CMOS technology.

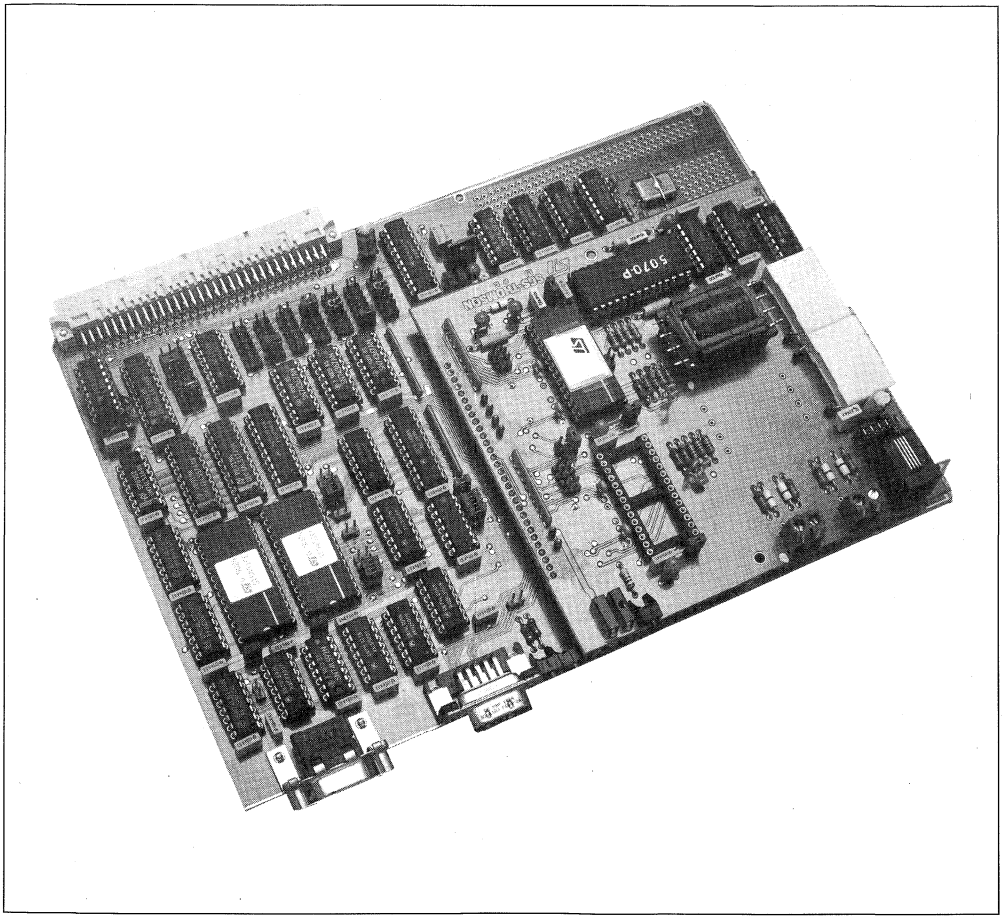
The DATACOM products form a co-ordinated family of Link Layer Controllers for different applications that all share the same pin out and bus interface. This approach saves man-years of development effort when needing to design new equipment that requires different OSI link layer protocols in the HDLC family.

The 7MHz full duplex MK502X5 series of products described in this databook are used in volume applications in ROUTERS, CENTRAL OFFICE Wide Area Networks, and CELLULAR RADIO applications. Device certification in major networks, world-wide, reduces the time the design engineer must spend in software development. In fact, the

entire layer two of the OSI model is included on-chip for LAPB and X.75, CCS#7, and SDLC (Secondary), in the MK5025, MK5027, and MK5029 respectively.

The next step of evolution for the plug-compatible MK5025 family is MK50H25. The MK50H25 series Link Layer Controller supports SYSCLK of 33MHz and can "burst" data up to 50 MHz for T3 and FRAME RELAY applications. This series will expand the product portfolio for high performance devices designed to make the engineers' job easier.

Contact your SGS-Thomson sales representative for further information on any of the devices mentioned in this book.



Application support for SGS-THOMSON's ISDN integrated circuit product range includes demonstration and evaluation boards like this one, which allows rapid testing of U interface devices.

ISDN TUTORIAL

WHAT IS ISDN?

ISDN means Integrated Services Digital Network.

This is an all digital communication network offering the capability of communicate through voice, data or video using a bandwidth that is increased from the 3 khz of the analog telephone to the 144 Kbps offered by 2x64 Kbps voice/data B channels

CCITT defines the ISDN as:

A network evolved from the telephony integrated digital network that provides end-to-end digital connectivity to support a wide variety of services, to which users have access by a limited set of standard multipurpose customer interfaces.

Text Box 1

plus a 16 Kbps signalling D channel.

This definition deserves some words for explaining carefully the meaning of this new communication concept.

The ISDN basic idea is simply to move the point of analog to digital conversion from the central office to the subscriber and make the signal transmitted over the standard copper cable a digital one.

As the digitization of the Telephone Network is expanding from the Core of the Central Office (Line Card, Switching and Digital Trunk) to the subscriber premises, so leaving a close and limited distance environment to get at the customer premises, the need for compatibility with the existent copper wiring becomes the center of the problem.

In the history of telecommunication the backwords compatibility is fundamental for any new transmission technique having the target to replace completely the preceding one.

A simple calculation can help in understanding the importance and the reason of this philosophy: we can reasonably consider that around 800 million subscriber copper wire access exists in the world; it is reported from various sources that the average distance between the nearest central office and the user telephone is around 1 km; conclusively we can say that around 800 million kilometers of twisted copper cable exist in the world: the biggest assets owned by the telecom service suppliers.

That highlights the basic challenge of ISDN: the possibility to bring a much wider bandwidth to the user without changing the existent cabling set up.

What are the advantages that an integrated services digital network will offer? The actual payoff is for both the service suppliers and the users.

The user will increase use of data communication: this means to be able to take either a telephone, personal computer or any other form of data communications equipment and plug directly into a standard phone jack gaining access to a number of high speed data links and a big variety of services.

For the PTTs ISDN represents a new, revenue generating, concept which takes advantage of their large capital investment in the telecom network providing an increased bandwidth to the subscriber, creating an outstanding growth of the added value of the existent installed cable base; the phone companies will be able to provide new services which customers will pay for!

Although it is difficult to evaluate quantitatively, an increase in productivity is foreseen by ISDN's subscribers.

ISDN services

- Conversational:
  - ISDN data transmission
  - Telephony (Conference)
  - Teletex
  - Telefax (Group 4)
  - Textfax (Mixed mode)
  - Telewriting
  - Image transfer
  - Videophone
  - Alarm services
  - Teleaction
- Messaging:
  - Voice mail
  - Text mail
  - Fax mail
- Retrieval:
  - Videotex
- Distribution:
  - Data
  - Voice
  - Image

Text Box 2

ISDN TERMINOLOGY/DEFINITIONS

In order to convert a subscribers connection from an analog to a digital one, each end of the copper loop must be changed.

Upon this conversion, one of two link types are defined, Basic or Primary access.

Under the Basic Access rate, each subscriber will be linked to the central office by 2B channels and 1D channel, (2B+1D). For Basic Access each B Channel represents a 64 kbps stream and the D Channel represents a 16 kbps flow. A minimum rate of 144 kbps full duplex transmission is therefore available.

Typically, a basic access subscriber will be an individual private user where, for example, he can connect at the same time 2 phones, or 1 phone and 1 fax or 1 phone and 1 PC.

Under the Primary Access rate, each subscriber will be able to transmit and receive over 30 B channels (23 in USA) and 1 D channel. This data rate is compatible with the 2.048 Mbps rate for E1 carriers (1.536 Mbps in USA as T1).

Typically, a primary access will link to a complex system that can consists of a PABX or a private network or a MUX. The primary access specifies a 4 wire structure.

In Fig.1 you can see the ISDN scheme for a basic access connection. In the diagram, blocks represent equipment or physical, tangible points along the phone line. Refer to the Text Box 3 for the meaning of the acronyms.

We can distinguish there the main parts of an ISDN link: the LT (Central Office digital line card), the U reference point (U interface), the NT, the S reference point (S interface), the TE (it can be both TE1 or TE2+TA).

The LT or Line Termination performs the functions to send and receive the 2B+D channels exchanged by the Central Office and the user equipment adapting the data format typical of U interface (i.e. 2B1Q or 4B3T) with the data format of the Central Office internal bus that links to the ET (Exchange Termination) where the various channels are routed to the other party.

Functionally the LT consists of a U interface transceiver and a suitable controller for the handling of the maintenance messaging.

Moreover the circuit for remote power feeding is also located on the LT: its function is to provide the power for NT feeding and, in case of emergency also for TE.

This kind of circuitry substitutes the traditional COMBO/SLIC analog line card systems of which SGS-THOMSON is a world wide leader (see SGS-THOMSON Line Card data book for more details).

Each subscriber will have two dedicated U interface transceivers: one in the LT and the other in the NT (close to the customer premises).

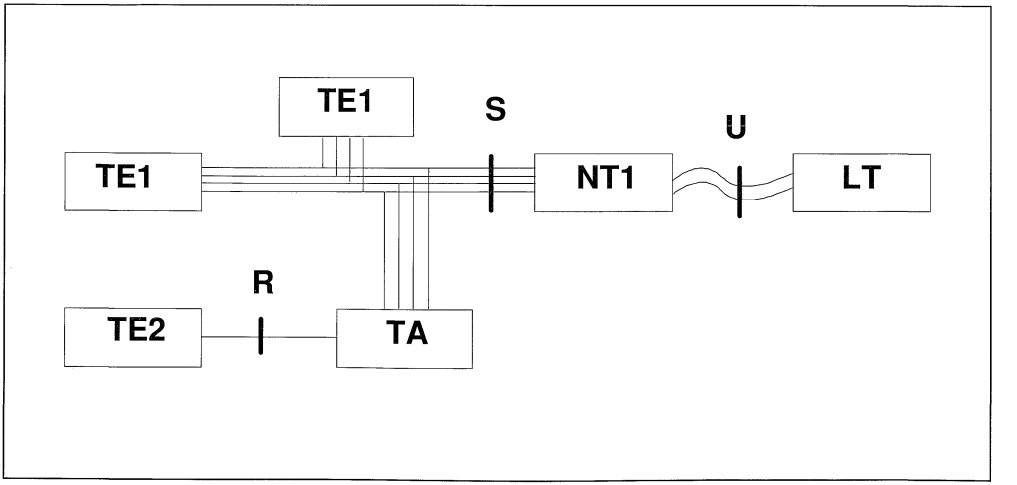
The physical link between the LT and NT is the U interface reference point: it is the standard 2 wire twisted copper cable.

Typically the cable section can be of 0.4mm, 0.6mm or more rarely 0.8mm. It can range up to a distance higher than 5 km for the 0.4mm section while reaching till 9 km for the 0.6mm.

Over these kind of distance a repeater is needed in order to insure a reliable and efficient transmission of data.

The Network Termination or NT terminates the network at the user's end of the 2 wire loop (on the subscribers premises). It is typically a plug

Figure 1: Basic ISDN Loop.



that is located in the subscriber permises. It converts the U interface to the S interface and acts as the master end of the user's line. Just like the TE, the NT is also a CPE (Customer Premises Equipment) and is owned by the PTTs (in USA instead is owned by the user).

The NT is considered CPE and physically resides at the end of the 2 wire loop. The signal exchanged by LT and NT travel only over two wires, the signal must be transmitted in both direction simultaneously. This transmission technique is called 'Echo Cancellation'.

The S interface is a physical link specified as a 4 wire (2 Tx and 2 Rx) bus that is completely regulated by CCITT I.430 specification. The distance over which the S interface can function is limited since in addition to electrically connecting (in parallel) up to 8 TE's with the NT, the S function has to arbitrate the use of these channels to all the TEs resident on the line.

LT	Line Termination
U	U reference point
NT	Network Termination
S	S reference point
TE1	Terminal Equipment 1
TA	Terminal Adaptor
R	R reference point
TE2	Terminal Equipment 2
CPE	Customer Premises Equipment

Text Box 3

For a point to point connection, in which only 1 TE is attached to the NT, the S interface is specified to have a range of 1 km. If the S interface is shared by more than 1 TE, a loop length of only 200 m can be achieved.

The TE or Terminal Equipment can be either a digital telephone, a personal computer, a facsimile machine, a printer or any kind of equipment that is able to interface directly the ISDN network (TE1) or a terminal made before the existence of ISDN that by the use of a TA or Terminal Adaptor function is linked either asynchronously or synchronously to the ISDN bus as synchronized data in the B or D channels.

ISDN LAPD PROTOCOL

In order to set up a user-to-user link and get access to a B channel (the equivalent operation of the dialling in the analog telephone network), certain formalities or protocol must be accomplished. All this message exchange take place in the D channel.

The term LAPD for link access protocol in the D channel is used to describe the message processing to set up a connection via the D channel.

Typically the process is started by the calling end that send the called user identification number to the Central Office using a special format (described in Fig. 2) on the D channel. This special format is defined by the LAPD specification, and is basically composed by two delimiting flags, an address field where the logical (SAPI: Service Access Point Identifier) and physical (TEI: Terminal Endpoint Identifier) type of called user are described, a control field where the type of message being sent is defined, the information field where a message (optional) is contained and the FCS (Frame Check Sequence) field where a CRC code for transmission errors verification is put.

Once the message has been found correct and the proper path to the called user has been set, the link between the two parties take place thanks to a physical B channel link allocation.

D channel is not only used for call set up but also for any kind of information exchange or service demand the user likes to do with the Central Office.

SGS-THOMSON ISDN PRODUCTS

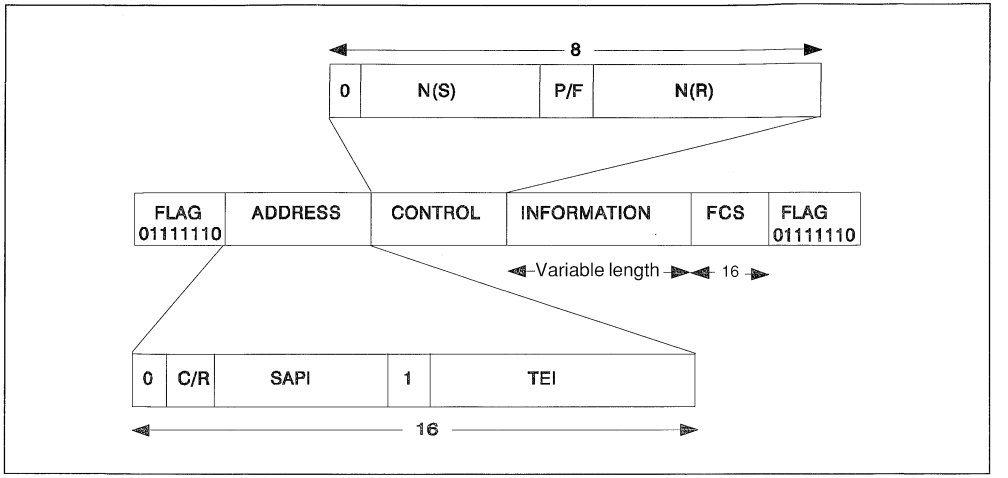
SGS-THOMSON has been working for the last 5 years in the development of the key devices of ISDN: ST5410 U Interface Device for 2B1Q line code, STU2071 U Interface Circuit for 4B3T line code, ST5421 S Interface Device, ST5451 HDLC&GCI controller, ST5430 ISDN Power Supply controller and ST5080 Programmable ISDN Audio Front End. Not only the effort has been spent in product design and development but also in specification study, application investigation, manufacture and engineering, technology research.

The technology choice greatly impact on the invention of ISDN architecture. As a matter of fact, being today activity the cornerstone for tomorrow integration upgrade, design cannot be done with standard processes, but with the most advanced both in term of lithography and metal layers. The HCMOS3/3A technologies are 1.2 micron process with double metal layers: a convenient tool that gives, beside immediate advantage of integration also outstanding geometrical reduction capability.

HCMOS3 is dedicated to fully digital device, while HCMOS3A, thanks to the addition of implanted polysilicon to substrate capacitor is well suited for mixed analog digital device.

ISDN architecture are conditioned not only by the long length link standards , but also the chip-to-chip communication at board level that is extremely important in terms of modularity and expandable potentiality.

Figure 2



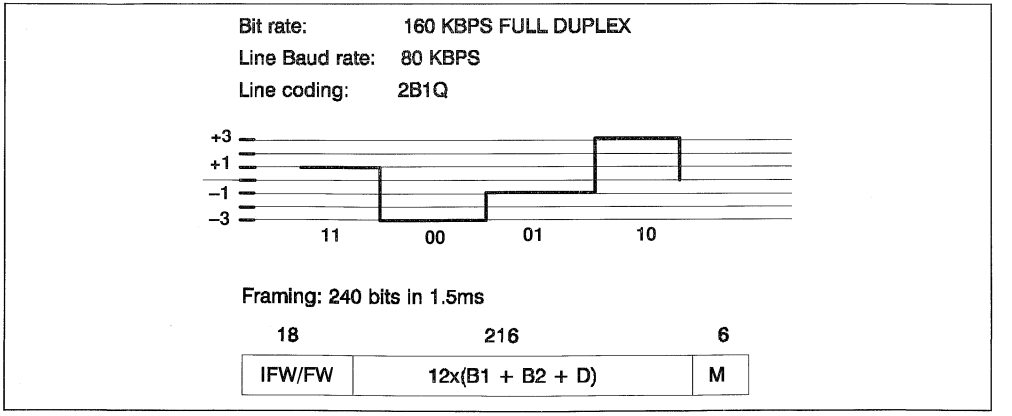
This big industrial problem (big both for semiconductor houses and for equipment manufacturers) has been skillfully solved with the invention of General Circuit Interface (GCI). This is an industrial standard jointly specified by Alcatel, Italtel, Plessey (now GEC Plessey Telecommunications Limited) and Siemens. SGS-THOMSON Microelectronics has participated to the definition of GCI as Associated Semiconductor Manufacturer.

GCI multiplexes on the same bus either voice/data (B channels), signaling (D channel), maintenance and service information (Monitor channel) and management messages (Command/Indicate channel) organized in four octets for a total of 256kHz data rate clocked at a double speed. To support all those data only four wires only are needed (Data-in, Data-out, Frame Synch and Clock) leading to a big simplification in PCB layout. Up to 8 GCI channels can be multiplexed together with a maximum data rate of 3088kHz. In terms of application it means that one GCI master device may drive up to 8 peripherals. GCI, beside having become a de facto standard, has without any doubt advantages in term of PCB layout directness and configuration change simplicity.

ST5410 is the U Interface Device (UID) for 2B1Q line code. This is, by far, the most important device dedicated to ISDN.

SGS-THOMSON target has been to produce a circuit that, beside being fully complying with both ANSI and ETSI specification, has the following characteristics: to be a single chip (28 pin) application, to have a power consumption lower than

Figure 3.



300mW from a single 5V power supply, to be GCI compatible and usable both in Line and Network Terminations.

The device accomplish all the system features to assist in 2B1Q standard procedures: NT/LT activation deactivation, CRC calculation and verification, Superframe/Frame formatting, EOC channel and Overhead bits transmission receiving with automatic messaging checking, on-chip timing recovery, elastic data buffers and backplane clock dejitterization plus digital and analog loopbacks.

ST5410 is expected to reach 5.5km range on 24AWG/26AWG standard cables supporting bridge taps, splices and mixed gauges as per the 15 test loops defined by ANSI to comply with the most complicated subscriber loop configurations.

STU2071 UIC (U Interface Circuit) is the U transceiver for the 4B3T line code. As ST5410 it is a single chip device (28 pin) requiring very low number of external components.

ST5421 S Interface Device with GCI (SID-GCI) is the cornerstone that ST is offering on the market for an easy and efficient design of ISDN Terminal and Network Termination equipments. It can be divided in three parts: the GCI and control digital circuitry, the S line driver and receiver filtering circuits and the blocks related to the control of the operation. ST5421 is fully complying with recommendation I.430 even overcoming the requirements of CCITT as far as the transmission performances are concerned.

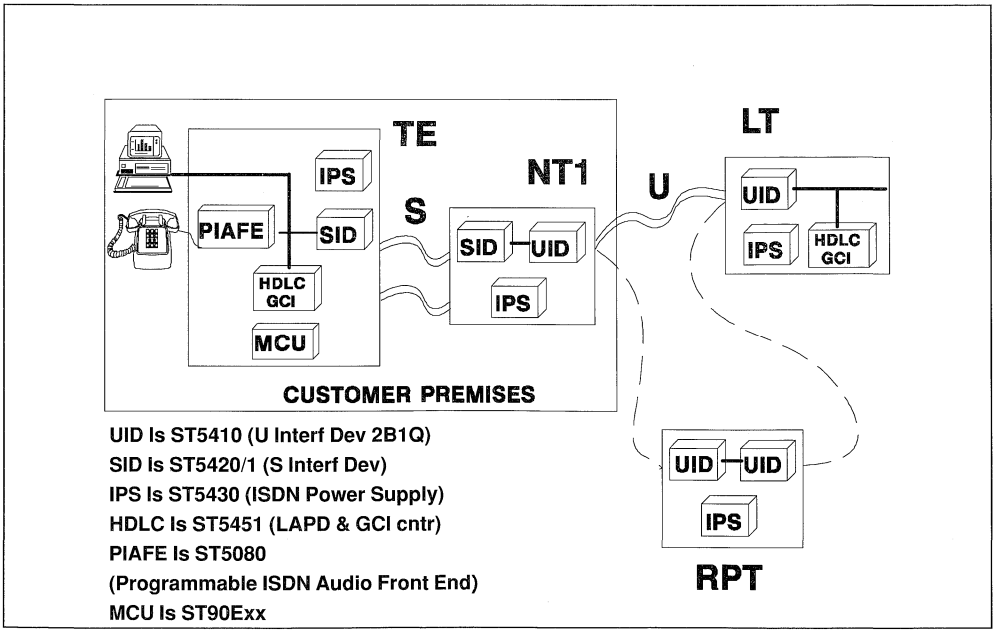
As per I.430, the device handles the four wires S interface (two wire pair: one for Tx and one for Rx) at a rate of 192kbit/s carrying the 2 B channels at 64kbit/s each for data and voice transmission, the D channel at 16kbit/s for signalling and packet data transfer, plus other extra service bits for frame alignment, D bits echo, and S&Q bits for multiframe monitor messaging.

ST5451 handles HDLC packet both in transmit and receive direction implementing LAPD and LAPB procedures. The device can be interfaced to any kind of PCM data stream and handles many different formats of the standard 2B+D channels provided a strobe is set during D bits time window. As far as HDLC packets are concerned ST5451 manages opening and closing flags, checks and calculates CRC, manages SAPI and TEI recognition and handles abort and idle signals.

ST5451 innovation is to be a GCI controller; it performs all the control functions on the Monitor and Command/Indicate channels, that GCI specify to be exchanged with a proper protection protocol to assure the consistency of the service messages exchanged.

SGS-THOMSON HDLC&GCI controller has built-in registers dedicated to Monitor and C/I channels and a logic circuitry that saves the local Up a lot of elaboration time. Moreover a selectable P interface suitable to be used both with multiplexed and non multiplexed intelligent units. When multi-

Figure 4: ISDN Building Blocks.



plexed micro interface is selected a DMA interface is provided; that helps in an optimize and fast access to the 128 bytes built-in FIFOs memories (64 for Tx and 64 for Rx).

ST5430, named ISDN Power Supply controller, is a Switch Mode Power Supply specially studied for ISDN application either in Terminals and in Network Terminations. Among its features for ISDN the soft-start capability, the undervoltage and the polarity reversal detection and the overcurrent detection to go in foldback limitation are the most outstanding. The input voltage can go up to 100 Volt while the oscillator frequency can go from 10 to 100 khz.

ST5080, Programmable ISDN Audio Front End, is much more than a 5V Codec and Filter. Completely programmable in Gains, it features also various characteristics for an easy design of an ISDN or a digital phone. ST5080 features also a built-in loudspeaker amplifier, dual switchable microphone amplifier inputs, internal sidetone circuit, on-chip anti-Larsen circuit and a circuitry for direct connection to very simple hand-free circuit such as the TEA7540 a device that is becoming the star of this kind of application.

GLOSSARY

INTEGRATED SERVICES DIGITAL NETWORK

2B1Q - Line code in which two binary bits are converted into one quaternary symbol for transmission across the U interface. Specified by ANSI and ETSI.

4B3T - Line code in which four binary bits are converted into three ternary symbols for transmission across the U interface.

Access Protocol - A defined set of procedures that is adopted at an interface at a specified reference point between a user and a network to enable the user to employ the services and/or facilities of that network.

Adaptive Equalization - Technique for compensating the effect of different quality and lenght of lines (typically distortion) on the carried signals, getting a flat frequency response.

A-Law - European standard for the digitization of voice in a non-linear manner.

AMI - Alternate Mark Inversion. A special line code where "1s" are represented by 0 volt, "Os" by alternate positive or negative levels. Used over S interface bus.

Amplifier - An electronic circuit used on an analog transmission facility that detects a weak signal and makes it stronger. An amplifier often amplifies the noise on the channel as well as the original signal.

ANSI (American National Standard Institute) - It coordinates the activity of ITU and ISO for U.S. and defines the communication standard there.

Architecture - An overall scheme or plan that may be partially or fully implemented. An architecture represents the goal toward which its implementors strive. The term architecture is often used to describe database management systems, operating systems, data communication systems, and other highly complex software/hardware mechanisms.

Attenuation - Decrease in the magnitude of current, voltage, or power of a signal in trasmission between two points. Can be expressed in decibels (dB).

Audio Frequencies - Frequencies that can be heard by the human ear (typically 30 to 20,000 hertz). In Telecom (telephone) the filters limit the bandwidth to 340/3400Hz range.

Bandwidth - The range of frequencies available. The difference expressed in Hertz (cycles per second) between the highest and lowest frequencies of a frequency band.

Baud - Unit of signaling speed. The speed in baud is the number of discrete conditions, or signal events, per second. If a signal event represents only one bit condition, the line speed in baud is the same as the bit rate in bits per second. When each signal event represents other than one bit, baud does not equal bits per second.

B Channel - A switchable, optionally transparent, 64k-bps channel. Two B channels are included in the ISDN basic-rate service.

Bearer services - Basic communications services. Includes 64kbit/s circuit switched digital services to be used for both voice telephony and non-voice services; packet switched services operating at speeds of up to 1.5 Mbit/s in North America and 2 Mbit/s in Europe.

BER (Bit Error Rate) - The ratio of the number of data units in error to the total number of data units.

BRA - Basic Rate Access.

Burst - Several events occuring within a short period of time.

CCITT (Comite' Consultatif International Telegraphique et Telephonique) - An organization in the International Telecommunication Union that publishes recommendations of importance to data communication. Reccommendation X.25 is published by the CCITT.

Centrex - A service offered by operating telephone companies which provides, from the telephone company central office, functions and features comparable to those provided by a PBX.

CEPT - Conference for European Post and Telecommunications.

Channel - A transmission path between two points. It is usually the smallest subdivision of a transmission system by means of which a single type of communication service is provided.

Circuit Switching - A method of communicating in which a dedicated communications path is established between two devices through one or more intermediate switching nodes. Unlike packet switching, digital data are sent as a continuous stream of bits. Data rate is guaranteed, and delay is essentially limited to propagation time. Provides a permanent end-to-end path between two terminals for the duration of the communication.

CMOS (Complementary Metal Oxide Semiconductor) - A technology where both MOS p-channel and n-channel are diffused together.

CO (Central Office) - The place where communication common carriers terminate customer lines and locate the switching equipment that interconnects those lines. Also referred to as an exchange, end office, or local central office (see LT).

CPE (Customer Premises Equipment) - The apparatus present at the user location that allows connection to the line; in ISDN they are NT and TE.

CODEC (Coder/decoder) - Transforms analog data into a digital bit stream (coder), and digital signals into analog data (decoder).

COMBO - Combined codec and filter IC. It supports voice transmission over an ISDN network by converting analog signals in a telephone handset into the digital signals required by the module interface.
COMBO is a trademark of National Semiconductor.

Common Carrier -In the United States, companies that furnish long-distance telecommunication services to the public. Common carriers are subject to regulation by federal and state regulatory commissions.

Common Channel Signaling - A method of signaling in which signaling information relating to a multiplicity of circuits, or function or for network management, is conveyed over a single channel by addressed messages.

Contention - A method of line control in which the terminals request to transmit. If the channel in question is free, transmission proceeds; if it is not free, the terminal waits until the channel becomes free.

CRC (Cyclical Redundancy Check) - Use of a particular type of arithetic algorithm for generating error detection bits in a data link protocol (as CRC4 or CRC16).

Crosstalk - The unwanted transfer of energy from one circuit, called the disturbing circuit, to another circuit, called the disturbed circuit.

CSDN - Circuit Switched Digital Network.

D Channel - A channel whose primary purpose is to convey signaling information between a terminal and the network switch but whose surplus capacity can be used for user-packet data and other data, such as telemetry. It operates at 16k bps for basic-rate access and 64k bps for primary-rate access usually in HDLC format.

Decibel (dB) - One-tenth of a bel. A unit for measuring relative strength of a signal parameter, such as power or voltage. The number of decibels is 10 times the logarithm (base 10) of the ratio of the measured quantity to the reference level. The reference level must always be indicated, such as 1 milliwatt for power ratio.

Digital PBX - A private branch exchange (PBX) that operates internally on digital signals. Thus, voice signals must be digitized for use in the PBX.

Digital Transmission - The transmission of digital data or analog data that have been digitized, using either an analog or digital signal, in which the digital content is recovered and repeated at intermediate points to reduce the effects of impairments, such as noise, distortion, and attenuation.

DSI (Digital Systems Interface) - A chip-to-chip interface for ISDN modules, supported both by National Semiconductor and SGS-THOMSON.

ET (Exchange Termination) - The part of Central Office that implements channel switching.

ETSI - European Telecommunication Standard Institute.

Exchange Area - A geographical area within which there is a single uniform set of charges for telephone service. A call between any two points within an exchange area is a local call.

Filter - A network designed to transmit of frequencies within one or more bands and to attenuate of other frequencies.

Flow Control - A function performed by a receiving entity to limit the amount or rate of data sent by a transmitting entity.

Format - A specified arrangement of data that permits identification of control and information fields by their location in the transmitted data stream.

Four Wire Circuit - A facility in which transmission is done over a twisted pair and reception is done over another twisted pair.

Frame - Sequence of time slots repeated according to sampling rate. In BRA frame consists of 48 bit time slots repeated every 250 us. In PRA a frame consists of 192 bit time slots (N.A. standards) /256 bit time slots (CCITT/E1, CEPT) repeated every 125 µs.

Full-Duplex Transmission - Transmission of data in both directions at the same time.

GCI - The General Circuit Interface (GCI) is a standard interface between devices for subscriber access in ISDN and analogue enviroments. The principle use in the various applications is to control the subscriber line interface circuitry. It is intended that GCI will gain international acceptance as an industry standard due to its well defined and supported features.

GCI-SCIT - Special version of GCI for terminal application.

Half-Duplex Transmission - Data transmitted in either direction, one direction at a time.

Handshaking - Exchange of predetermined signals for purposes of control when a connection is established over a data link.

HDLC (High Level Data Link Control) - Bit-oriented protocol to ensure integrity of data during the transmission process by adding control information in a special frame format, standardized by the International Standards Organization (ISO) and documented in ISO Standards 3309 and 4435.

HDLC Controller - A circuit for full HDLC frame control, eg. ST5451, available from SGS-THOMSON.

IDN (Integrated Digital Network) - A communication network that combines the technologies of digital switching and digital transmission of information.

IEEE (Institute of Electrical and Electronics Engineers) - An organizatiion that, among other activities, produces data communication standards. Particularly important are the IEEE 802 group of standards for variious types of local area networks.

Inband Signaling - Signaling that uses the same paths and frequencies as that used for voice or data messages.

Interface - A common boundary between two systems or pieces of equipment that ensures proper connection between equipment.

ISDN (Integrated Services Digital Network) - A communication network that uses an integrated digital network (IDN) to carry all forms of traffic, such as voice, computer data, and facsimile.

ISO (International Standards Organization) - An international organization for standardization. ISO publishes many standards that are important for data communication. The OSI Refereference Model is being developed by the ISO.

ITU (International Telecommunication Union) - The telecommunications agency of the United Nations, established to provide standardized communication procedures and practices including frequency allocation and radio regulations on a worldwide basis. The CCITT is part of the ITU. (See also International Telegraph and Telephone Consultative Committee.)

LAN - Local Area Network.

LAPB & LAPD (Link Access Protocol Balanced & D Channel) - Bit-oriented data link protocols standardized by the CCITT that specify the functions of the data link level of CCITT Recommendation X.25. LAP and LAPB are compatible subsets of HDLC. (See also HDLC.)

Local Loop - A transmission path, generally twisted pair, between the individual subscriber and the nearest switching center of a public telecommunications network. Also referred to as a subscriber loop.

LOOP - A pair of wires carrying direct current between central office and a customer's terminal.

LT (Line Termination) - A digital line card (usually equipped with U interface or S interface device) that provides termination of the subscriber loop at the PBX or central office.

MICROWIRE - Synchronous serial data transfer between a microcontroller and one or more serial device. It is supported by both National and SGS-THOMSON.
MICROWIRE is a trademark of National Semiconductor

Modulation - The process by which some characteristic of one wave is varied in accordance with another wave or signal. This technique is used in modems to make data machine signals compatible with communication facilities.

Multiplexing - Use of common channel in order to make two or more channels, either by splitting the frequency band transmitted by the common channel into narrower bands, each of which is used to constitute a distinct channel (frequency-division multiplexing), or by allowing this common channel to several information channels, one at a time (time-division multiplexing).

NMOS (N-channel Metal Oxide Semiconductor) - A technology where MOS n-channel is diffused.

Noise - Random electrical signals, introduced by circuit components or natural disturbances, that tend to degrade the performance of a communication channel.

NT1 (Network Termination 1) - An equipment (located at customer premises) that, beside terminating the U line, converts the U line code (2B1Q or 4B3T) into the S interface format (I.430).

NT2 (Network Termination 2) - Functionally similar to a PABX in that it can accept many S lines on the Network side, connect to many S lines of the user side and provide also internal switching capability.

OSI (Open System Interconnection) - This model for the construction of data networks was first published by the ISO in November 1978. It was intended to provide a basis for open systems architecture a network in which there is no single central control point, but the inweheel control resides in various nodes of the network operating to common standards. Each control level provides a clear definition of the protocols and formats and allows interaction between users who have implemented the architecture. The control levels or layers have been defined as follows:
Layer 1 - Physical Layer. The phisical transport of the bit stream.
Layer 2 - Data Link Layer.
Layer 3 - Network Layer. Provides routing and relaying through intermediate systems.
Layer 4 - Transport Layer. Provides transparent, error-free transmission between end-systems.
Layer 5 - Session Layer. Handles the dialogue between communicating processes.
Layer 6 - Presentation Layer. Concerned with standard presentation of information.
Layer 7 - Application Layer. Provides the user with network services via applications programs.

PABX (Private Automatic Branch Exchange) - An automatic, private switchboard linked to the Central Office with a analog or digital connection and with several internal users providing also special internal services (conference, automatic busy line recall, abbreviated selection and so on).

Packet Switching - The techinique of transmitting units of data (called packets) of some fixed maximum size through a mesh-structured network from an originating station to a destination station. In packet switching, a physical path is not set up between the originating and destination station. Contrast with Circuit switching.

PCM (Pulse-Code Modulation) - A modulation technique in which a pulse train is created in accordance with a code. With PCM, the input signal is first quantized, and the signal amplitude at a particular instant in time is represented by a binary numer that can be transmitted over a digital communication channel as a series of pulses of some fixed amplitude. PCM is used to convert an analog signal, such as telephone voice, into a digital bit stream.

PDN (Public Data Network) - A communication network, designed specifically for the transmission of computer data, that is used by many individual subscribers. Most public data networks use the technique of packet switching rather than circuit switching.

Point - to - Point - A network configuration in which two communicating stations are connected by a single communications channel that is not shared by any other stations.

PRA (Primary Rate Access) - Multiplexed communication link to an ISDN where the link has a channel structure consisting of either 23 or 30 B channels for voice or data and one D channel for control.

PRI (Primary Rate Interface) - A full digital connection, typically between PABX and CO or CO and CO, at 2Mbit/s in Europe (PCM30) and at 1.544Mbit/s in U.S. (PCM24).

Protocol - A formal statement of the procedures that are adopted to ensure communication between two or more functions within the same layer of a hierarchy of functions.

PTT - Postal Telephone and Telegraph. Generic term for European telephone administration.

R Interface - Connects a terminal adapter (TA) to non ISDN (TE2) equipment, often through an RS-232C port. Industry-standard serial data transmission interface. Developed for single-ended data transmission at

up to 19.2 Kb/s. Industry-standard differential data transmission interface. Developed for long distances and noise environments.

RBOC (Regional Bell Operating Company) - Before the divestiture of AT&T, the 22 Bell Operating Companies were AT&T subsidiaries that built, operated, and maintained the local and intrastate network and provided most of the day-to-day service for customers. Alter divestiture, the BOCs retain their identity within seven regional companies (RBOCs) and are responsible for local service as defined by local access and transport areas (LATAs).

RS-423 - Industry-standard data transmission interface. Developed for single ended data transmission with a maximum data rate to 100 Kbaud (up to 30 ft.) and a maximum distance of 4000 feet (up to 1 Kbaud).

S interface - A 4 wire 1000 meter Basic Access interface between various TE/TA or NT equipment. Usually applied within a Private Network such as PBX. The point where ISDN terminal equipment (TE) customer premise can connect to network termination (NT) equipment. Fully defined by CCITT recommendation I.430.

SAPI (Service Access Point Identifier) - A field of LAPD frame that indicates the logical address of the called user.

Signaling - The exchange of information specifically concerned with the establishment and control of connections, and with management, in a telecommunication network.

SS 7 (Signaling System Nr.7) - CCITT standards for communicating between ISDN carrier switches where signaling infos are one common channel.

TA - Terminal Adaptor. This function rate adapts existing non-ISDN terminals, printer, etc., to the ISDN.

TE1 - Terminal equipment. Any terminal, printer, phone, voice/data terminal designed to be compatible with and directly connected to ISDN.

TE2 - Terminal Equipment, non-ISDN.

TEI (Terminal Equipment Identifier) - A field of LAPD frame that indicates the physical address of the called user.

Teletext - A one-way information retrieval service. A fixed number of information pages are repetitively broadcast on unused portions ofa TV channel bandwidth. A decoder at the TV set is used to select and display pages.

Time Compression Multiplexing - A means for providing full-duplex digital data transmission over a single twisted pair. Data are buffered at each end and are sent across the line at approximately double the subscriber data rate, with the two ends taking turns.

T Interface - Electrically identical to the S interface, the T interface has a different protocol than the S interface to link NT2 boxes to the NT1 box.

Transceiver - Transmitter - Receiver.

Twisted Pair - A pair of wires used in transmission circuits that are twisted together to minimize coupling.

μLaw - North American standard for the digitization of voice in a non-linear manner.

UART - Universal Asynchronous Receiver/Transmitter. Local serial channel.

U Interface - A twisted-pair subscriber loop that provides basic-rate access to the NT1 reference point from the ISDN network (typically LT). This interface only supports point-to-point operation.

Videotex - A two-way information retrieval service accessible to terminals and TV sets equipped with a special decoder. Pages of information at a central resource are retrieved interactively over a switched telephone line connection.

Wideband - Communication channel having a bandwidth greater than a voice-grade channel and therefore capable of higher-speed data transmission. Sometimes called broadband.

ISDN

Type Number	Function	Page
GS1T70-D540	ISDN DC-DC Converter	275
ST5080	Piafe Programmable ISDN Audio Front End	245
ST5410	2B1QU Interface Device	27
ST5410	User Manual	81
ST5420	Sid-µW: S/T Interface Device with Microwire/DSI	153
ST5421	Sid-GCI: S/T Interface Device with GCI	187
ST5430	ISDN Power Supply	207
ST5451	ISDN HDLC and GCI Controller	213
STU2071	4B3TU Interface Circuit	139
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DATACOM

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MK5021	Technical Manual	293
MK5025	CCITTZ.25 Link Level Controller	339
MK50H25	High Speed X.25 Link Level Controller	379
MK5027	SS7 Signalling Link Controller	381
MK5029	Technical Manual	399

Application Note Number	Function	Page
AN489	MK5025 Single Channel LAPD	451
AN490	MK5025 NET2 Conformance	453
AN491	MK5025 Daisy Chain DMA	455
AN492	MK5025 NRZ to NRZI Conversion	459
AN493	MK5025 Transparent Mode	461
AN494	MK5025 Synchronous Timing	465

ISDN DATASHEETS

2B1Q U INTERFACE DEVICE

ADVANCE DATA

GENERAL FEATURES

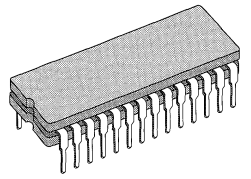
- SINGLE CHIP 2B1Q LINE CODE TRANSCEIVER
- SUITABLE FOR BOTH ISDN AND PAIR GAIN APPLICATIONS
- MEETS OR EXCEEDS ANSI T1.601-1988 U.S. STANDARD
- MEETS OR EXCEEDS ST/LAA/ELR/822 FRENCH SPECIFICATIONS
- SINGLE 5V SUPPLY
- 28 PINS PACKAGE
- 300mW ACTIVE AND 10mW INACTIVE POWER DISSIPATION
- HCMOS3A SGS-THOMSON ADVANCED DOUBLE-METAL SINGLE-POLY CMOS PROCESS

TRANSMISSION FEATURES

- 160 KBIT/S FULL DUPLEX TRANSCEIVER
- 2B1Q LINE CODING WITH SCRAMBLER/DESCRAMBLER
- 18KFT (5.5KM) ON 26AWG/24AWG TWISTED PAIR CABLES
- SUPPORTS BRIDGE TAPS, SPLICES AND MIXED GAUGES
- >70DB ADAPTIVE ECHO-CANCELLATION
- DIGITAL FEEDBACK EQUALIZATION
- ON CHIP TIMING RECOVERY WITHOUT EXTERNAL PRECISION COMPONENTS
- DIRECT CONNECTION TO SMALL LINE TRANSFORMER

SYSTEM FEATURES

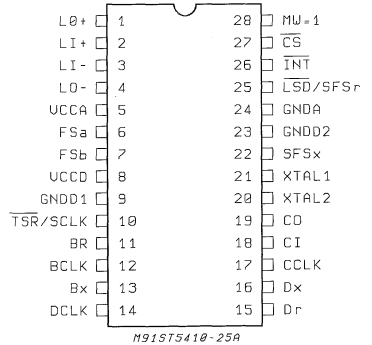
- ACTIVATION/DEACTIVATION CONTROLLER
- ON CHIP CRC CALCULATION AND VERIFICATION INCLUDING PROGRAMMABLE BLOCK ERROR COUNTER
- EOC CHANNEL AND OVERHEAD-BITS TRANSMISSION WITH AUTOMATIC MESSAGE CHECKING
- GCI AND MW/DSI MODULE INTERFACES COMPATIBLE
- DIGITAL LOOPBACKS
- ELASTIC DATA BUFFERS AND BACKPLANE CLOCK DE-JITTERIZER



Ceramic DIP28

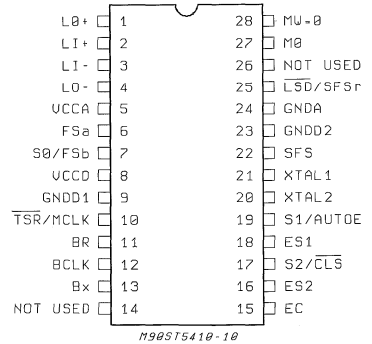
PIN CONNECTIONS (Top views)

MICROWIRE MODE



M91ST5410-25A

GCI MODE



M90ST5410-10

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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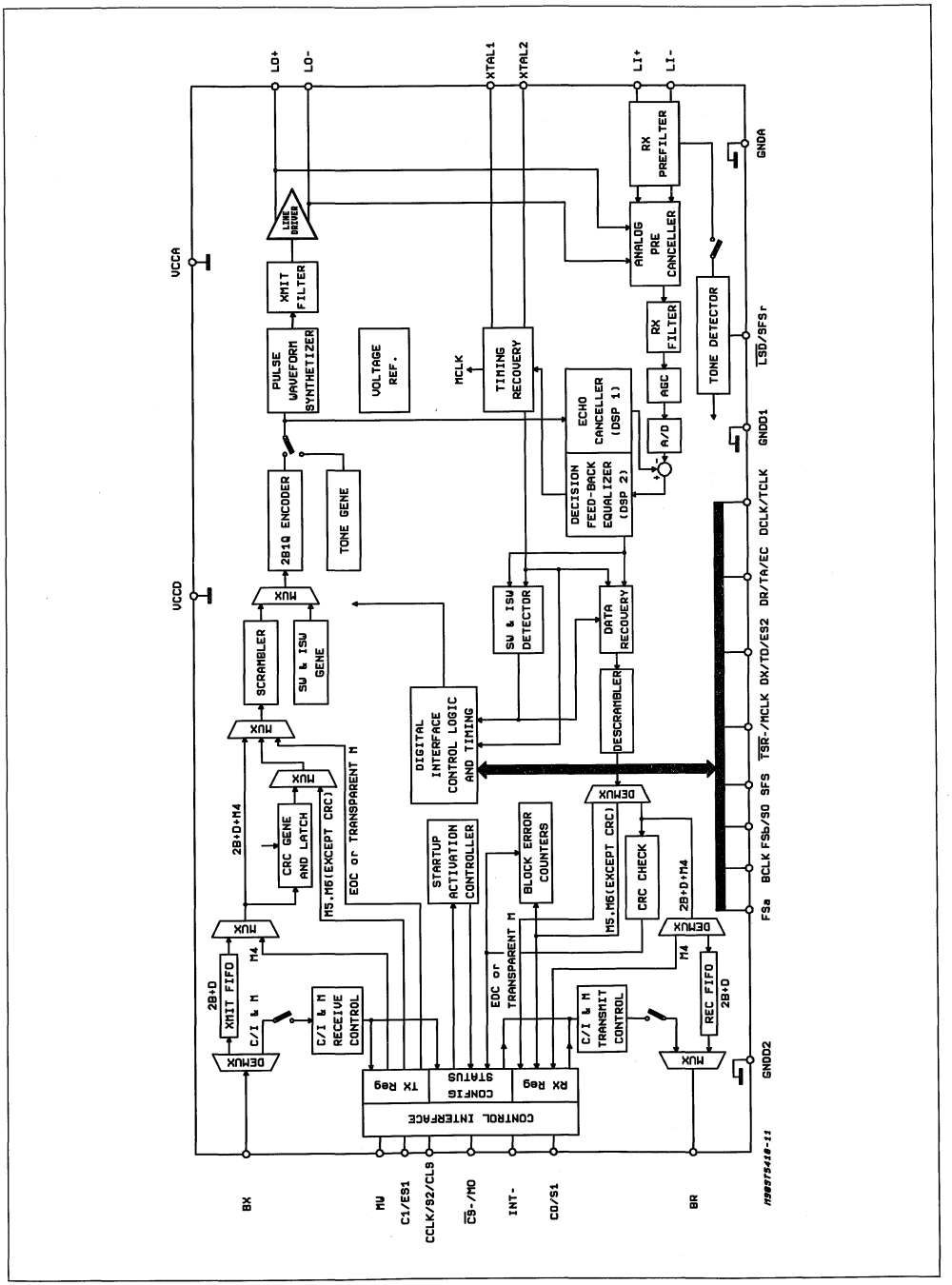
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Figure 1: ST5410 Block Diagram.



GENERAL DESCRIPTION

ST5410 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device is fully compatible with both ANSIT1.601-1988 U.S. and ST/LAA/ELR/822 French specifications.

The equivalent of 160 kbit/s full-duplex transmission on a single twisted pair is provided, according to the formats defined in the a.m. spec. Frames include two B channels, each of 64 kbit/s, one D channel of 16 kbit/s plus an additional 4 kbit/s M channel fcr loop maintenance and other user functions. 12 kbit/s bandwidth is reserved for framing. 2B1Q Line coding is used, where pairs of bits are coded into one of 4 quantum levels. This technique results in a low frequency spectrum (160 kbit/s turn into 80 kband), thereby reducing both line attenuation and crosstalk and achieving long range with low Bit Error Rates.

The system is designed to operate on any of the standard types of cable pairs including mixed gauges (26AWG, 24 AWG and 22 AWG) linking the loop by means of one simple transformer. Good noise margins are achieved even when bridged taps are present. On 26AWG cable, the transmission range is in excess of 5.5 km (18 kft) in presence of crosstalk and noise as specified by ANSI standard. ST 5410 is designed to operate with Bit Error Rate less than 10^{-6} on 45 dB loss loops with near-end Crosstalk (NEXT) of 52 dB as specified in european ETSI recommendation.

To meet these very demanding specifications, the device includes two Digital Signal Processors, one configured as an adaptive Echo-Canceller to cancel the near end echoes resulting from the transmit/recive hybrid interface, the other as an adaptive line equalizer. A Digital Phase-Locked Loop (DPLL) timing recovery circuit is also included that provides in NT1 a 15.36 MHz synchronized clock to the rest of the system. Scrambling and descrambling are performed as specified in the US and French specifications.

On the system side, ST5410 can be linked to two bus configuration simply by pin MW bias.

MICROWIRE(μW)/DSI mode (MW= 5V): 144 kbit/s 2B+D basic access data is transferred on a multiplex Digital System Interface with 4 different interface formats (see fig. 2 and 3) providing maximum flexibility with a limited pin count (BCLK, Bx, Br, FSa, FSb). Three pre-defined 2B+D formats plus an internal time slot assigner allows direct connection of the UID to the most common multiplexed digital interfaces (TDM/IDL). Bit and Frame Synchronisation signals are inputs or outputs depending on the configuration selected. Data buffers allow any phase shift between the line and the digital interface. That permits building of slave-slave configurations e.g. in NT12 trunk-cards.

It is possible to separate the D from the B channels and to transfer it on a separate digital interface (Dx, Dr) using the same bit and frame clocks as for the B channels or in a continuous mode using an internally generated 16 kHz bit clock output (DCLK).

All the Control, Status and Interrupt registers are handled via a control channel on a separate serial interface MICROWIRE compatible (CI, CO, $\overline{CS}$, CCLK, $\overline{INT}$) supported by a number of microcontroller including the ST6, ST9 and COPS families from SGS-THOMSON

GCI mode (MW= 0V). Control/maintenance channels are multiplexed with 2B+D basic access data in a GCI compatible interface format (see fig. 4a) requiring only 4 pins (BCLK, Bx, Br, FSa). On chip GCI channel assignement allows to multiplex on the same bus up to 8 GCI channels, each supporting data and controls of one device. Bit and Frame Synchronisation signals can be inputs or ouputs depending on the configuration selected. Data buffers, again, allow to have any phase between the line interface and the digital interface.

Through the M channel and its protocol allowing to check both direction exchanges, internals register can be configurated, the EOC channel and the Overhead-bits can be monitored. Associated to the M channel, there are A and E channels for enabling the exchanged messages and to insure the flow control. The C/I channel allows the primitive exchanges following the standard protocol.

In both mode (μW and GCI) CRC is calculated and checked in both directions internally.

In LT mode, the superframe can be synchronized by an external signal (SFS) or be self running. In NT mode the SFS is always output synchronized by the transmit superframe.

Line side or Digital Interface side loopbacks can be selected for each B1, B2 or D channel independently without restriction in transparent or in non-transparent mode.

Activation and deactivation procedures, which are automatically processed by UID, require only the exchange of simple commands as Activation Request, Deactivation Request, Activation Indication. Cold and Warm start up procedures are operated automatically without any special instruction.

PIN FUNCTIONS

Pin	Name	Description
1, 4	LO+, LO-	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the proper line interface circuit the line signal conforms to the output specifications in ANSI standard with a nominal pulse amplitude of 2.5 Volts.
2, 3	LI+, LI-	Receive 2B1Q signal differential inputs from the line transformer.
5, 8	VCCD, VCCA	Positive power supply input for the analog and digital sections, which must be +5 Volts +/-5% and must be directly connected together.
6	FSa	When the Digital Interface clocks are selected as inputs, this signal must be a 8 kHz clock input which indicates the start of the frame on the Digital Interface data input pin Bx. In microwire mode two phases between the rising edge of FSa and the first slot of the frame can be selected by means of bit DDM in CR1: Delayed timing mode or non Delayed timing mode. When GCI Format is selected, FSa defines the frame begining for both Tx and Rx directions and non delayed timing mode is automatically selected. When the Digital Interface clocks are selected as outputs, FSa is a 8KHz output pulse conforming with the selected Interface format.
9, 23, 24	GNDD1, GNDD2, GNDA	Negative power supply pins, which must be connected together close to the device. All digital and analog signals are referred to these pins, which are normally at the system Ground.
10	$\overline{\text{TSR}}$	(LT configuration only) This pin is an open drain output normally in the high impedance state which pulls low when B1 and B2 time-slots are active. It can be used to enable the Tristate control of a backplane line-driver.
	MCLK	(NT mode only) 15.36 MHz clock output which is frequency locked to the received line signal (unlike the XTAL pins, it is not freerunning) .
11	Br	Data output: 2B+D basic access data received from the line can be shifted out from the TRISTATE output Br at the BCLK frequency on the rising edges during the assigned time slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only BI & B2 data is shifted out from Br on the rising edges of BCLK. In Format 4 and GCI mode, data is shifted out at half the BCLK frequency on the transmit rising edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels and output Br becomes open drain. There is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

PIN FUNCTIONS (Continued)

in	Name	Description
12	BCLK	Bit Clock: This signal determines the data shift rate on the Digital Interface.When slave mode is selected,,BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz. When master mode is selected , BCLK is an output at 256 kHz, 512 kHz, 1536 kHz, 2048 kHz or 2560 kHz depending on the selection in Command Register 1. BLCK is synchronous with FSa/b Frame syncsignals and phase locked to the recovered clock received from the line. In formats 1-3, data is shifted in and out at the BCLK frequency. In format 4 and in GCI mode, data is shifted in and out at half the BCLK frequency.
1 3	Bx	Data input: 2B+D basic access data to transmit to the line can be shifted in at the BCLK frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in at the BCLK frequency on the falling edges during the assigned time slots. In format 4 and in GCI mode, data is shifted in at half the BCLK frequency on the receive falling edges. When GCI mode is selected, 2B+D data is combined with the GCI Control channels.
20	XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, if used. Otherwise, this pin must be left no connected.
21	XTAL1	The master clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a logic level clock input from a stable source. This clock does not need to be synchronized to the digital interface clocks (FSa, BCLK).Crystal specifications: 15.36 MHz +/-50ppm parallel resonant; Rs ≤ 20 ohms; load with 33pF to GND each side.
22	SFS	Super Frame synchronization I/O: When LT configuration is selected, the rising edge of SFS indicates the beginning of the Transmit Super Frame on the line. Two modes can be selected. In the first mode, SFS is an input that synchronizes the Transmit Frame counter of the UID core. SFS must be synchronous with FSa but with any phase . In the second mode, SFS is a square wave output issued from the free-running Transmit Frame counter. When NT configuration is selected, SFS is always a square wave output which indicates the beginning of the Transmit Superframe. There is no direct phase-relation between the data on the line and the data on the digital interface.
25	$\overline{\text{LSD}}$	Line Signal Detect output (default conf.): This pin is an open drain output which is normally in the high impedance state but pulls low when the device previously in the power down state receives a wake-up by Tone from the line. This signal is intended to be used to wake-up a micro-controller from a low power idle mode. The $\overline{\text{LSD}}$ output goes back in the high impedance state when the device is powered up.
	SFSr	Super Frame Synchronization output. When LT configuration is selected, it is possible to configurate pin 25 as SFSr that provides a square wave output indicating the beginning of the received Super Frame from the line. As for SFSx, there is no direct phase-relation between the data on the line and the data on the digital interface.
28	MW	MICROWIRE selection: When set high, MICROWIRE control interface is selected. All the internal registers can be accessed through it. When set low, GCI interface is selected. All the internal registers can be accessed through the GCI Monitor and Command/Indicate Control channels.

PIN FUNCTIONS (Specific to MICROWIRE MODE ONLY (MW = 1))

Pin	Name	Description
	FSb	This is a 8 kHz clock input which define the start of the frame on the Digital Interface data ouput pin Br. Two phases between the rising edge of FSb and the first slot of the frame can be selected with the same command as for FSa; Delayed timing mode or non Delayed timing mode. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse conforming with the selected format.
14	DCLK	(D channel port enabled, continuous mode selected) D channel Clock output: when the D channel port is enabled in continuous mode, data are shifted in and out at 16 kHz on the falling and rising edges of DCLK respectively. DCLK is synchronous with the BCLK frequency. When DCLK is disabled, it must be tied to GNDD.
15	Dr	(D channel port enabled) D channel data output: when the D channel port is enabled, D channel data is shifted out from the UID on this pin in two selectable modes: In multiplexed mode, data is shifted out at the BCLK frequency on the rising edges when the assigned time slot is active. In continuous mode, data is shifted out at the DCLK frequency on the rising edge continuously.
16	Dx	(D channel port enabled) D channel data input: When the channel port is enabled, D channel data is shifted in the UID on this pin in two selectable modes: In multiplexed mode, data is shifted in at the BCLK frequency on the falling edges when the selected receive time slots are active. In continuous mode, data is shifted in at the DCLK frequency on the falling edge continuously. When the D channel port is disabled, Dx must be tied to GNDD.
17	CCLK	Clock input for the MICROWIRE control channel: data is shifted in and out on the rising and falling edges of CCLK respectively. CCLK may be asynchronous with the digital interface clock.
18	CI	MICROWIRE control channel serial input: two bytes data is shifted into the UID on this pin on the rising edges of CCLK.
19	CO	MICROWIRE control channel serial output: two bytes data is shifted out from the UID on the falling edges of CCLK. When not enabled by $\overline{CS}$, CO is high-impedance.
26	$\overline{INT}$	Interrupt output: Latched open-drain output signal which is normally high impedance and goes low to request a read cycle. Pending interrupt data is shifted out from CO at the following read-write cycle. Several pending interrupts may be queued internally and may provide several interrupt requests. $\overline{INT}$ is freed upon receiving of $\overline{CS}$ low and can goes low again when $\overline{CS}$ is freed.
27	$\overline{CS}$	Chip Select input: When this pin is pulled low, data can be shifted in and out from the UID through CI & CO pins. When high, this pin inhibits the MICROWIRE interface. For normal read or write operation, $\overline{CS}$ has to be pulled low for 16 CCLK periods of time.

PIN FUNCTIONS (Specific to GCI MODE ONLY (MW = 0))

Pin	Name	Description
15	EC	External Control Output: controlled by the bit LEC in the TxM56 register.
18, 16	ES1,ES2	External Status inputs: during full synchronization the status of ES1, ES2 is loaded in the LES1, LES2 bits of the RxM56 register at each status change and an interrupt is issued. In NT mode, with AUTOE = 1, ES1/ES2 status are automatically sent on the line as ps1/ps2.
27	M0	GCI clocks I/O selection: when M0 is set low, BCLK and FSa clocks are inputs. BCLK can have any value between 512 kHz and 6176 kHz. GCI is selected in slave mode. When M0 is set high, BCLK and FSa clocks are outputs. FSa is a 8 kHz clock signal while BCLK is a 512 kHz or a 1536 kHz depending on CLS pin polarization. GCI channel 0 is automatically selected.In addition, when M0 is set high, NT configuration is also selected. When M0 is set low, NT or LT configuration must be selected through Configuration Register 2.
7,19,17	S0/FSb, S1/AUTOE, S2/CLS	(M0 = 0: slave mode) GCI number selection: these 3 pins S0, S1, S2 are significant when GCI is selected in slave mode only. A GCI channel constituted of 32 bits and relative to one basic access can be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection among 8 available GCI channels is made by programming the S0-S2 pins. (M0 = 1: master mode) S0 becomes FSb (output pulse indicating 2nd 64Kbit time slot.) S1 becomes AUTOE (input) S2 becomes $\overline{CLS}$ (input) GCI Clock Selection: while M0 is set high, $\overline{CLS}$ high selects the 1536 kHz frequency on BCLK and $\overline{CLS}$ low selects the 512 kHz frequency on BCLK.

FUNCTIONAL DESCRIPTION

Digital Interfaces

ST5410 provides a choice between two types of digital interface for both control data and (2 B + D) basic access data.

These are:
a) General Circuit Interface: GCI.
b) Microwire/Digital System Interface: µW/DSI

The device will automatically switch to one of them by sensing the MW input pin at the Power up.

µW/DSI MODE

Microwire control interface
The MICROWIRE interface is enabled when pin MW equal one. Internal registers can be written or read through that control interface.
It is constituted of 5 pins:

CI: data in
CO: data ouput
CCLK: data clock input
$\overline{CS}$: Chip Select input
$\overline{INT}$: Interruption output

Transmission of data onto CI & CO is enabled when $\overline{CS}$ input is low.

A Write cycle or a Read cycle is always constituted of two bytes. CCLK must be pulsed 16 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial Receive input register on the rising edge of each CCLK pulse. At the same time, data from the Transmit output register is shifted out onto the CO ouput on the falling edge of each CCLK pulse. The bit 7 (the first) is available as soon as $\overline{CS}$ goes low.

You can write in the UID on CI while the UID send back a register content to the microprocessor. If the UID has no message to send, it forces the CO output to all zero's.

If the UID is to be read (status change has occured in the UID or a read-back cycle has been requested by the controller), it pulls the $\overline{INT}$ output low until $\overline{CS}$ is provided. $\overline{INT}$ high to low transition is not allowed when $\overline{CS}$ is low (the UID waits for $\overline{CS}$ high if a pending interrupt occurs while $\overline{CS}$ is low) .

When $\overline{CS}$ is high, the CO pin is in the high impedance state.

Note: Special format is used for EOC channels.

Write cycle
The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: Write/Read Indicator
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the adressed register.
A0 set high indicates a read-back cycle request and the byte following is not significant. The UID will respond to the request with an interrupt cycle. It is than possible for the micro to receive the required register content after several other pending interrupts.

Read cycle
When UID has a register content to send to the microprocessor, it pulls low the $\overline{INT}$ output to request $\overline{CS}$ and CCLK signals. Note that the data to send can be the content of a Register previously requested by the microprocessor by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1 if read back
forced to 0 if spontaneous
D7-D0: Register Content

Digital System Interface
Two B channels, each at 64 kbit/s and one D channel at 16 kbit/s form the Basic access data. Basic access data is transferred on the Digital System Interface with several different formats selectable by means of the configuration register CRI.
The DSI is basically constituted of 5 wires (see fig.2 and 3):

BCLK bit clock
Bx data input to transmit to the line
Br data output received from the line
FSa Transmit Frame sync
FSb Receive Frame sync

It is possible to separate the D channel from the B channels and to transfer it on a separate Digital Interface constituted of 2 pins:

Dx D channel data input
Dr D channel data ouput

The multiplexed mode uses the same bit and frame clocks as for the B channels. The continuous mode

uses an internally generated 16 kHz bit clock output:

DCLK D channel clock output.

ST5410 provides a choice of four multiplexed formats for the B and D channels data as shown in fig.2 and 3.

Format 1: the 2B+D data transfer is assigned to the first 18 bits of the frame on Br and Bx I/0 pins. Channels are assigned as follows: B1(8 bits), B2(8 bits), D(2 bits), with the remaining bits ignored until the next Frame sync pulse.

Format 2: the 2B+D data transfer is assigned to the first 19 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows: B1(8 bits), D(1 bit), 1 bit ignored, B2(8 bits), D(1 bit), with the remaining bits ignored until the next frame sync pulse.

Format 3: B1 and B2 Channels can be independently assigned to any 8 bits wide time slot among 64 (or less) on the Bx and Br pins. The transmit and receive directions are also independent. When multiplexed mode is selected, the D channel can be assigned to any 2 bits wide time slot among 256 on the Bx and Br pins or on the Dx and Dr pins (D port disabled or enabled in multiplexed mode continuous respectively).

Format 4: is a GCI like format excluding Monitor channel and C/I channel. The 2B+D data transfer is assigned to the first 26 bits of the frame on Br and Bx I/O pins. Channels are assigned as follows. B1(8 bits) B2(8 bits), 8 bits ignored, D(2 bits), with remaining bits ignored up to the next frame sync pulse.

For all formats when D channel part is enabled "continuous mode" is possible. When the D channel port is enabled in multiplexed mode, only the 2 B channels use the Bx and Br pins. D bits are assigned according to the related format.

When the Digital Interface clocks are selected as inputs, FSa must be a 8 kHz clock input which indicates the start of the frame on the data input pin Bx. When the Digital Interface clocks are selected ae outputs, FSa is an 8 kHz output pulse conforming to the selected format which indicates the frame beginning for both Tx and Rx directions.

When the Digital Interface clocks are selected as inputs, FSb is a 8 kHz clock input which defines the start of the frame on the data ouput pin Br. When the Digital Interface clocks are selected as outputs, FSb is a 8 kHz output pulse indicating the second 64Kbit slot.

Two phase-relations between the rising edge of FSa/FSb and the first (or second for FSb as output) slot of the frame can be selected depending on format selected: Delayed timing mode or non Delayed timing mode.

Non delayed data mode is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa is coincident with the first 8 bits wide time-slot while FSb is coincident with the second 8 bits wide time-slot. Non delayed mode is not available in format 2.

Delayed timing mode, which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, Fsa (1bit wide pulse) indicates the first 8 bits time-slot beginning while FSb indicates the second. Delayed mode is not available in format 4.

2B+D basic access data to transmit to the line can be shifted in at the BCLX frequency on the falling edges during the assigned time-slots. When D channel port is enabled, only B1 & B2 data is shifted in during the assigned time slots. In format 4, data is shifted in at half the BCLK frequency on the receive falling edges.

2B+ D basic access data received from the line can be shifted out from the Br output at the BCLK frequency on the rising edges during the assigned time-slots. Elsewhere, Br is in the high impedance state. When the D channel port is enabled, only B1 & B2 data is shifted out from Br. In Format 4, data is shifted out at half the BCLK frequency on the transmit rising edges; there is 1.5 period delay between the rising transmit edge and the receive falling edge of BCLK.

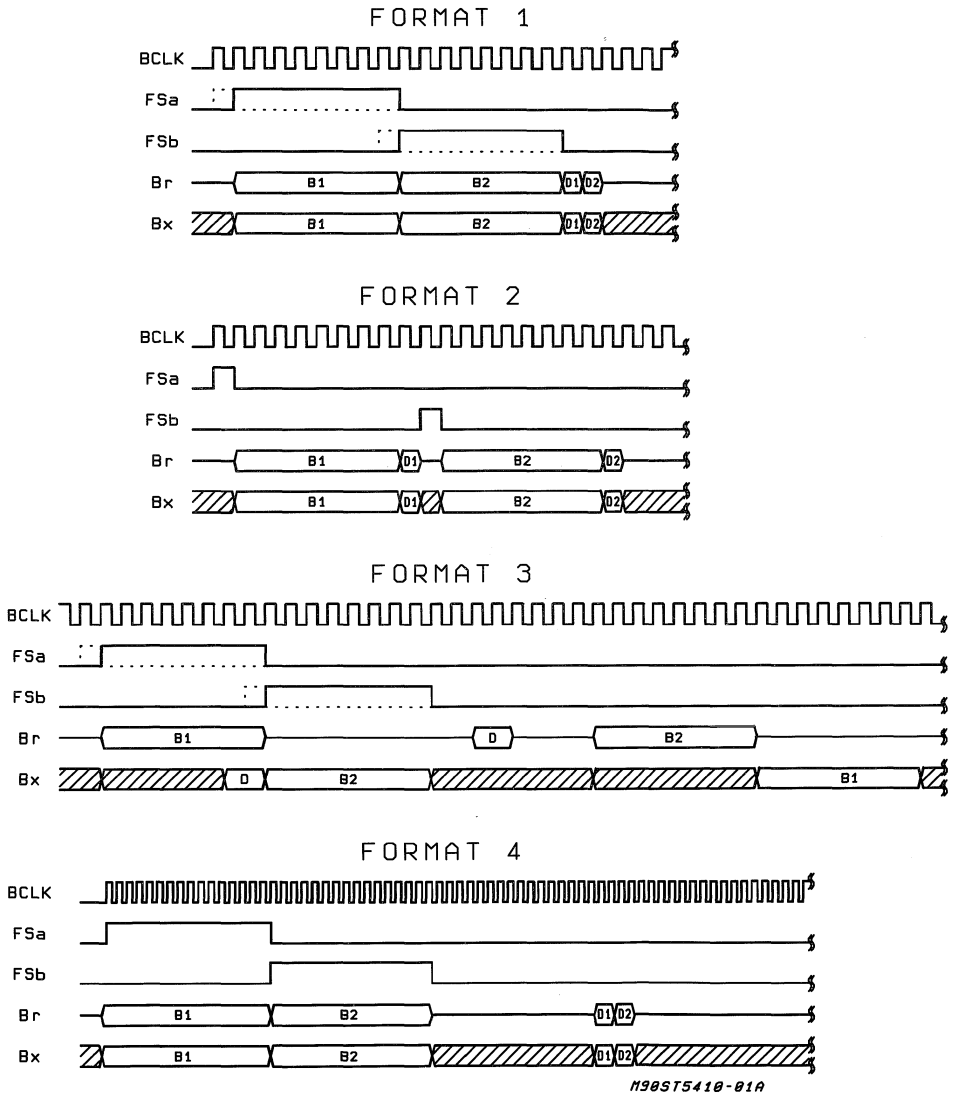
Bit Clock BCLK determines the data shift rate on the Digital Interface. Depending on mode selected, BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 6176 kHz or an output at a frequency depending on the format and the frequency selected. Possible frequencies are:

256 KHz, 512 KHz, 1536 KHz,
2048 KHz, 2560 KHz.

In format 4 the use of 256kHz is forbidden.

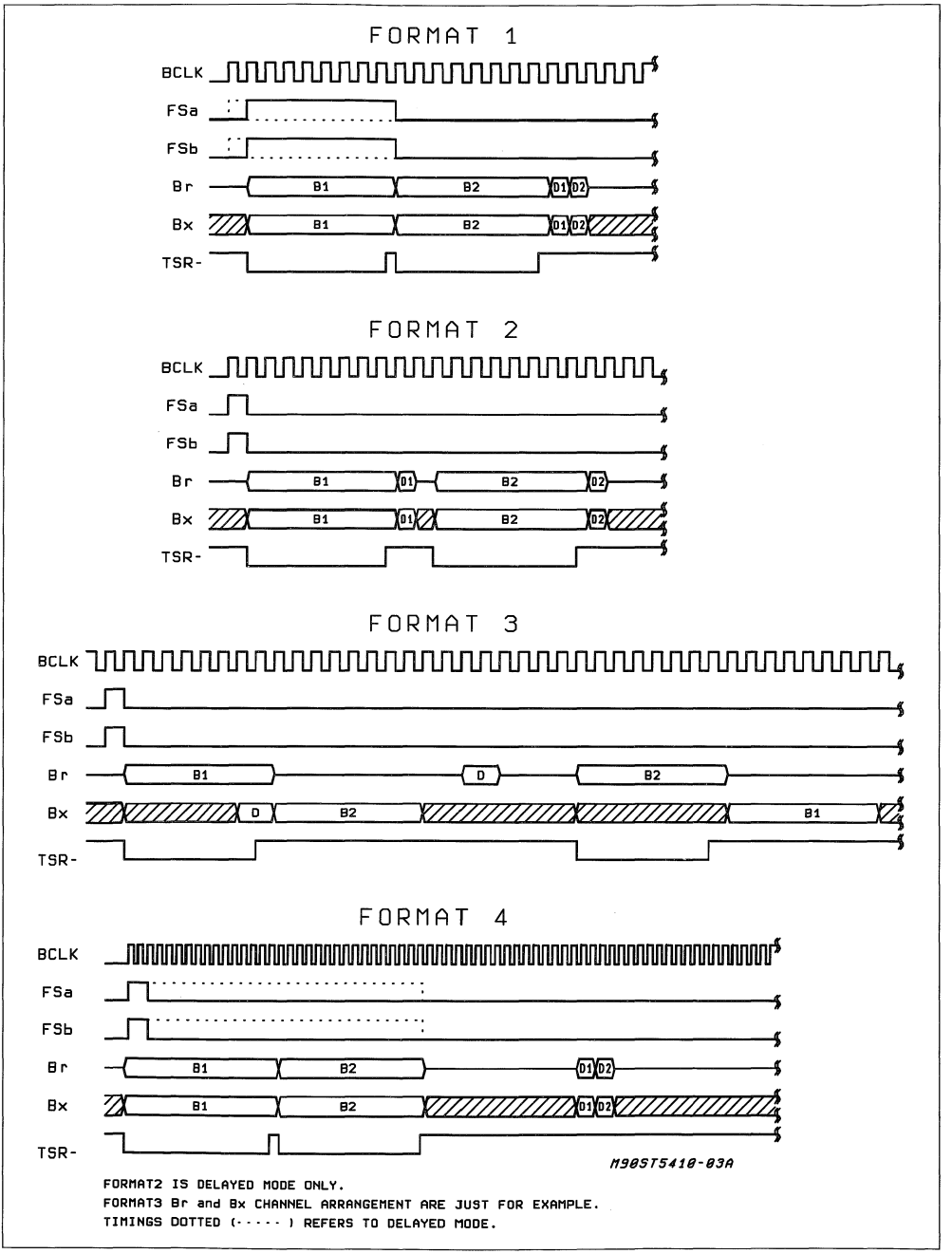
BCLK is synchronous with FSa/b frame sync signal. When output, BCLK is phased locked to the recovered clock received from the line.

Figure 2: DSI interface formats: MASTER mode.



FORMAT2 IS DELAYED MODE ONLY.
FORMAT3 Br and Bx CHANNEL ARRANGEMENT ARE JUST FOR EXAMPLE.
TIMINGS DOTTED (·····) REFERS TO DELAYED MODE.

Figure 3: DSI interface formats: SLAVE mode.



GCI MODE

The GCI is a standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop :
In a Terminal, GCI interlinks the S interface transceiver, the ISDN layer 2 (LAPD) controller and the voice/data processing components as an audio-processor or a Terminal Adaptor module.

In NT1-2, PABX subscriber line card, or central office line card (LT), GCI interlinks the UID, the ISDN Layer 2 (LAPD) controllers and eventually the backplane where the channels are multiplexed.

Frame Structure

2B+D data and control interface is transferred in a time-division multiplexed mode based on 8 kHz frame structure and assigned to four octets per frame and direction.(see fig.4a).
The 64 kbit/s channels B1 and B2 are conveyed in the first two octets; the third octet (M: Monitor) is used for transferring most of the control and status registers; the fourth octet (SC: Signalling & Control) contains the two D channel bits, the four C/I (command/Indicate) bits controlling the activation/deactivation procedures, and the E & A bits which support the handling of the Monitor channel.
These four octets per frame serving one ISDN

Figure 4a: GCI interface format.

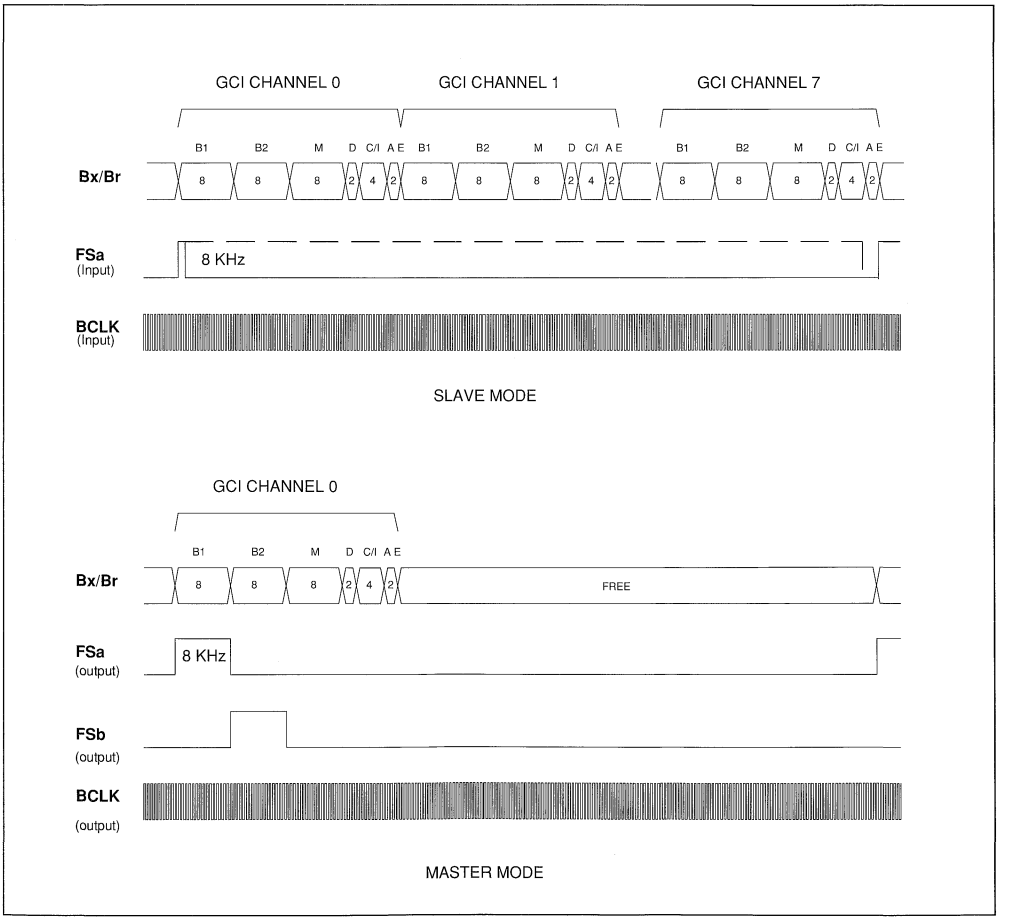
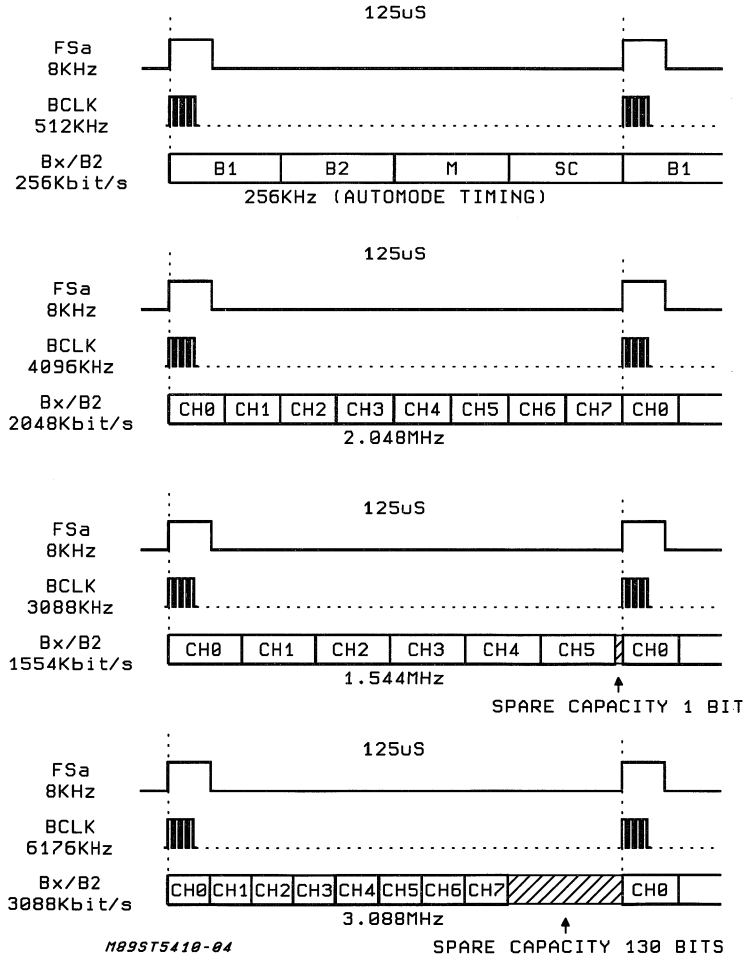


Figure 4b: GCI Multiplex Examples.



subscribers line form a GCI Channel. One GCI channel calls for a bit rate of 256 kbit/s.

In NT1-2s or subscriber Line Cards up to 8 GCI channels may be carried in a frame of a GCI multiplex. The bit rate of a GCI multiplex may be from 256 kbit/s and up to 3088 kbit/s. Adjacent 4-octet slots from the frame start are numbered 0 to 7. The GCI channel takes the number of the slot it occupies. Spare bits in the frame beyond 256 bits from the frame start will be ignored by GCI compatible devices but may be used for other purposes if required (see Fig.4b). GCI channel number is selected by biasing pins S0,S1,S2.

Physical Links.

Four physical links are used in the GCI.

Transmitted data to the line: Bx
Received data from the line: Br
Data clock: BCLK
Frame Synchronization clock: FSa

GCI is always synchronized by frame and data clocks derived by any master clock source. These two clock signals are provided to each component linked by GCI.

A device used in NT mode can deliver clock sources able to synchronize GCI, either directly, or via a local Clock Generator synchronized on the line by means of the MCLK 15.36 MHz output clock.Frame clock and data clock could be independent of the internal devices clocks. Logical one on the Br output is the high impedance state while logical zero is low voltage. For E and A bits, active state is voltage Low while inactive state is high impedance state.

Data is transmitted in both directions at half the data clock rate. The information is clocked by the transmitter on the front edge of the data clock and can be accepted by the receiver after 1 to 1.5 period of the data clock.

The data clock (BCLK) is a square wave signal at twice the data transmission frequency on Bx and Br with a 1 to 1 duty cycle. The frequency can be choosen from 512 to 4096 kHz with 16 kHz modularity. Data transmission rate depends only on the data clock rate.

The Frame Clock is a 8 kHz signal for synchronization of data transmission. The front edge of this signal gives the time reference of the first bit in the first GCI input and output channel, and reset the slot counter at the start of each frame

When some GCI channels are not selected on devices connected to the same GCI link, these time slots are free for alternative uses.

GCI configuration select is done by bias of input pins according to TABLE 1.

Table 1: GCI Configuration selection.

Pin name	TE/NT1	NT12/LT*
MW	0	0
M0	1	0
S2/CLS	CLS = 0: 512 KHz CLS = 1: 1536 KHz	S2
S0/FSb	FSb	S0
S1/AUTOE	AUTOE	S1

* Differentiation between NT and LT mode is done by configuration register 2 (NTS bit)

Monitor channel

The Monitor channel is used to write and read all ST5410 internal registers. Protocol on the Monitor channel allows a bidirectional transfer of bytes between UID and a control unit with acknowledgement at each received byte. Bytes are transmitted on the Br output and received on the Bx input in the Monitor channel slot.
A write or read cycle is always constituted of two bytes.(see fig. 5)

Note: Special format is used for EOC channel.

Write cycle

The format to write a message into the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Address
A0: Write/Read Indicator set low
D7-D0: Register Content

After the first byte is shifted in, Register address is decoded. A0 set low indicates a write cycle: the content of the following received byte has to be loaded into the addressed register.

A0 set high indicates a read-back cycle request. the second byte content is not significative. ST5410 will respond to the request by sending back a message with the register content associated with its own address. It is than possible for the micro to receive the required register content after several other pending messages.

Read cycle

When UID has a register content to send to the controller, it send it on the monitor channel directly. Note that the data to send can be the content of a Register previously requested by the controller by means of a read-back request.

The format of the message sent by the UID is:

A7	A6	A5	A4	A3	A2	A1	A0

1st byte

D7	D6	D5	D4	D3	D2	D1	D0

2nd byte

A7-A1: Register Adress
A0: forced to 1
D7-D0: Register Content

Exchange Protocol

ST5410 validates a received byte if it is detected two consecutive times identical. (see fig. 5)

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses A bit to acknowledge the received byte.When no message is transferred, E bit and A bit are forced to inactive state.

A transmission is started by the sender (Transmit section of the Monitor channel protocol handler) by putting the E bit from inactive to active state and by sending the first byte on Monitor channel in the same frame. Transmission of a message is allowed only if A bit sent from the receiver has been set inactive for at least two consecutive frames.

When the receiver is ready, it validates the incoming byte when received identical in two consecutive frames. Then, the receiver set A bit from the inactive to the active state (preacknowledgement) and maintain active at least in the following frame (acknowledgement).

If validation is not possible (two last bytes received are not identical) the receiver aborts the message by setting the A bit active for only a single frame.

The second byte can be transmitted by the sender putting the E bit from the active to the inactive state and sending the second byte on the Monitor channel in the same frame . The E bit is set inactive for only one frame.

If it remains inactive more than one frame, it is an end of message.

The second byte may be transmitted only after receiving of the pre-acknowledgement of the previous byte . Each byte has to be transmitted at least in two consecutive frames.

The receiver validates the current received byte as for the first one and then set the A bit in the next two frames first from the active state to the inactive state (pre-acknowledgement) and back to the active (acknowledgement). If the receiver cannot validates the received current byte (two bytes received not identical)it pre-acknowledges normally but let the A bit in the inactive state in the next frame which indicates an abort request .

If a message sent by the UID is aborted, the UID will send again the complete message until receiving of an acknowledgement .

A message received by the UID can be acknowledged or aborted with flow Control.

The most significant bit (MSB) of Monitor byte is sent first on the Monitor channel. E & A bits are active low and inactive state on DOUT is 5 V. When no byte is transmitted, Monitor channel slot on Br is in the high impedance state.

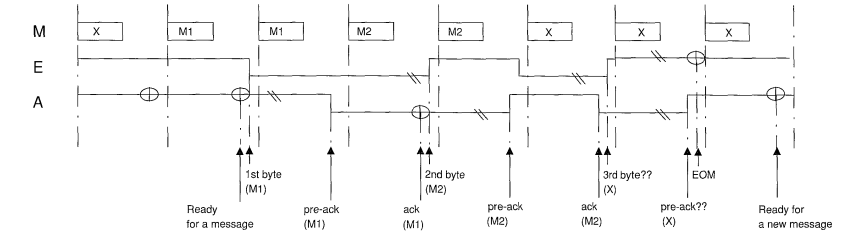
C/I channel

The C/I channel is used to load the Activation Control Register and to read the Activation Indication Register.

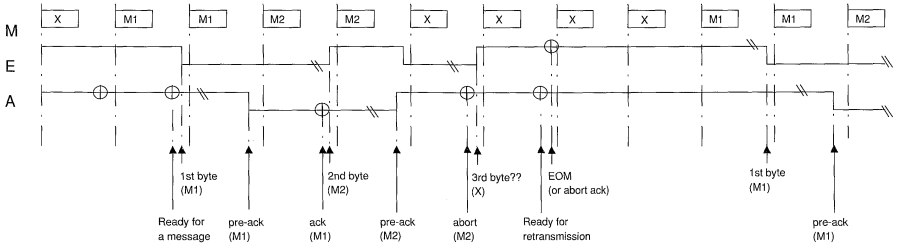
A four bits code (C1, C2, C3, C4) is transmitted on the Br output in the C/I channel of the GCI channel. The code is sent permanently at a 8 kHz frequency as long as the content the transmitted register remains unchanged. C1 bit is transmitted first.

A four bits code (C1, C2, C3, C4) is received on the Bx input in the C/I channel of the GCI channel . A change in the receive C/I channel code is validated if it has been received identical in two consecutive frames.

Figure 5: GCI Monitor channel messaging examples.



TWO BYTES MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE ABORTED ON THE SECOND AND RETRANSMITTED

E & A BITS TIMING

TURNING ON AND OFF THE DEVICE

ST5410 contains an automatic sequencer for the complete control of the start-up activation sequences specified by the ANSI and French specifications. Interactions with an external control unit requires only Activate Request and Deactivate Request commands, with the option of inserting breakpoints. Automatic control of act and dea bits in the M4 bit positions is provided, along with the specified 40 ms, 480 ms and 15 s timers used during the sequencing.

By default, during ACT procedure, the 15s timer is enabled, to force the device to abandon the sequence where the time limit is reached.

Except the Power up and Power down control that is slightly different, the Activation/Deactivation procedures are identical in GCI and Microwire modes. Same command codes or indication codes are used. In Microwire mode, Activation Control is done by writing in the Activation Control Register ACT. In GCI mode, these registers are accessed directly by the Command/Indicate channels.

Power on initialization

Following the initial application of power, ST5410 enters the power down deactivated state in MICROWIRE mode or in GCI mode depending on the polarization of the MW input.
All the internal circuits including the master oscillator are inactive and in a low power state except for the 10 kHz Tone signal detector. The line outputs LO+/LO- are low impedance and all digital outputs are high impedance. All programmable registers and the activation controller are reset to their default value.

In µW/DSI mode, configuration programming has to be completed before a power up instruction.

In GCI mode, GCI configuration is done by means of pins polarization and register programming.
In NT1 and TE equipments, GCI configuration is defined fully by means of the configuration pins M0, and CLS at Power On Reset.
For LT and NT1-2 equipments, GCI configuration is first defined by means of the configuration pins M0, S2, S1, S0 and must be completed by means of Control Register Programming prior the Power Up instruction.

Power up control

µW/DSI: control instruction PUP in ACT register is required to power up the UID.

GCI: when in TE/NT1 mode (M0=1), the UID provides the GCI clocks needed for control channel transfer; PUP control instruction is provided to the UID by pulling low the Bx data input; ST5410 then reacts sending GCI clocks. It is possible to operate an automatic power up of the UID when a wake up tone is detected from the line by connecting the $\overline{LSD}$ output directly to the Bx input.

GCI: when in LT/NT12 mode (M0=0), the UID powers up after that PUP code (0000) on C/I Control Channel has been sent.

When UID is in the power down state and a 10 kHz tone TN or TL is detected from the line, $\overline{LSD}$ and $\overline{INT}$(µW/DSI only) open drain outputs are forced to zero.

In NT configuration, code LSD (0000) is loaded in the activation indication register RXACT.

In LT configuration, code AP (1000) is loaded in the activation indication register.
In µW/DSI these indications are sent onto CO at the following access even if the UID is still in power down mode.
In GCI, these indications are sent onto the C/I channel as soon as GCI clocks are available.

$\overline{LSD}$ open drain output is set back in the high impedance state as soon as the UID is powered up.

$\overline{INT}$ open drain output is set back in the high impedance state when the $\overline{CS}$ input is detected at zero.

Power up transition enables all analog and digital circuitry, starts the Crystal oscillator and internal clocks. The LSD output is in the high impedance state even if a tone is detected from the line. As for the PDN instruction, PUP has no influence on the content of the internal registers.

Power down control

A control instruction PDN in ACT register is required to power down the device after a period of activity. PDN forces directly the device to the low power state. It should therefore only be used after the UID has been put in the line deactivated state. PDN has no influence on the content of the internal registers, but immediately stops the output clocks when UID is in master mode.

When line is fully deactivated DI code put UID in power down. UID waits for 2 frames (250µs) before entering power down state. During this time on GCI bus the code DI (1111) is sent an C/I. The clocks are stopped as soon as UID is in power down. The DI command is recommended in GCI mode.

Configuration Registers remain in their current state and can be changed either by the µW control interface or the CGI Monitor channel (if M0 = 0 only) depending on mode selected. It is then possible, for instance, after a normal deactivation procedure followed by a power down command, to power up again the device in order to operate directly a Warm Start procedure. In Power Down mode low impedance (with Typical value of 12Ω) between Li+ and Li- is ensured to maintain adaptation to the line impedance.

Software Reset

When the device is either powered-up or down, a control instruction RES resets the activation controller ready for a cold start. That feature can be used if the far-end equipment fails to warm start, for example if the line card or NT has been replaced or if in a regenerator, the loss of synchronisation of the second section imply the reset of the first section for a further cold start. The configuration registers remain in their selected value.

COMMAND/INDICATION (C/I) CODING

The Command/Indication codes are given in Table 2. For each mode a list of recognized Control codes and generated Indicate codes is given. Here after you have a detailed description depending on mode selected.

The C/I codes can be used:

a) in GCI mode, according to the already described rules.

b) in µW/DSI, using the register ACT described in chapter 'Internal register description'

NT mode: Control.

0000 (PUP) Power Up Request.
In GCI configuration with clocks selected as outputs, when UID is in Power down state, Power Up request is done by pulling low the Bx data input; UID reacts sending GCI clocks; code PUP enters no other change. In the other configurations, the PUP instruction powers up the device.

0001 (RES) RESET.
This code resets UID for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (EI) Error Indication.
EI code indicates that a transmission error has been detected on the TE side of the loop relative to UID. act bit is forced to 0 in the SN3 signal transmitted to the line.

0101 (PDN) Power Down Request.
PDN instruction forces the device to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an NT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line by sending TN and SN1.

1100 (AI) Activation Indication.
The AI code indicates that TE side of the loop relative to UID has been activated. act bit is sent equal 1 in the SN3 signal transmitted to the line.

1111 (DI) Deactivation Indication. (GCI only)
The DI instruction allows the UID to automatically enter the Power down state if the line is deactivated. When the line is not deactivated, DI has no effect.

NT mode : Indication.

0000 (DR/LSD) Deactivation Request.
When in the deactivated state either powered up or down, the LSD code is sent if a 10 kHz wake-up tone is detected. If the device is powered down, the $\overline{\text{LSD}}$ pin is also pulled low.
When in activated state, DR code indicates that network has decided to deactivate the line. dea bit has been received equal 0. UID enters the normal deactivate state waiting for a further Warm Start.

0100 (EI) Error Indication.
The EI code indicates that a transmission error has been detected on the loop for more than 480 ms (loss of synchro or loss of signal). UID enters the receive RESET state. EI also indicate that act bit has been received equal 0, or that 15sec timer has expired.

TABLE 2: C/I channel codes.

CODE	TE/NT1/NT12		LT	
C1C2C3C4	Ind	Com	Ind	Com
0000	DR/LSD	PUP	TIM*	PUP/DR
0001	—	RES	—	RES
0100	EI	EI	EI	FAO
0101	—	PDN	—	PDN
0110	—	—	SYNC	—
1000	AP	AR	AP	AR
1100	AI	AI	AI	AI
1111	DI	DI	DI	DI

(*) GCI code only for power up/power down control.

1000 (AP) Activation Pending.
Indicates that the network has decided to activate the loop. SL2/SL3 signal is received with the act bit set to 0.

1100 (AI) Activation Indication.
AI code indicates that network side of the loop relative to UID is activated. SL3 signal is received with the act bit equal 1.

1111 (DI) Deactivation Indication.The DI code indicates that the UID has entered the deactivated state H1.

LT mode: Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in the Power down state, the PUP code powers up the UID. When in the Power Up state, the DR code forces the UID through the appropriate deactivation sequence where the dea bit is set to 0 in four consecutive superframes before ceasing transmission.

0001 (RES) RESET.
This code resets the UID ready for a cold start. Configuration registers remain in their current value. Can be operated with the device either powered up or down.

0100 (FAO) Force act bit to 0.
The act bit is forced to 0 in the SL3 signal transmitted to the line. Is intended to reflect either a transmission error detected on the network side of the loop relative to UID or to acknowledge receiving of an act bit set to 0 from the line.

0101 (PDN) Power Down Request.
PDN instruction forces ST5410 to Power down state. It should normally only be used in µW/DSI mode after the ST5410 has been put in a known state, e.g. in an LT after a DI status indication has been reported.

1000 (AR) Activation Request.
Being in inactive Power Up state, AR instruction forces UID through the appropriate sequence to activate the line.

1100 (AI) Activation Indication.
The AI code is an optional command recognised only when the second break point BP2 is enabled giving the authorization to set the act bit equal one

1111 (DI) Deactivation Indication.
When line is fully deactivated the DI command allows UID to enter power down state. DI is recommended in GCI mode.

LT mode: Indication.

0000 (TIM) Timing required (GCI only)
The TIM code acnowledges PUP command in the case where the UID was previously in the Power Down state.

0100 (EI) Error Indication.
EI code indicates that a transmission error or a act bit equal zero has been received on the loop. In the first case, UID will enter automatically RESET state waiting for a further Cold Start and a DI primitive will be sent. EI also indicate that act bit has been received equal 0, UID being in the activate state.

0110 (SYNC) Synchronization Indication.
SYNC code is sent to indicate that ST5410 is superframe synchronized.

1000 (AP) Activation Pending.
AP code indicates that TE side is attempting to activate the loop. UID waits AR command to send SL1.

1100 (AI) Activation Indication.
The AI code indicates that the UID has received SN3 signal with act bit set to one. That means that the TE side of the loop relative to the UID is activated.

1111 (DI) Deactivation Indication.
The DI code indicates that the UID has entered the Deactivated state .

Activation/deactivation sequencing
Activation/deactivation signals onto the line are in accordance with the activation/deactivation state matrix given in Appendix A.
The startup procedures are in accordance with the T1.601-1988 and ST/LAA/ELR/822 procedures. All the timers defined in the standard are on chip. It is possible in any case to disable the 15sec timer replacing it with an external soft timing.
Refer to T1.601-1988 document for standard procedures description.

Table 3.

INTERNAL REGISTERS																
COMMAND REGISTERS																
FUNCTION		**BYTE 1**								**BYTE 2**						
		7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
No Operation (NOP)		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR	W	0	0	1	0	0	0	0	0	CIE	EIE	FIE	OB1	OB0	OC1	OC0	0
	R	0	0	1	0	0	0	0	1	X	X	X	X	X	X	X	X
CR1	W	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
	R	0	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X
CR2	W	0	0	1	0	0	1	0	0	SFS	NTS	DMO	DEN	DD	0	BP2	0
	R	0	0	1	0	0	1	0	1	X	X	X	X	X	X	X	X
CR3	W	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
	R	0	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X
TXB1 TSA	W	0	0	1	1	0	0	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	0	1	X	X	X	X	X	X	X	X
TXB2 TSA	W	0	0	1	1	0	0	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X
RXB1 TSA	W	0	0	1	1	0	1	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X
RXB2 TSA	W	0	0	1	1	0	1	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
	R	0	0	1	1	0	1	1	1	X	X	X	X	X	X	X	X
TXD	W	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
	R	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X
RXD	W	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
	R	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X
TXM4	W	0	1	0	0	0	0	0	0	ACT	M42	M43	M44	M45	M46	M47	M48
TXM56	W	0	1	0	0	0	0	1	0	0	0	LEC	M51	M61	M52	FEB	CTC
ACT Register	W	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
EC01	W	0	1	0	0	0	1	1	0	07	06	05	04	03	02	01	00
BEC1	R	0	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X
Tx EOC Register	W	0	1	0	1	E	F	G	H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: bit 7 of byte 1 is always the first bit clocked into the device.
Note 2: In the Tx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address;
H = dm, the EOC data/message mode indicator.

Note 3: X= don't care (it is recommended that these bits be set = 0).

Note 4: M42 in TXM4 only significant in LT mode.

Table 3: (continued)

STATUS REGISTERS											
FUNCTION	**BYTE 1**								**BYTE 2**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
READABLE CONFIGURATION REGISTERS																
Default (No Change on a Write cycle)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR Contents	0	0	1	0	0	0	0	0	NBE	ECE	FBE	OB1	OB0	OC1	OC0	0
CR1 Contents	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CLK	BEX
CR2 Contents	0	0	1	0	0	1	0	0	SFS	NTS	DMO	DEN	DD	BP1	BP2	0
CR3 Contents	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
TXB1 Contents	0	0	1	1	0	0	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
TXB2 Contents	0	0	1	1	0	0	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB1 Contents	0	0	1	1	0	1	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB2 Contents	0	0	1	1	0	1	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
TXD Contents	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD Contents	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
REGISTERS WHICH GENERATE SPONTANEOUS INTERRUPTS (NOTE 2)																
RXM4	0	1	0	0	0	0	0	0	M41	M42	M43	M44	M45	M46	M47	M48
RXM56 Spare Bits	0	1	0	0	0	0	1	0	0	ES2	ES1	M51	M61	M52	feb	neb
ACT Indication Reg	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
BEC1 (Note 3)	0	1	0	0	0	1	1	0	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
Rx EOC Register (Note 4)	0	1	0	1	E	F	G	H	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: bit 7 of byte 1 is always the first bit clocked out from the device.

Note 2: All these Registers, with the exception of the EOC Register, set bit 0 of byte 1 as follows: bit 0=0 when the register is read in response to an Interrupt; bit 0=1 when reading back the register in response to a readback command.

Note 3: BEC1 may be polled, via the appropriate read command (see Table 1), at any time to read the current error count. When reading in response to a spontaneous interrupt, the data byte is always X'00.

Note 4: In the Rx EOC Register:
E = ea1, the msb of the EOC destination address;
F = ea2, bit 2 of the EOC destination address;
G = ea3, the lsb of the EOC destination address;

Note 5: ES1, ES2 (RXM56) not significant in µW mode.

INTERNAL REGISTERS DESCRIPTION.

Here following a detailed description of ST5410 internal registers.

Internal registers can be accessed:

a) In GCI mode, according to the monitor channel exchange rules.

b) in µW/DSI mode, using the MICROWIRE interface according to the rules described in section "µW control interface".

By default:
1) When not stated the registers are read-write.
2) Superframe formats (according to AN51 Std) are reported in table 2 and 3.

Overhead bits programmable register (OPR)

After reset: 00H

CIE	EIE	FIE	OB1	OB0	OC1	OC0	0

CIE Near-End CRC Interrupt Enable:

CIE = 1: the RXM56 register is queued in the interrupt register stack with nebe bit set to zero each time the CRC result is not identical to the corresponding CRC received from the line. If in two or more consecutive superframes, an error is detected, two or more interrupt cycles are issued.

CIE = 0: no interrupt is issued but the error detection remains active for instance for on chip error counting.

EIE Error counting Interrupt Enable:

EIE = 1: an interrupt is provided for the counter which goes in overflow (FF).

EIE= 0: no interrupt is issued. It is feasible to read the counters even if no relevant interrupt has been provided.

FIE FEBE Interrupt Enable:

FIE = 1: the RXM56 register is queued into the interrupt register stack each time the febe bit is received at zero in a superframe. If in two or more consecutive superframes, febe bit is received equal zero, two or more interrupt cycles are issued.

FIE = 0: no interrupt is issued but the receive febe bit remains active for on chip error counting

OB1, OB0 Overhead Bit processing:
select how each spare overhead bit received from the line is validated and transmitted to the system. RXM4 and RXM56 registers are independently provided onto the system interface as for the eoc channel. Spare overhead bits are validated independently.

OB1	OB0	
0	0	each super frame, a signal is generated for the RXM4 or the RXM56 register. Spare bits are transparently transmited to the system.
0	1	a signal is set at each new spare overhead Bits received.
1	0	a signal is set at each new spare overhead Bits received and confirmed once. (two times identical).
1	1	a signal is set at each new spare overhead Bits received and confirmed twice. (three times identical).

If new bits are received at the same time in M4 and M56, both registers RXM4 and RXM56 are queued in the interrupt register stack.
Bits act, dea are dedicated to the activation procedure. Validation is always done in accordance with the ANSI rule: validation at each new activation bit received and confirmed twice independently from the above rules. These bits are taken into account directly by the activation decoder. An interrupt is not generated for the RM4 Register when one of these bits changes.

OC1, OC0 eoc channel processing:
select how a received eoc message is validated and transmitted to the system.
The eoc message is signaled:
- in µW/DSI mode: on the control interface by an interrupt
- in GCI mode: on the Monitor channel.

OC1	OC0	
0	0	every half a super frame, a signal is generated for the RXEOC register. eoc channel is transparently transmitted to the system.
0	1	a signal is set at each new eoc message received.
1	0	a signal is set at each new eoc message received and confirmed once. (two times identical)
1	1	a signal is set at each new eoc message received and confirmed twice. (three times identical).

Configuration register 1 (CR1)

FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

FF1, FF0 Frame Format Selection:
Refer to fig.1.

FF1	FF0	
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4

CK0-CK2 Digital Interface Clock select:
CK0-CK2 bits select the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK frequency:
0	0	0	256KHz
0	0	1	512KHz
0	1	0	1536KHz
0	1	1	2048KHz
1	X	X	2560KHz

DDM Delayed Data Mode select:
Two different phase-relations may be establish between the Frame Sync input and the first bit of the frame on the Digital Interface:

DDM = 0: Non delayed data mode (not available in Format 2) is similar to long frame timing on the COMBOI/II series of devices: The first bit of the frame begins nominally coincident with the rising edge of FSa/b. When output, FSa starts with the first 8 bits wide time-slot while FSb with the second 8 bits wide time-slot.

DDM = 1: delayed data mode (not available in Format 4): which is similar to short frame sync timing on COMBO I/II, in which the FSa/b input must be set high at least a half cycle of BCLK earlier the frame beginning. When output, FSa pulse indicates the first 8 bits wide time-slot while FSb indicates the second.

CMS Clocks Master Select:

CMS = 0: BCLK, FSa and FSb are inputs; BCLK can have in Format 1, 2 and 3 value between 256KHz to 4048KHz, value in Format 4: 512KHz to 6176KHz.

CMS = 1: BCLK, FSa and FSb are outputs; FSa is a 8 kHz clock pulse indicating the frame beginning, FSb is a 8 kHz clock pulse is indicating the second time-slot. BCLK is a bit clock signal whose frequency bits CK2-CK0.

BEX B channels Exchange:

BEX = 0: B1 and B2 Tx/Rx channels are associatedwith B1 and B2 registers respectively.

BEX = 1: B1 and B2 channels are exchanged.

Configuration register 2 (CR2)

SFS	NTS	DMO	DEN	DD	0	BP2	-

SFS Super Frame Synchronization Select:
Significant in LT mode only.

SFS = 0: SFS is an input that synchronizes the transmit frame counter of ths GSC board (timing to be precised).

SFS = 1: SFS is an output issued from the free-running Transmit Frame counter of the GSC board. in NT mode SFS is always an output.

NTS LT / NT mode Select.

NTS = 0: LT mode selected

NTS = 1: NT (NT1, NT2, TE) mode selected

DMO D channel Transfer mode Select.
Significant only when DEN=1.

DMO = 1: D channel data is shifted in and out on Dx and Dr pins in continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively.

DMO = 0: D channel data is shifted in and out on Dx and Dr pins in a multiplexed mode at the BCLK frequency on the falling and rising edges of BCLK respectively when the assigned time-slots are active.

DEN D channel port Enable.

DEN = 0: D channel port disabled. D bits are transferred on Br and Bx; Multiplexed mode is selected automatically. Test port (TA, TD, TCLK) is selected and may be activated by a Test instruction.

DEN = 1: The D channel port (DX, DR, DCLK) is selected. D bits are transferred on Dr and Dxin a mode depending on DMO bit setting. Test port is disabled.

DD 2B+D Data channel Disable.

DD = 0: 2B+D channel transfer is enabled as soon as the line is completly synchronized.

DD = 1: 2B+D channel transfer is idle; 2B+D bits transmitted to the line are ones or zero depending on configuration respectively selected. 2B+D bits on the Digital Interface are in

the high impedance state. A second level of transparency control is provided for each channel independently from the others when format 3 is selected. See bits EB1, ED and EB2 in TXB1 and TXB2 configuration registers.

BP2 Break Points.
Significant only when NTS=0 (LT selected).

BP2 = 1: a break point in the activation sequencer is enabled after the UID has detected that NT was activatsd avoiding automatic response by act bit = 1.

BP2 = 0: the break point is disabled allowing automatic activation sequencing.

Configuration register 3 (CR3)
After reset: 00H

LB1	LB2	LBD	DB1	DB2	DBD	TLB	-

LB1, LB2, LBD Line side Loopback select.
When set high they turn each individual B1, B2, or D channel from the Line receive input to the Line transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if the D port is selected).

DB1, DB2, DBD Digital side Channel Loopback select.
When set high they turn each individual B1, B2, or D channel from the Digital Interface receive input to the Digital Interface transmit output. They may be set separately or together. The loopback is operated close to Bx and Br (or Dx and Dr if D port selected).

TLB Transparent Loopback select

TLB = 0: loopback are non transparent when line side loopback is set, data transmitted onto the digital interface is forced to one. When digital side loopback is set data transmitted onto the line is forced to one or zero depending on NT or LT configuration respectively.

TLB = 1: 2B+D is transparently transferred through the UID.

Configuration register TXB1
Significant only when format 3 selected.
After reset: 00H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B1 Time Slot Assignment
Those bits define the binary number of the transmit B1 channel time-slot on Bx input. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXB2
Register significant only when format 3 selected.
After reset: 01H

-	-	TS5	TS4	TS3	TS2	TS1	TS0

TS5-TS0 Transmit B2 Time Slot Assignment
Those bits define the binary number of the transmit B2 channel time-slot on Bx input. Time slots are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB1
Register significant only when format 3 selected.
After reset: 00H

EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0

EB1 B1 channel transparency

EB1= 1: B1 channel transparency enabled.

EB1= 0: B1 channel transmitted forced to one or zero depending on NT or LT configuration and forced the selected B1 channel time slot on Br output in the high impedance state.

ED D channel transparency enabling

ED = 1: enables the D channel transparency.

ED = 0: forces the D channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected D channel time slot on Br or Dr output in the high impedance state

TS5-TS0 Receive B1 Time Slot Assignment
TS5-TS0 bits define the binary number of the receive B1 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register RXB2
Register significant only when format 3 selected.
After reset: 01H

EB2	-	TS5	TS4	TS3	TS2	TS1	TS0

EB2 B2 channel transparency
EB2 = 1: enables the B2 channel transparency.
EB2 = 0: forces the B2 channel transmitted onto the line to one or zero depending on NT or LT configuration respectively and forces the selected B2 channel time slot on Br output in the high impedance state.

TS5-TS0 Receive B2 Time Slot Assignment
Those bits define the binary number of the receive B2 channel time-slot on BR output. Time slot are numbered from 0 to 63. The register content is taken into account at each frame beginning.

Configuration register TXD
Significant only when format 3 is selected with the D channel Digital interface selected in the multiplexed mode:
After reset: 0CH in GCI
08H in µW/DSI

DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

DX5-SX0 Transmit D channel Time Slot Assignment
DX5-DX0 and SX1-SX0 bits define the binary number of the transmit D channel time-slot. DX5-DX0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot, SX1,SX0 bits define the binary numbar of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Configuration register RXD
Significant only when format 3 is selected with the D channel Digital interface selected in multiplexed mode.
After reset: 0CH in GCI
08H in µW/DSI

DR5	DR4	DR3	DR3	DR2	DR1	SR1	SR0

DR5-SR0 Receive D channel Time Slot Assignment
DR5-DR0 and SR1-SR0 bits define the binary number of the receive D channel time-slot. DR5-DR0 bits define the binary number of the 8 bits wide timeslot. Time slot are numbered from 0 to 63. Within this selected time slot., SR1,SR0 bits define the binary number of the 2 bits wide time-slot. Sub time-slots are numbered 0 to 3. The register content is taken into account at each frame beginning.

Transmit M4 channel register (TXM4)
(write only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

The TXM4 Register is constituted of 7 bits: m42, m43, m44, m45, m46, m47, m48. When the line is fully activated (super framing synchronized), the UID shall continuously send in the M4 channel field the register content to the line once per superframe. Register content is loaded in the transmit register at each superframe.
m41 is the act bit. m42 in LT mode in the LT to NT direction is the dea bit. These activation bits are controlled directly by the on chip activation encoder-decoder. The corresponding bits in the TXM4 register are not significant.

Transmit M5 and M6 channels register (TXM56)
(write only)
After reset: 3EH

-	-	LEC	m51	m61	m52	feb	CTC

LEC External Control pin
The logical level of the output EC is directly controlled by the bit LEC (GCI mode only).

m51, m61, m52 M5 and M6 spare over-head bits
Those spare overhead bits are normally equal to 1. Default value can be changed by setting the respective bits.

feb Transmit febe bit control
The febe bit which is normally at logical 1 and automatically set low in the following superframe when a CRC checking error has been detected in the previous received superframe may be forced to 0 by writing 0 in bit position feb. The febe bit set to zero is sent once to the line in the following available superframe.

CTC Corrupted Transmit CRC Control
CTC = 0: allows the normal calculation of the CRC for the transmitted data to the Line
CTC = 1: CRC result is transmitted inverted starting from next superframe. That ensure transmission of a corrupted CRC.

Activation control register (ACT)
(write only, µW only)
After reset XFH

-	-	-	-	C4	C3	C2	C1

This register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly adressed by means of the C/I channel. Activation Control instructions are coded on 4 bits.

Transmit EOC register (TXEOC)
(write only)
After reset: FFFH

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

TXEOC Register is constituted of 12 bits. When the line is fully activated (super framing synchronized), ST5410 shall continuously send into the EOC channel field the eoc bits twice per superframe. TXEOC register is loaded in the transmit register at each half a superframe.
The address of this register is composed only of 4 bits. The W/R indicator is not needed.

Receive spare M4 overhead bits register (RXM4)
(read only)
After reset: 7FH

-	m42	m43	m44	m45	m46	m47	m48

RXM4 Register is constituted of 8 bits. When the line is fully activated (super frame synchronized), ST5410 extracts the M4 channel bits. m41 is the act bit; m42 in NT mode is the dea bit these bits are under the control of the activation sequencer. No interrupt cycle is provided for the RXM4 register when a change on one of the activation bits is detected.
When one of the remaining received spare bits is validated following the criteria selected in the Configuration Register OPR, the RXM4 register content is queued in the interrupt register stack. Activation bits status are also delivered.

Receive m5, m6 overhead bits register (RXM56)
(read only)
After reset: FFH

-	ES2	ES1	m51	m61	m52	feb	neb

When the line is fully activated (super frame synchronized), ST5410 extracts the overhead bits.
When one of the received spare bits m51, m61, m52 is validated following the criterias selected in the Configuration Register OPR, the RXM56 register content is queued in the interrupt register stack.If the FIE bit in OPR register is set high, the RXM56 register content is queued in the interrupt register stack each time the febe bit is received equal zero with bit feb equal 0.
The CRC received from the far-end is compared at the end of the superframe with the CRC calculated by the UID during that superframe. If an error is detected, the febe bit in the transmit direction is forced equal zero in the next superframe. If the CIE bit in the OPR register is set high, the RXM56 register is queued in the interrupt register stack at each CRC error detected with bit neb equal zero.
ES1,ES2 bits indicates the status of the inputs pins ES1,ES2 respectively. At each status change, the RXM56 register is queued in the interrupt register stack.

Activation indication register (RXACT)
(read only)
Afterr reset: XHF

-	-	-	-	C4	C3	C2	C1

This Register is constituted of four bits: (C1, C2, C3, C4). In GCI mode, this register is directly connected to the C/I channel. At each activation status change, an interrupt request is queued in the interrupt register stack. In GCI mode, the C1-C4 bits are directly sent on the C/I channel. Activation Indication instructions are coded on 4 bits according to activation description.

Block Error counter 1 (EC1)
(read only)
After reset: 00H

ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

This Register indicates the binary value of the Error up-counter 1. The register accounts for the febe and mebe errors. When counter goes in overflow (FF) , an interrupt is provided for the EC1 register with value FF.

Offset Block error control counter 1 register (EC1) read only
(write only)
After reset: 00H

o7	o6	o5	o4	o3	o2	o1	o0

Block Error Counter 1 can be preset at a value given by Offset register EC1 Error. The counter is preset at that value each time the counter is read or when the preset value is loaded. o7-o0 is the binary value of the error up-counter 1 offset.

Receive EOC register (RXEOC)
(read only)

ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

The RX EOC Register is constituted of 12 bits. When the line is fully activated (super frame synchronized) and when a eoc message is received and validated in accordance with the criteria selected in the Configuration Register OPR, the RX EOC Register is queued in the interrupt register stack. The address of this register is composed only of 4 bits. The W/R indicator is not needed.
After each activation process, this register generates an interrupt giving the first received EOC channel content, even if it is a FFFH.

Table 4: Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms).
All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat
act = activation bit (set = 1 during activation)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
dea = deactivation bit (set = 0 to announce deactivation)
uoa = (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

Table 5: NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 602 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat

act = activation bit (set = 1 during activation)
ps_1, ps_2 = power status bits (set = 0 to indicate power problems)
ntm = NT in Test Mode bit (set = 0 to indicate test mode)
cso = cold-start-only bit (set = 1 to indicate cold-start-only)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
sai = S/T interface activation bit. Used in restricted activation only (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

LINE CODING AND FRAME FORMAT

2B1Q coding rule requires that binary data bits are grouped in pairs so called quats (see Tab.6). Each quat is transmitted as a symbol, the magnitude of which may be 1 out 4 equally spaced voltage levels (see Fig. 6). No redundancy is included and in the limit there is no bound to the Running Digital Sum (RDS), although scrambling controls the RDS in the pratical sense +3 quat referers to the nominal pulse wavwform specified in the ANSI standard. Other quats are deduced directly with respect of the ratio and keeping of the waveform.

The frame format used in UID follows ANSI and French specifications (see Tab. 4 and 5). Each complete frame cosists of 120 quats, with a line baud rate of 80 kbaud/s, giving a frame duration of 1.5ms. A9 quats sync-word defines the framing boundary. Furthermore, a Multiframe consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the multiframe boundary. Prior to transmisssion, all data, with the exception of the sync-word,is scrambled using a self-synchronizing scrambler to perform the specified 23rd-order polynomial. Descrambling is included in the receiver. Polynomial is different depending on the direction TE to NT or NT to TE.

Maintenance functions

M channel

In each frame there are 6 "overhead" bits assigned to various control and maintenance functions. Some programmable processing of these bits is provided on chip while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. See OPR, TXM4, TXM56, TXEOC, RXM4, RXM56, RXEOC register description fo details. New data written to any of the Overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half superframe, as appropriate.

Embedded Operatione Channel (EOC)

The EOC channel consists of two complete 12 bits messages per superframe, distributed through the M1, M2 and M3 bits of each frame. Each message is composed of 3 fields; a 3 bit address identifying the message destination/origin, a 1 bit indicator for the data mode i.e. encoded message or raw data, and an 8 bits information field. The Control Interface (Microwire or Monitor channel in GCI) provides access to the complete 12 bits of every message in TX and RX EOC registers.

UID does not recognize the received and encoded messages e. g. send corrupted CRC, then the apprpriate command register instruction must be written to the device to invoke the relevant function.

It is possible to select a transparent transmission mode in which the EOC channel can be considered as a transparent 2 kbit/s channel. See OPR register description for details.

M4 channel

M4 bit positions of every frame is a channel in which are trasmitted data bits loaded from the TXM4 transmit register and from the on-chip activation sequencer once the superframe. On the receive side, M4 bits from one complete superframe are first valitated and then stored in the RXM4 Receive Register or transmitted to on-chip activation sequencer. See OPR, TXM4 and RXM4 registers description for details.

Spare M5 and M6 bits

The spare bit positions in the M5 and M6 field form a channel in which are transmitted data bits loaded from the TXM56 transmit register. On the receive side, the spare bits in the M5 and M6 field are first validated and then stored in the RXM56 receive register. See OPR, TXM56 and RXM56 registers description for details.

CRC calculation/checking

In transmit direction, an on-chip CRC calculation circuit automatically generates a checksum of the 2B+D+M4 bits using the specified 12th order polynomial. Once per superframe, the CRC is transmitted in the M5 and M6 bit positions. In receive direction, a checksum is again calculated on the same bits as they are received and, at the end of the superframe compared with the received CRC. The result of this comparison generates a "Far End Block Error" bit (febe) which is transmitted back towards the other end of the Line in the next bute-one superframe and an indication of Near End Block Error is sent to the system by means of Register RXM56. If there is no error in superframe, febe is set = 1, and if there is one or more errors, febe is set = 0.

UID also includes an 8 bits Block Error Counter associated with the febe bits transmitted and received. Block error counting is always enabled but it is possible to disabled the overflow interrupt and/or to enabled/disabled the interrupt issued at each received or transmitted block error detection. See OPR register for details.

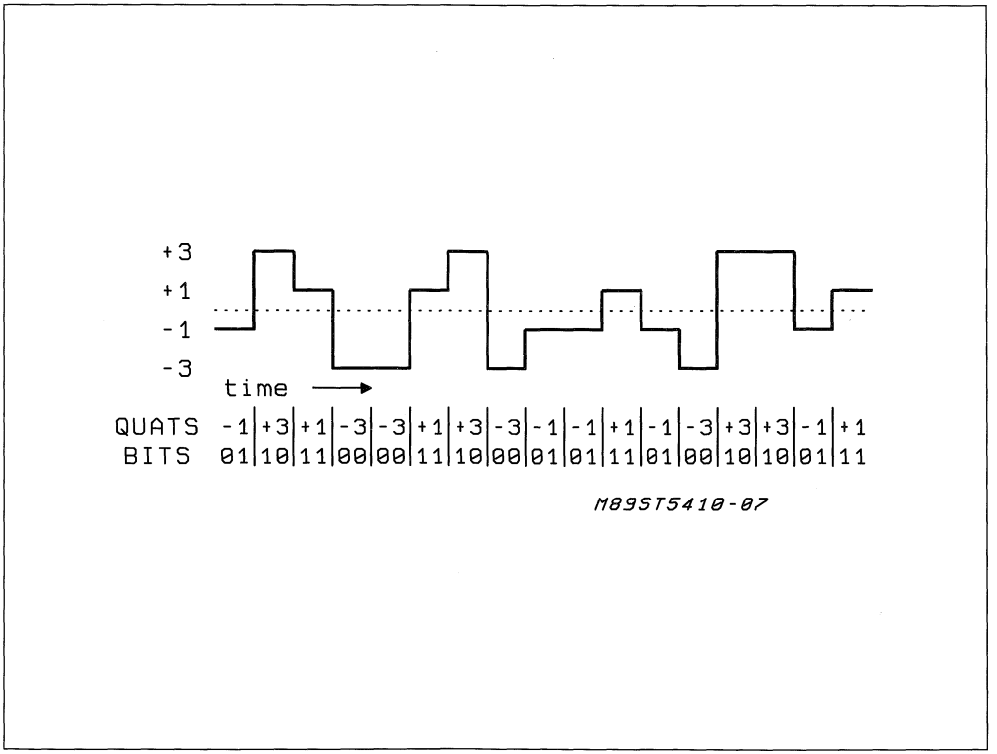
Table 6: 2B1Q Encoding of 2B+ D Fields.

Data	Time → B_l				B_g				D
Bit Pairt	$b_{11}b_{12}$	$b_{13}b_{14}$	$b_{15}b_{16}$	$b_{17}b_{18}$	$b_{21}b_{22}$	$b_{23}b_{24}$	$b_{25}b_{26}$	$b_{27}b_{28}$	d_1d_2
Quat # (relative)	q_1	q_2	q_3	q_4	q5	q_6	q_7	q_8	q_9
# Bits	8				8				2
# Quats	4				4				1

Where: b_{11} = first bit of B_1 octet as received at the S/T interface
b_{18} = last bit of B_l octet as received at the S/T interface
b_{21} = first bit of B_2 octet as received at the S/T interface
b_{28} = last bit of B_2 octet as received at the S/T interface
d_1 d_2 = consecutive D-channel bits (d_1 is first bit of pair as received at the S/T interface)
q_i = ith quat relative to start of given 18-bit 2B+D data field.

NOTE: There are 12 2B+D 18-bit fields per 1.5 msec basic frame.

Figure 6: Example of 2B1Q Quaternary Symbols.



LINE SECTION

Data transmitted to the line consists of the 2B+D channel data received from the Digital Interface through an elastic data buffer allowing any phase deviation with the line, the activation/deactivation bits (M4) from the on-chip activation sequencer, the CRC code plus maintenance data (eoc channels) and other spare bits in the overhead channels (M4, M5, M6). Data are multiplexed and scrambled prior to addition of the sync-word, whiich generated within the device. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver Outputs, LO+, LO- are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer designed as shown in the Application section, results in a signal amplitude of normally 2.5V pk on the line for single quats of the +3 level. However, because of the RDS accumulation of the 2B1Q line code, continuous random data will produce signal swings considerably greater than this on the line. Short-circuit protection is included in the output stage; over-voltage protection must be provided externally.

In LT applications, the Network reference clock given by the FSa 8kHz clock input synchronizes the transmitted data to the line. The Digital Interface normally accepts BCLK and Fsa signals from the network, requiring the selection of Slave Mode in CRI. Retiming circuitry on chip allow the 15.36MHz crystal oscillator (or the logic level clock input on XTAL1) to be plesiochronous with respect to the network clock provided the sum of frequency inaccuracies, expressed in ppm deviation from nominal, of the network clock plus the XTAL1 one does not exceed 150ppm.

In NT applications, data is transmitted to the line with a phase deviation of half a frame relative to the received data as specified in the ANSI standard.

The receive input signal should be derived from the transformer by a coupling circuit aa shown in the Application section. At the front end of the receive section is a continuous filter which limits the noise bandwidth to approximately 200kHz. Then, a precanceller provides a degree of analog echo cancellation in order to limit the dynamic range of the composite signal which noise bandwidth limited by a 4th order butterworth switched capacitor low pass filter. After an automatic gain control, a 13bits A/D converter then samples the composite received signal before the echo cancellation from local transmitter by means of an adaptive digital transversal filter. The attenuation and distortion of the received signal from the far-end, caused by the line, is equalized by a second adaptive digital filter configured as a Decision Feedback Equlizer (DFE), that restores a flat channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

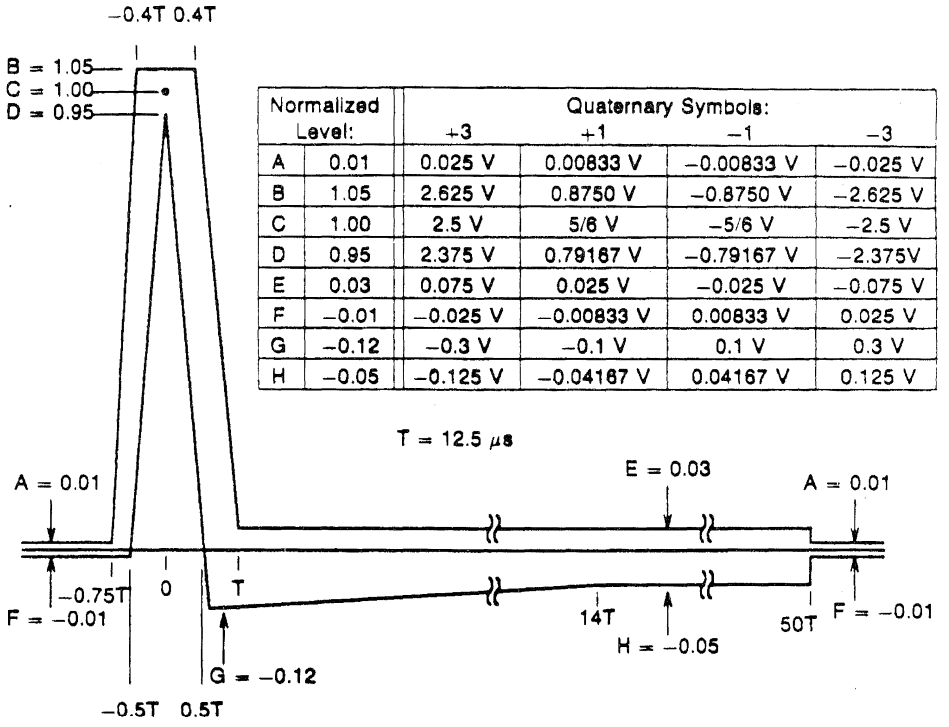
A timing recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a very low-jitter clock for optimum sampling of the received symbols. The 15.36MHz crystal oscillator (or the logic level clock input) provides the reference clock for DPLL. In NT configuration, MCLK output provides a very low jitterized 15.36MHz clock to the system.

Received data is then detected and flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. ST5410 is frame-synchronized when two consecutive synchwords have been consecutively detected. Frame lock will be maintained until six consecutive errored sync-words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss of frame sync condition persists for 480ms the device will cease searching, cease transmitting and go automatically into the RESET state, ready for a further cold start. When UID is frame-synchronized, it is superframe-locked upon the first superframe-locked upon the first superframe sync-word detection. No loss of superframe sync-word is provided.

While the receiver is synchronized, data is descrambled using the specified polynomial, and individual channels demultiplexed and passed to their respective processing circuits: user's 2B+D channel data is transmitted to the Digital Interface through an elastic data buffer allowing any phase deviation with the Line; the activation/deactivation bits (M4) are transmitted to the on-chip cativation sequencer; CRC is transmitted to CRC checking section while maintenance data (eoc) and other spare bits in the overhead channels (M4, M5, N6) are stored in their respective Rx registers.

In NT applications, if the Digital Interface is selected in master mode (see CR1) BCLK and FSa clock outputs are phase-locked to the recovered clock. If it is selected in Slave mode ie for NT1-2 application, the on-chip elastic buffers allow BCLX and FSa to be input from an external source, which must be frequency locked to the received line signal ie using the XTA1 output but with arbitrary phase.

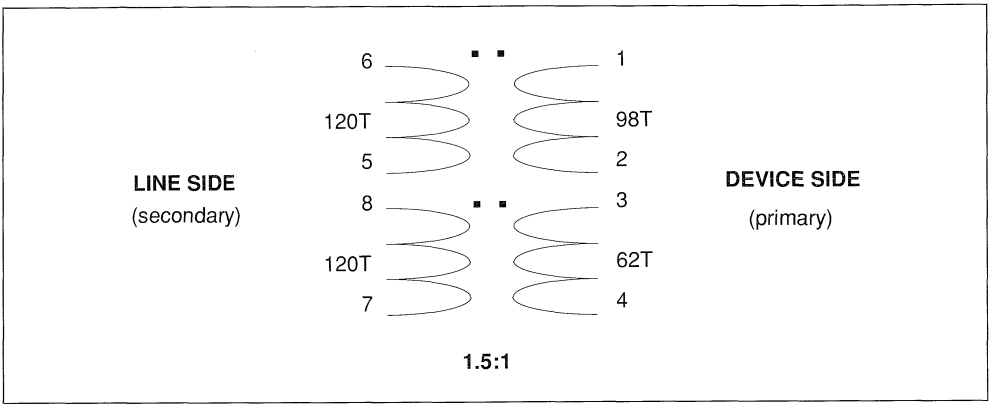
Figure 7: Normalized Output Pulse From NT1 or LT..



Normalized Level:		Quaternary Symbols: +3	+1	−1	−3
A	0.01	0.025 V	0.00833 V	−0.00833 V	−0.025 V
B	1.05	2.625 V	0.8750 V	−0.8750 V	−2.625 V
C	1.00	2.5 V	5/6 V	−5/6 V	−2.5 V
D	0.95	2.375 V	0.79167 V	−0.79167 V	−2.375V
E	0.03	0.075 V	0.025 V	−0.025 V	−0.075 V
F	−0.01	−0.025 V	−0.00833 V	0.00833 V	0.025 V
G	−0.12	−0.3 V	−0.1 V	0.1 V	0.3 V
H	−0.05	−0.125 V	−0.04167 V	0.04167 V	0.125 V

Line Interface Circuit
It is very important, for compliance with the ANSI and French standard, that the recommended line interface circuit should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure the performance requirements are met under all the specified loop conditions. Deviations from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

Figure 8: Transformer Design.



Turns Ratio: Np:Ns = 1:1.5.
Secondary Inductance: Lp 27mH.
Winding Resistances: 30 ohms > (2.25Rp + Rs) > 10 ohms.
Return Loss at: 40 kHz against 135 ohms 26 dB.
Saturation characteristics: THD –70dB when tested with 50mA d.c. through the secondary and a 40kHz sine-wave injected into the primary at a level which generates 5V p-p into 135 ohms at the secondary.

List of suppliers:

SHOTT
PULSE ENGINEERING
AIE

Table 7.

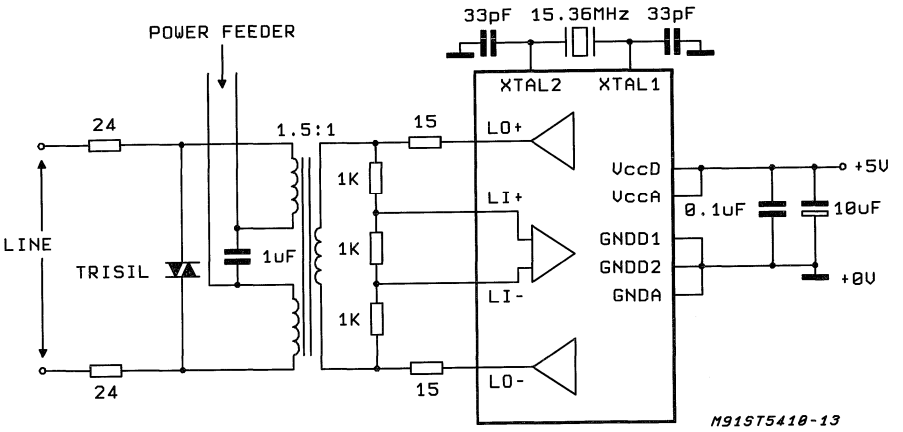
WINDING	NUMBER OF TURNS	WIRE GAUCE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG
WINDING	**INDUCTANCE**	**RESISTANCE**
1-2 + 3-4	12 mH	less than 5 ohms
5-6 + 7-8	27 mH	less than 10 ohms

Note: the split primary winding is designed to minimize leakage inductance.

Board Layout

While the pins of the UID are well protected against electrical misuse, it is recommended that the standard CMOS practise of applayng GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used. Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the ST5410. To maximize performance, do not use the philosophy of separating analog and digital grounds for chip. The 3 GND pins should be connected together as close as possible to the pins, and the 2 VCC pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the 3 GND pins order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 1.5µF should be connected from this common point to VCC pins as close as possible to the chip. Taking care with the board layout in the following ways will also help prevent noise injection into the receiver frontend and maximize the transmission performances. Keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components. Keep the device, the components connected to LI+/LI- and the transformer as close as possible. Simmetrical layout for the line interface is suggested.

Figure 9: Recommended Connections.



0.1% MATCHING IS REQUIRED TO MEET THE LONGITUDINAL BALANCE SPECIFICATION

THE 15ohm AND 1K RESISTORS IN THE INTERFACE CIRCUIT SHOULD BE 1%.

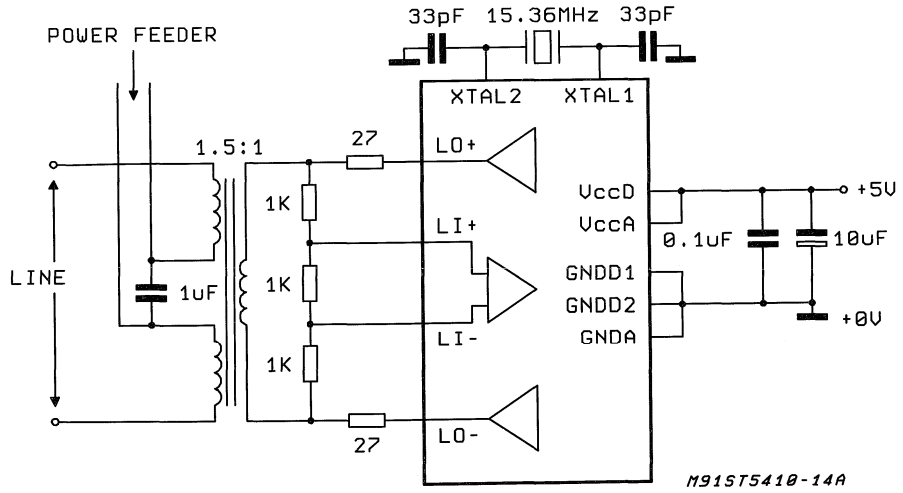
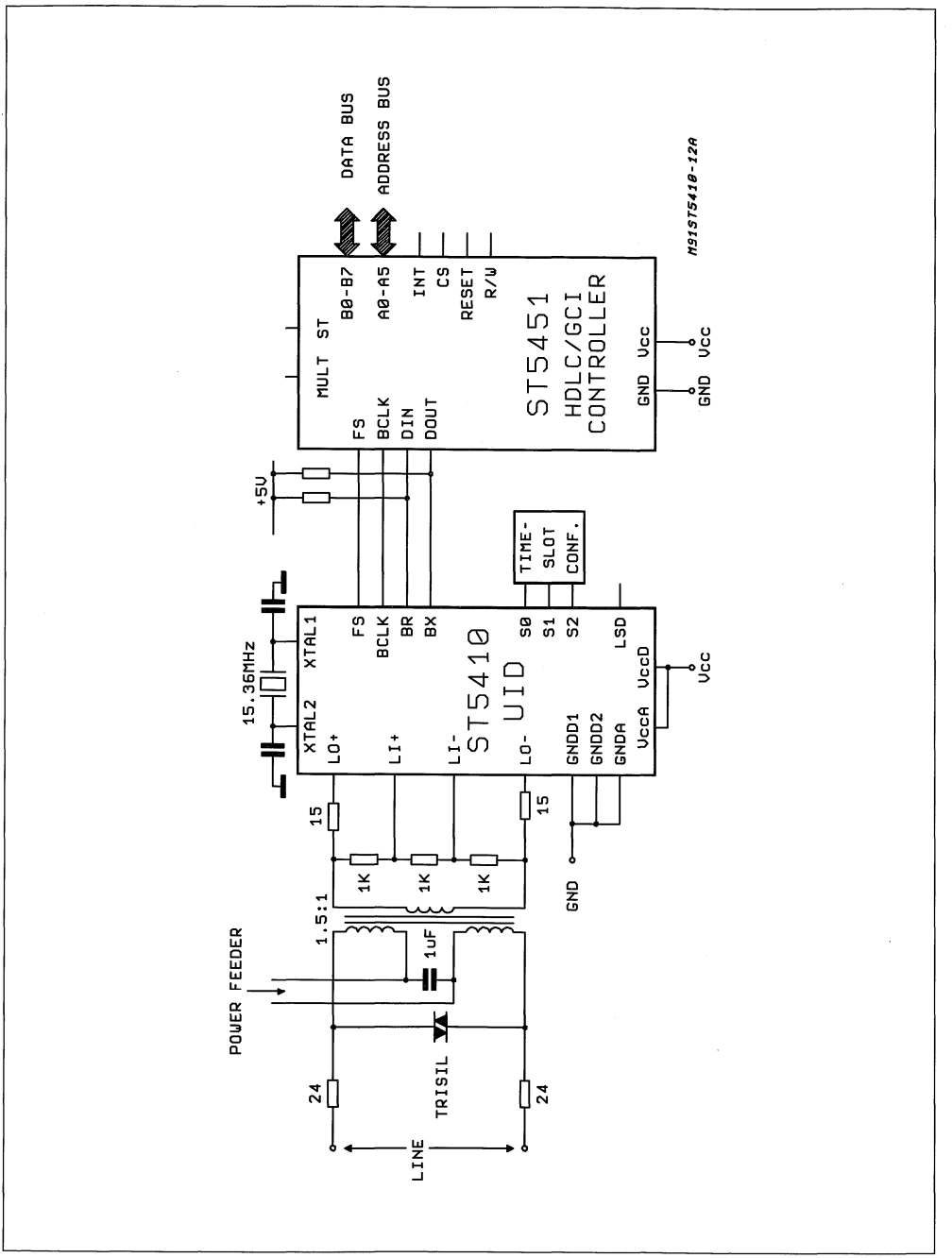


Figure 10: LT Application



APPENDIX A
State Matrix

EVENT	STATE NAME	Power Off	Full Reset	Alertg	Awake	EC Training	WAIT SN2	CHECK SN2	EC Covrg'd	SW Sync	ISW Sync	Active	Deact'n Alert'n	Tear Down	Pending Deact'n	Recv Reset
	STATE CODE	J0	J1	J2	J3	J4	J4. 1	J4.2	J5	J6	J7	J8	J9	J10	J11	J12
	TX	SL0	SL0	TL	SL0	SL1	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL3 dea = 1 no change (*)	SL3 dea = 1 act = 1	SL3 dea = 0 act = 0	SL0	SL0	SL0
POWERON		J1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
ACTIVATION REQUEST (AR)		/	ST T5 J2	-	-	-	-	-	-	-	-	-	-	-	-	-
DEACTIVATION REQUEST (DR)		/	-	-	-	-	-	-	-	-	J9	J9	-	-	-	-
END OF TONE TL (3 ms)		/	/	J3	-	/	/	/	/	/	/	/	/	/	/	/
RECEIVED TONE TN and ACTIVATION REQUEST (AR)		/	ST T5 J3 AP	-	-	/	/	/	/	/	/	/	/	/	/	ST T5 STP T7 J3 AP
LOSS OF SIGNAL ENERGY		/	-	-	J4	-	-	J4.1	/	/	/	/	/	/	/	/
ECHO CANCELLER CONVERGED		/	-	-	-	J4.1	-	-	-	-	-	-	-	-	-	-
B-ASIC FRAME SYNC (SW)		/	/	/	/	/	/	/	J6	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	/	STP T5 J7 SYNC	-	-	-	-	-	-
RECEIVED act = 0		/	/	/	/	/	/	/	/	/	-	J7 EI	-	-	-	-
RECEIVED act = 1		/	/	/	/	/		/	/	/	J8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	/	J10 EI	J10 EI	-	-	-	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	/	/	/	/	ST T7 J12 EI	ST T7 J12 EI	ST T7 J12 EI	-	/	/	/
END OF THE LAST SUPERFRAME WITH dea = 0 (4th)		/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
EXPIRY OF TIMER (**) T5 (15 seconds)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	/	-	/	-	/	/
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	/	/	/	/	/	/	/	ST T7 J12	J1 D1	-
EXPIRY OF TIMER (**) T7 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1
DETECTION OF SIGNAL ENERGY		/	-	-	-	-	J4.2	J5	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	-	-	-	-	-	-

(*) FAO command is needed to send act = 0
(**) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN LT MODE

EVENT	STATE NAME	Power Off	Full Reset	Alertg	EC Training	WAIT SL	CHECK SL	EC Covrg'd	SW Sync	ISW Sync	Pending Active	Active	Pending Deact'n	Tear Down	TE Inactive	Recv Reset
	STATE CODE	H0	H1	H2	H3	H3.1	H3.2	H4	H5	H6	H7	H8	H9	H10	H11	H12
	TX	SN0 INFO0	SN0 INFO0	TN INFO0	SN1 INFO0	SN0 INFO0	SN0 INFO0	SN0 INFO0	SN2 INFO0	SL3 act = 0 INFO2	SN3 act = 1 INFO2	SN3 act = 1 INFO4	SN3 no change	SN0 INFO0	SN3 act = 0 INFO2	SN0 INFO0
POWERON		H1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
RECEIVED S/T INFO 1 SIGNAL (Received AR)		/	ST T4 H2	-	-	-	-	-	-	-	-	/	/	-	/	-
RECEIVED S/T INFO 3 SIGNAL (Received AI)		/	/	/	/	/	/	/	/	H7	-	-	-	-	H7	/
RECEIVED S/T INFO 0 SIGNAL (Received EI)		/	-	-	-	-	-	-	-	-	H11	H11	-	-	-	-
END OF TONE TN (9 ms)		/	/	H3	-	-	-	/	/	/	/	/	/	/	-	/
RECEIVED TONE TL and ACTIVATION REQUEST (AR)		/	ST T4 H2 LSD	-	/	/	/	/	/	/	/	/	/	/	-	ST T4 STP T6 H2 LSD
ECHO CANCELLER CONVERGED		/	-	-	H3.1	-	-	-	-	-	-	-	-	-	-	-
BASIC FRAME SYNC (SW)		/	/	/	/	/	/	H5	-	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	STP T4 H6 AP	-	-	-	-	-	-	-
RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 DP	H9 DP	H9 DP	-	-	H9 DP	-
RECEIVED act = 0 and dea = 1		/	/	/	/	/	/	/	/	/	-	H7 EI	-	-	-	-
RECEIVED act = 1 and dea = 1		/	/	/	/	/	/	/	/	/	H8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	H10 EI	H10 EI	H10 EI	-	-	H10 EI	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	ST T6 H12 EI	/	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	/	/	ST T6 H12 EI	-
EXPIRY OF TIMER (*) T4 (15 seconds)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	/	/	/	/	-	/	-
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	H3.1	/	/	/	/	/	ST T6 H12	ST T7 J12	/	/
EXPIRY OF TIMER T6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 DI
DETECTION OF SIGNAL ENERGY		/	-	-	-	H3.2	H4	-	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	-	-	-	-	-	-	-

(*) When timer is enabled (default)

ACTIVATION/DEACTIVATION FINITE STATE MATRIX IN NT MODE

APPENDIX B
Electrical Parameters

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	– 0.3 to 7.0	V
V_{IN}	Input Voltage	– 0.3 to 7.0	V
T_A	Operting Temperature Range	0 to 70	°C
T_{stg}	Storage TemperatureRange	– 55 to 150	°C

TRANSMISSION ELECTRICAL PARAMETERS

Parameter	Min.	Typ.	Max.	Unit
LINE INTERFACE FEATURES				
Differential Input Resistance		140		KΩ
Line Driver Load			1000	pF
Differential Output Offset at LO+ / LO–	– 30	0	30	mV
Power up Output Differential Impedance (20KHz Bandwidth)		1		Ω
Power Down Output Diffrential Impedance	8	12	16	Ω
POWER CONSUMPTION				
I_{CCO}		2		mA
I_{CC1}		55		mA
TRANSMISSION PERFORMANCES				
Transmit Pulse Amplifier		3.2		V
Transmit Pulse Linearity	36	50		dB
Input Pulse Amplitude Differential Between LI+ and LI	±4		±800	mVpk

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Dig Inputs			0.7	V
V_{IH}	Input High Voltage	All Dig Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Inputs			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Inputs	V_{CC}–0.5		0.7	V
V_{OL}	Output Low Voltage	Br, I_O = +7mA All other Dig Outputs, IO = 1mA			0.4	V
V_{OH}	Output High Voltage	Br, I_O = –7mA All other Dig Outputs, I_O = –1mA All Outputs, I_O = –100µA	2.4 2.4 V_{CC}–0.5			V V V
I_L	Input Current	Any Dig Input, GND < V_{IN} < V_{CC}	–10		10	µA
I_{OZ}	Output Current in High Impedance State (TRISTATE)	Br, INT, LSD, CO, DR GND, V_{OUT} < V_{CC}	–10		10	µA

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
MASTER CLOCK (timing diagram 15)						
FMCLK	Frequency of MCLK Tolerance	Including Temperature, Aging, Etc...	 –100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tWMH	Clock Pulse Width, MCLK High Level	$V_{IH} = V_{CC} - 0.5V$	20			ns
tWML	Clock Pulse Width, MCLK Low Level	$V_{IL} = 0.5V$	20			ns
tRM tFM	Rise Time of MCLK Fall Time of MCLK	Used as a Logic Input			10 10	ns ns
DIGITAL INTERFACE (timing diagrams 1 to 12)						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 Format 4 and GCI Mode	256 512		4095 6144	KHz KHz
tWBH	Clock Pulse Width, BCLK High Level	Measured from V_{IH} to V_{IH}	30			ns
tWBL	Clock Pulse Width, BCLK Low Level	Measured from V_{IL} to V_{IL}	30			ns
tRB	Risae Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High or Low to BCLK Low	DSI or GCI Slave Mode only	30			ns
tHBF	Hold Time, BCLK Low to FS High or Low	DSI or GCI Slave Mode only	20			ns
tDBF	Delay Time, BCLK High to FS High or Low	DSI or GCI Master Mode only	–20		20	ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150pF + 2 LSTTL Loads			80	ns
tDBDZ	Delay Time, BCLK High to Data HZ				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150pF + 2 LSTTL Loads See Timing Diagram 9			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHBD	Hold time, BCLK to Data Invalid		20			ns
tDBT	Delay Time, BCLK High to TSR Low	Load = 100pF + 2 LSTTL Loads			80	ns
tDBTZ	Delay Time, BCLK Low to TSR HZ				50	ns
tDFT	Delay Tie, FS High to TSR Low	Load = 100pF + 2 LSTTL Loads See Timing Diagram 12			80	ns
D PORT IN CONTINUOUS MODE: 16KBITS/SEC (timing diagram 13)						
tSDD	Setup Time, DCLK Low to DX High or Low		50			ns
tHDD	Hold Time, DCLK Low to DX High or Low		50			ns
tDDD	Delay Time, DCLK High to DR High or Low	Load = 50pF + 2 LSTTL Loads			80	ns
MICROWIRE CONTROL INTERFACE (timing diagram 14)						
FCCLK	Frequency of CCLK				5	MHz
tWCH	Clock Pulse Width, CCLK High Level	Measured from V_{IH} to V_{IH}	85			ns
tWCL	Clock Pulse Width, CCLK Low Level	Measured from V_{IL} to V_{IL}	85			ns
tRC	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			15	ns
tFC	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			15	ns
tSSC	Setup Time, CSB Low to CCLK High		60			ns
tHCS	Hold Time, CCLK Low to CSB High		10			ns
tWSH	Duration of CSB High		200			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tDSO	Delay Time, CSB Low to CO Valid	Out First Bit on CO			50	ns
tDCO	Delay Time CCLK Low to CO Valid	Load = 50 pF + 2LSTTL Loads			50	ns
tDCOZ	Delay Time, CCLK Low to CO HZ				50	ns
tDCI	Delay Time, CCLK Low to INTB Low or HZ	Load = 80pF + 2LSTTL Loads			50	ns

Figure 11: BCLK, FSA, FSB, SLAVE MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

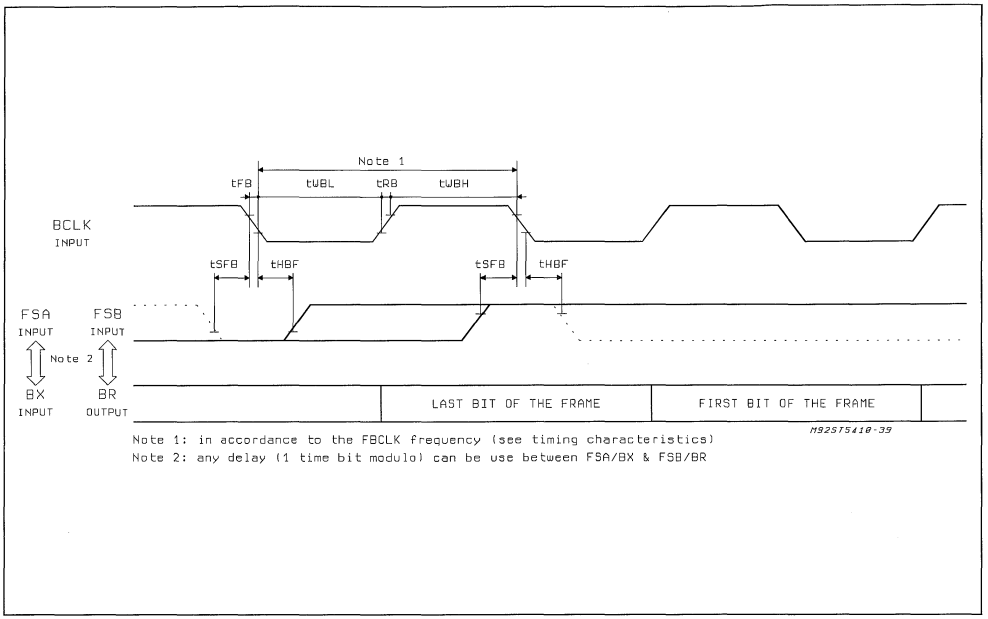


Figure 12: BCLK, FSA, FSB, SLAVE MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

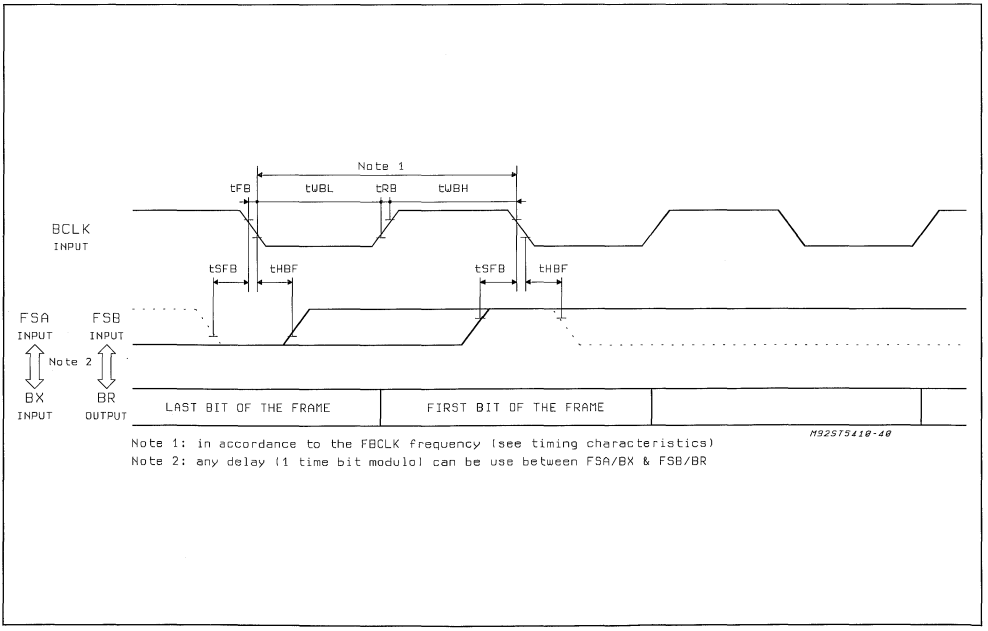


Figure 13: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

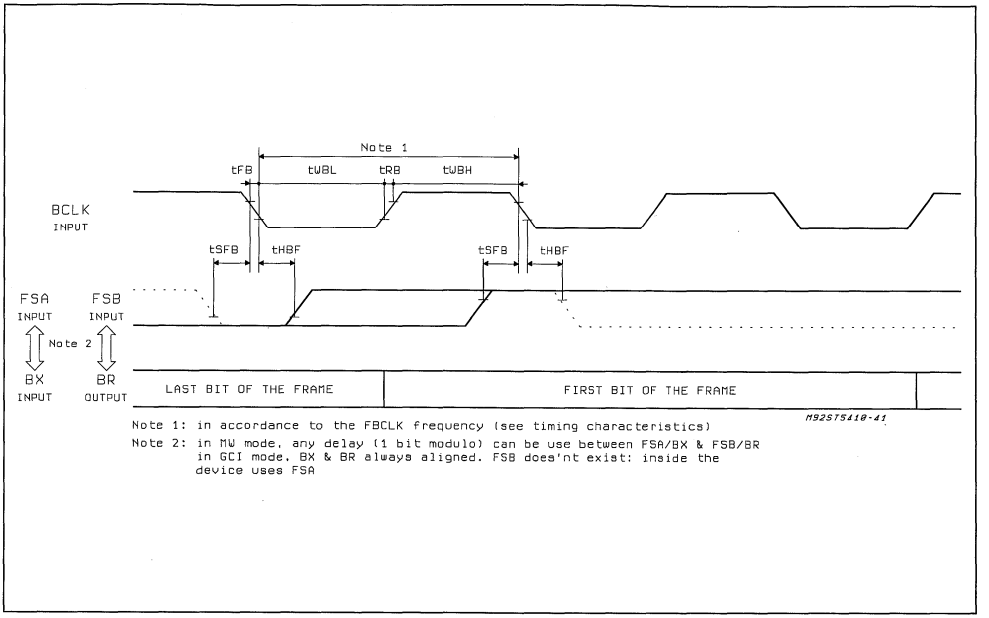


Figure 14: BCLK, FSA, FSB, MASTER MODE, DELAYED MODE, FORMATS 1 2 3 (MW ONLY)

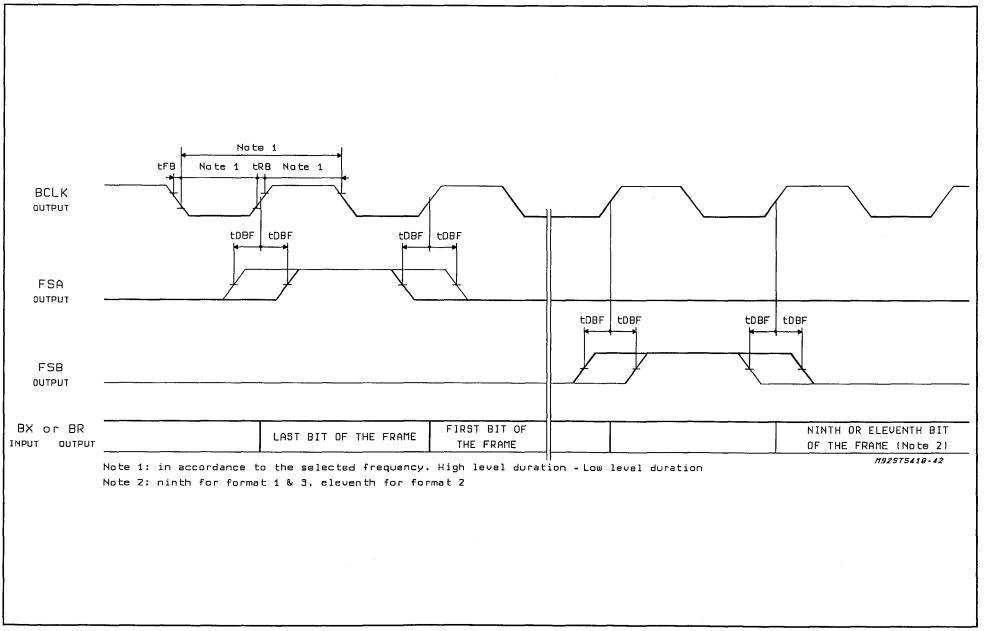


Figure 15: BCLK, FSA, FSB, MASTER MODE, NON DELAYED MODE, FORMATS 1 3 (MW ONLY)

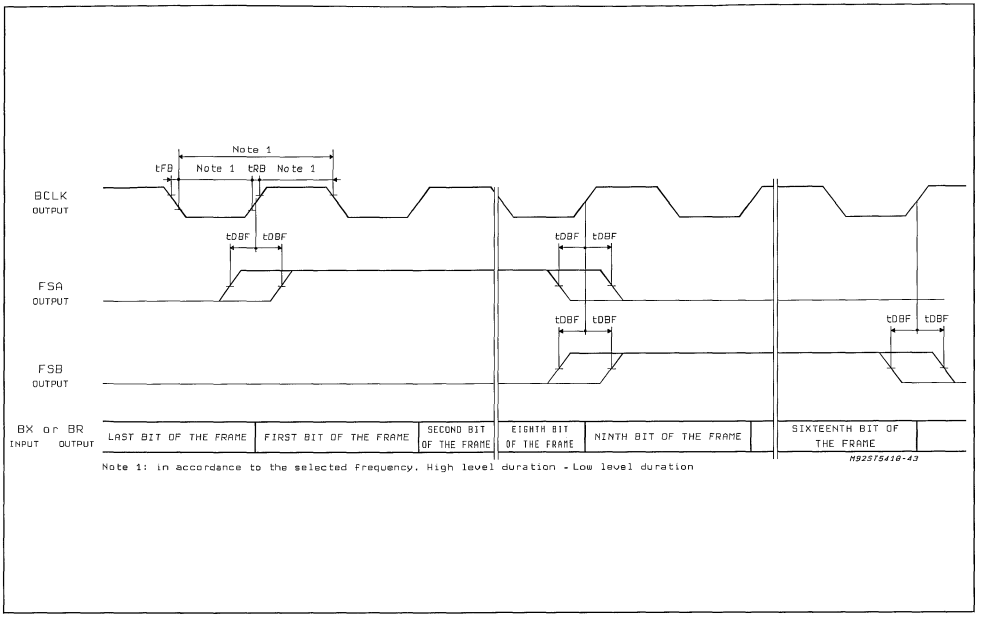


Figure 16: BCLK, FSA, FSB, SLAVE MODE, FORMAT 4 ALWAYS NON DELAYED MODE, (MW and GCI MODE)

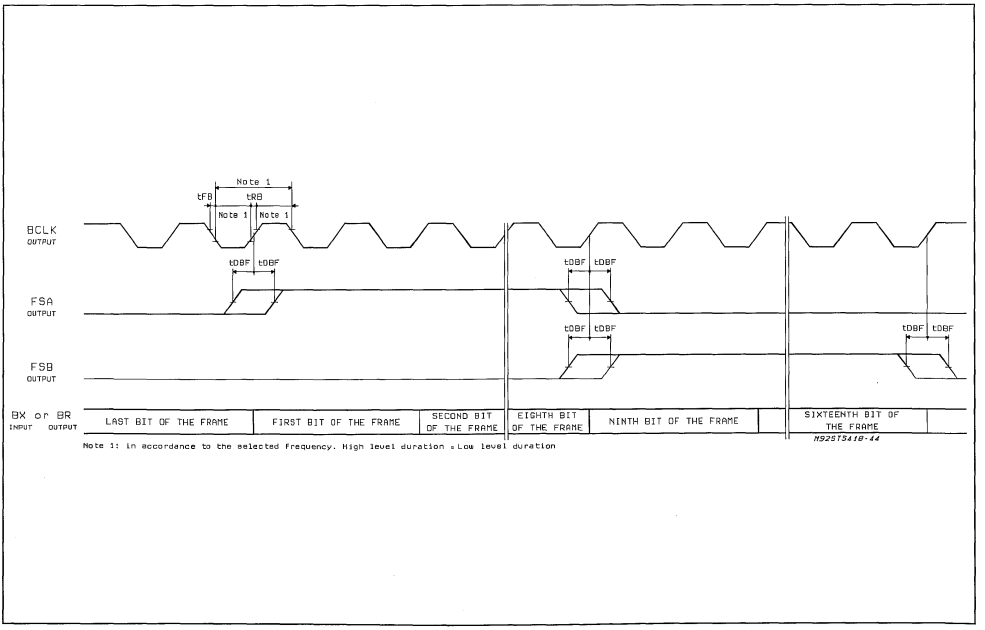


Figure 17: BX, DX, BR, DR, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

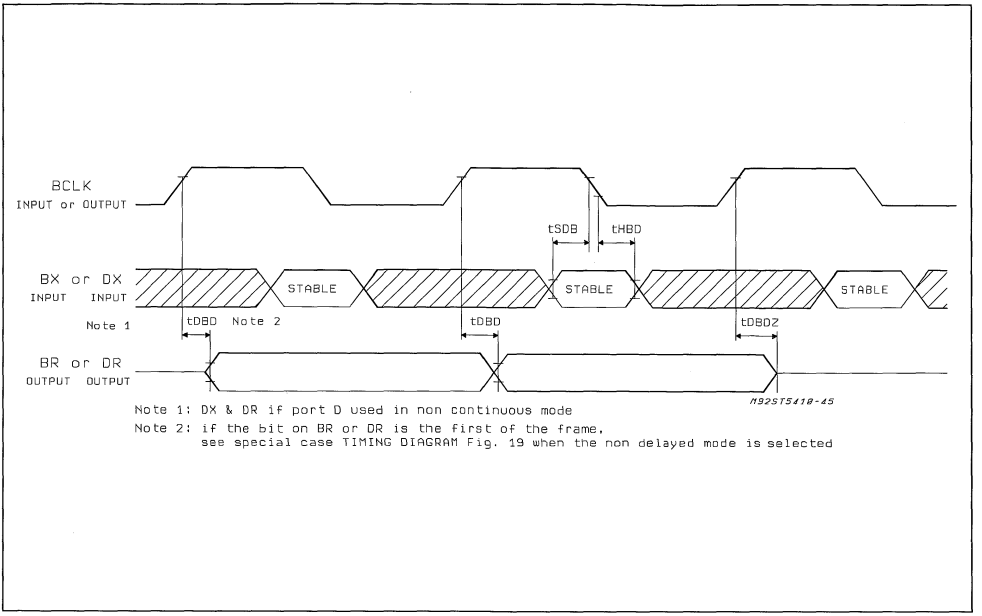


Figure 18: BX, DX, BR, DR, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED, FORMATS 1 2 3 (MW & GCI MODE)

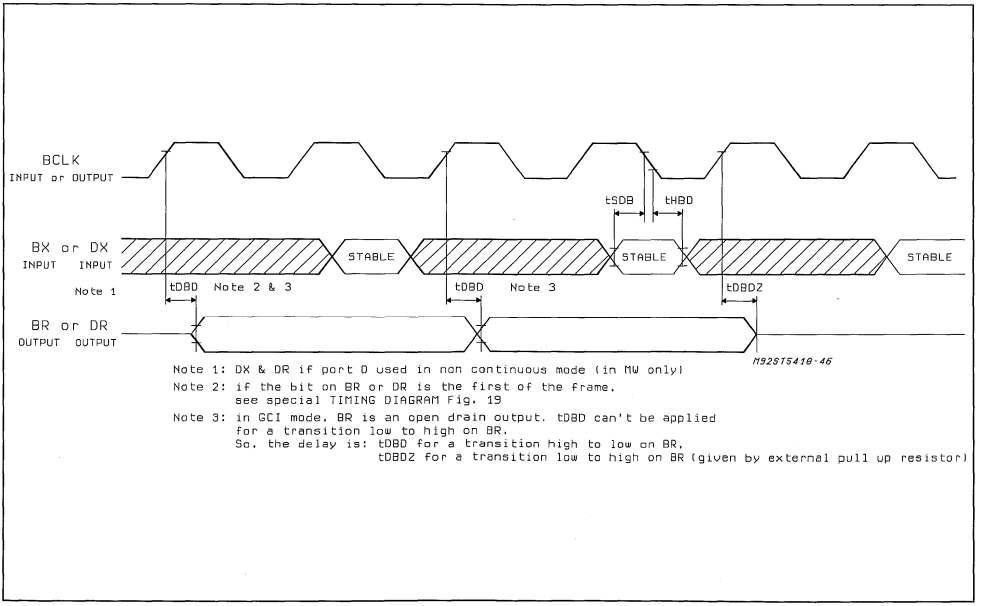


Figure 19: SPECIAL CASE BR, DR, ONLY FIRST BIT OF THE FRAME, IN SLAVE AND NON DELAYED MODES FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

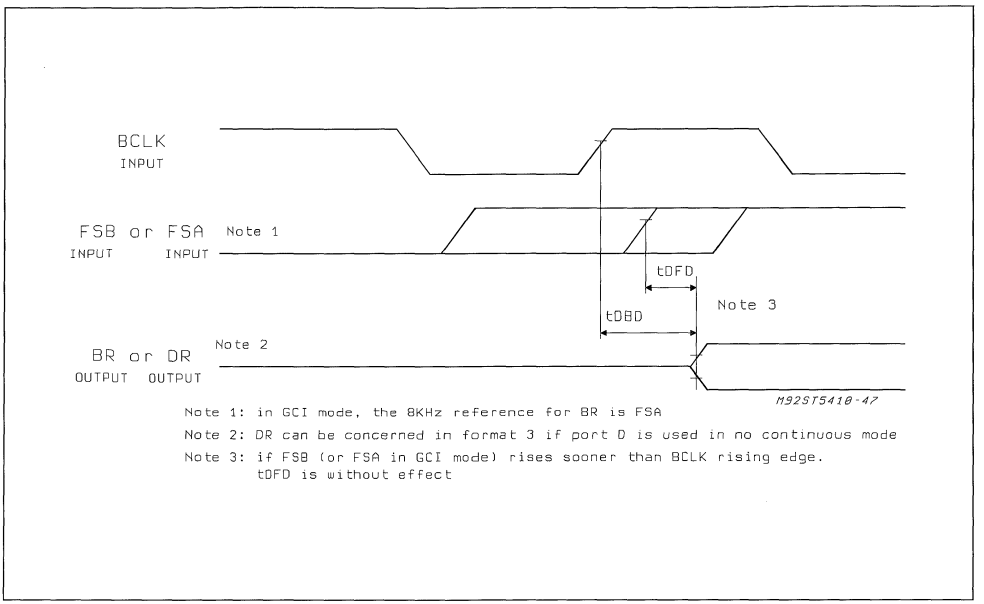


Figure 20: TSRB, SLAVE & MASTER, DELAYED & NON DELAYED, FORMATS 1 2 3 (MW ONLY)

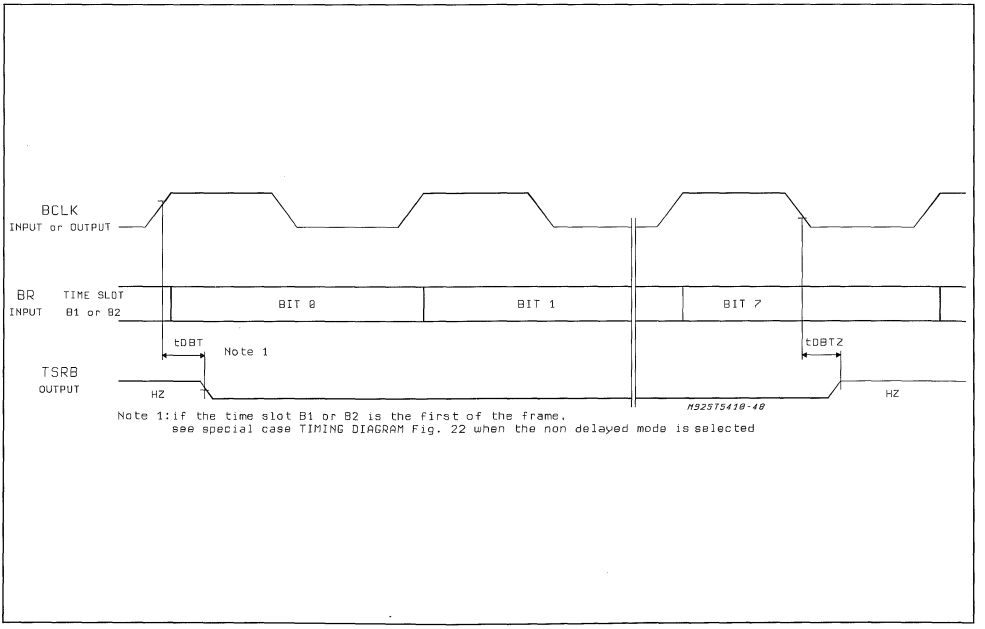


Figure 21: TSRB, SLAVE & MASTER, FORMAT 4 ALWAYS NON DELAYED MODE (MW & GCI)

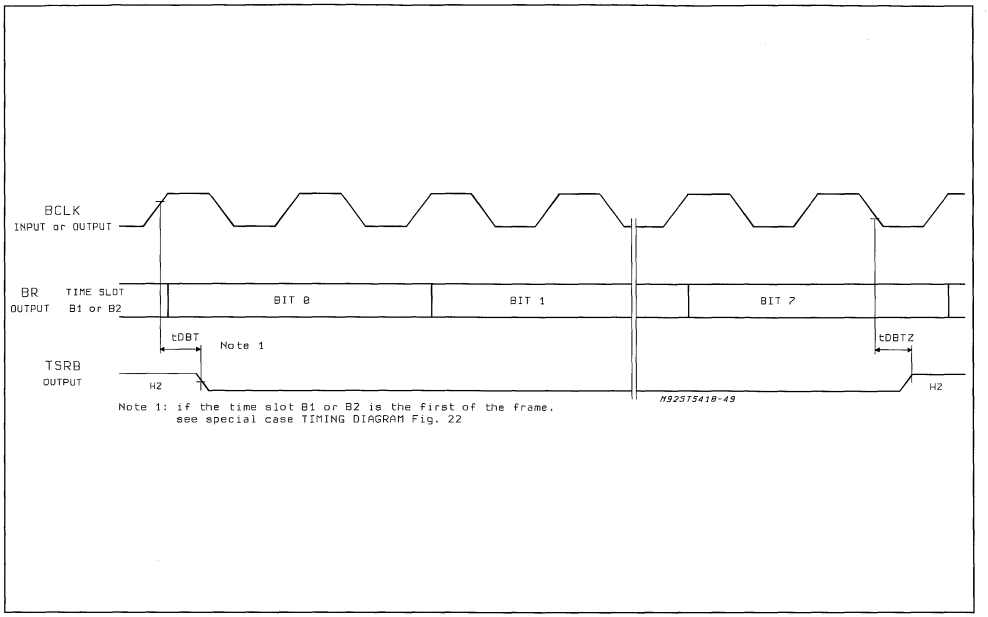


Figure 22: SPECIAL CASE TSRB, B1 OR B2 FIRST CHANNEL OF THE FRAME, IN SLAVE & NON DELAYED MODE, FORMATS 1 3 (MW MODE), FORMAT 4 (MW & GCI MODE)

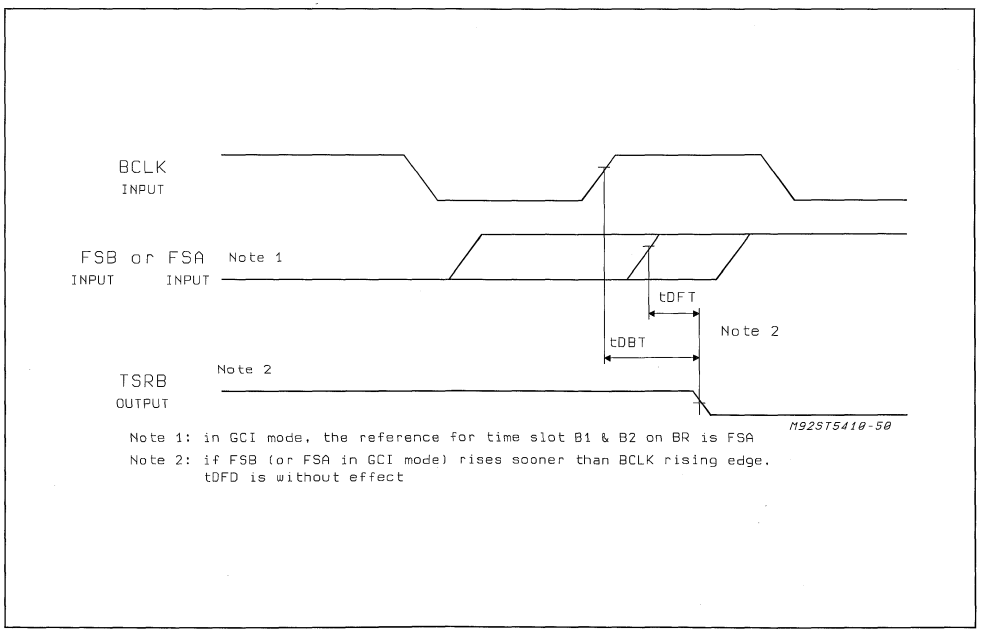


Figure 23: DCLK, DX, DR IN CONTINUOUS MODE SLAVE & MASTER, DELAYED & NON DELAYED MODES ALL FORMATS IN MW MODE ONLY

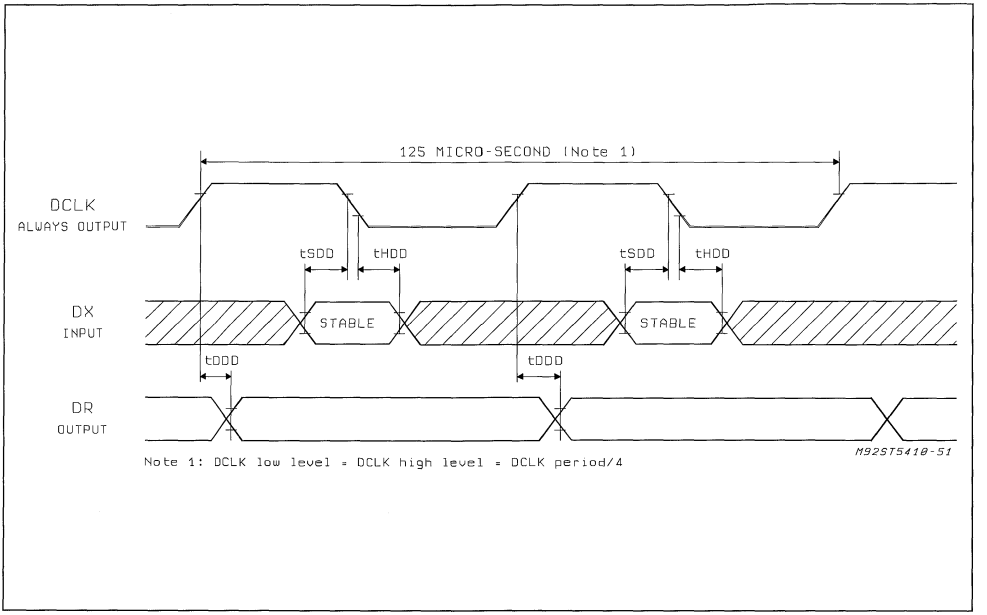


Figure 24: MW PORT

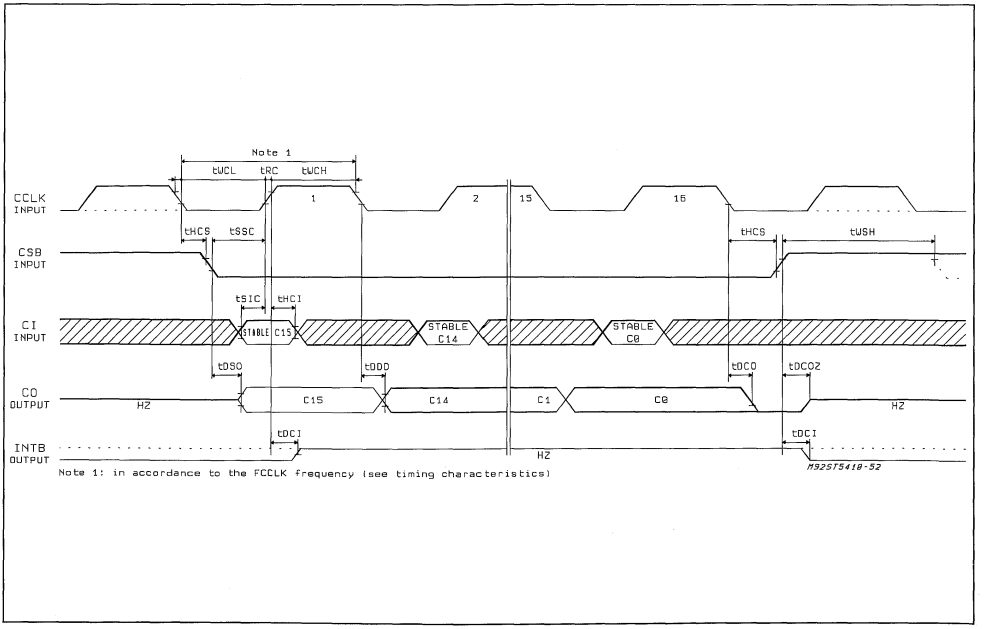
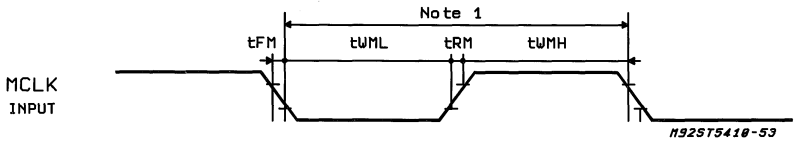


Figure 25: MCLK ALL MODES



Note 1: in accordance to the FMCLK frequency (see timing characteristics)

ST5410
2B1QU INTERFACE DEVICE

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INTRODUCTION

The SGS-THOMSON ST5410 is a complete monolithic transceiver for ISDN Basic access data transmission on twisted pair subscriber loops typical of public switched telephone networks. The device provides the required U-line interface together with a second on-board interchip industry-standard interface which may be chosen as GCI or MICROWIRE(TM)/DSI, as required. The device is fully compatible with both ANSI T1.601-1988 U.S. and CSE-C32-11 French specifications.

The equivalent of 160 kbits/s full-duplex transmission on a single twisted pair is provided. Frames comprise two B-channels, each of 64kbit/s, one D-channel of 16kbit/s, an additional M channel of 4kbit/s for loop maintenance and other user functions, and 12kbit/s is reserved for framing. The ISDN data rate of 144kbits/s is transmitted transparently (B1, B2, and D channels) together with control/status information for activation/deactivation of OSI layer 1 and for switching of test loops. An incorporated finite-state machine controls ISDN Layer 1 Activation/deactivation according to the ANSI and French specifications.

The circuit handles frame conversion from the U-line to GCI/MICROWIRE interfaces, and carries out recovery of timing reference signals for both interfaces from the received network reference signals. The control of the Layer 1 functions, especially the activation/deactivation procedures at the U-interface, is carried out by the exchange of special 4-bit Command/Indication codes in the C/I channel (GCI Mode), or via the activation/deactivation registers (MICROWIRE Mode).

The ST5410 UID User's guide is intended to complement the ST5410 data sheet. SGS-THOMSON follows a policy of continuous development and improvement of its range of products. The resultant changes are described in updates of the Data Sheet, the latest copy of which, obtainable from the reader's local SGS-THOMSON office, serves as the definitive product specification.

ST5410 ARCHITECTURE

1.1 General Description.

The ST5410 2B1Q U Interface Device is a complete monolithic transceiver for ISDN Basic access on twisted pair subscriber loops, typical of public switched networks. The device is fully compatible with both the ANSI T.1 601-1988 U.S. and CSE-C32-11 French specifications.

Basically the ST5410 provides an interface between a 2B1Q ANSI Basic rate U-Line signal and either a General Circuit Interface (GCI) or MICROWIRE/Digital System Interface (uW/DSI).

In both cases the two B voice/data channels and the D message channels are transferred transparently in both directions.

The U Reference signal also contains additional control and status information, eg. Layer 1 Activation/Deactivation control and status information. This can be transferred reciprocally to/from a time-division multiplexed channel in GCI or the

Figure 1.1: Typical Applications of the ST5410

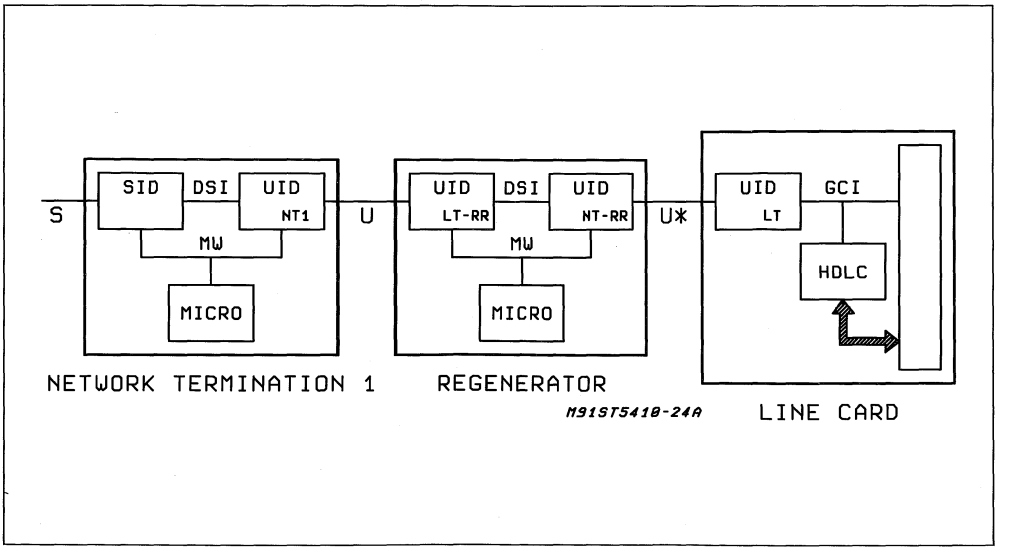
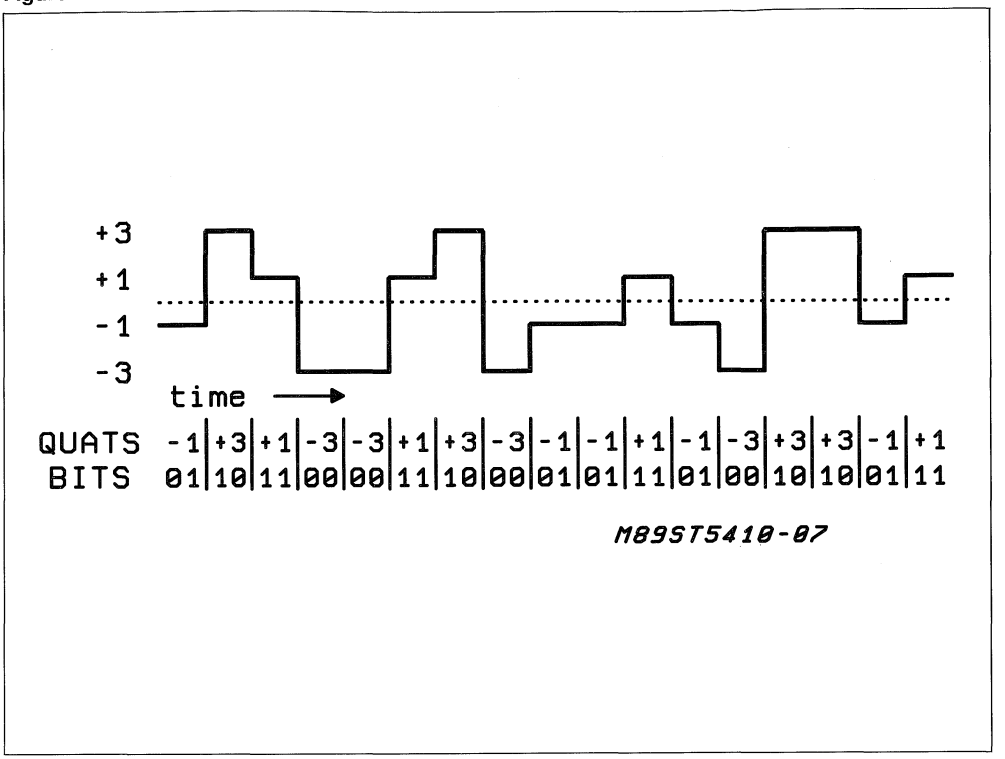


Figure 1.2: 2B1Q U-Line Code



serialcommunicationschannelintheMicrowire/DSI system.

Typical applications for the ST5410 are shown in figure 1.1 where the use of this chip in NT1, Repeater, and Central Office line card applications are shown.

1.2 The U Reference Point.

The U Reference Point provides a full-duplex service at Basic Rate on a single twisted metallic pair. The line-code is 2B1Q (2 binary, 1 quaternary), a 4-level pulse amplitude modulation code without redundancy (see figure 1.2). The line Baud rate is 80k/sec giving a transmission rate of 160 kbits per second in full duplex. The two B channels and the single D channel are time-multiplexed in a frame structure (figure 1.3) comprising 12 frames, each comprising 8 B1 bits, 8 B2 bits, and 2 D bits, together with 6 management control/status bits M, in a 1.5 millisecond period. Eight such frames are combined in a superframe of 12 milliseconds duration, the superframe start being denoted by an inverted 18 bit frame synchronization word (ISW) as shown in figure 1.4.

Figure 1.3: U-Line Frame Format

	← 1,5 milliseconds →		
FRAME	SW/ISW	12 X (2B+D)	M
Functions	Sync Word	2B+D	Overhead
# Quats	9	108	3
Quat Positions	1-9	10-117	118-120
# Bits	18	216	6
Bit Positions	1-18	19-234	235-240

Frames in the NT-to-Network direction are offset from frames in the Network-to-NT direction by 60 ± 2 quats.

Symbols & Abbreviations:

quat = quaternary symbol = 1 baud

−3, −1, +3, +3 = symbol names

2B+D = Customer data channels B_1, B_1 and D

SW = Synchronozation Word (9-Symbol Code) = + 3, + 3, − 3, − 3, − 3, + 3, − 3, + 3, + 3

ISW = Inverted (or complementary) Sync Word = − 3, − 3, + 3, + 3, + 3, − 3, + 3, − 3, − 3

M = M-Channel Bits, M_1-M_6

Figure 1.4: U-Line Superframe Format

Network-to-NT 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
A	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	uoa	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
B,C,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms).
All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat

act = activation bit (set = 1 during activation)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
dea = deactivation bit (set = 0 to announce deactivation)
uoa = (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

NT-to-Network 2B1Q Superframe Technique and Overhead Bit Assignments.

		FRAMING	2B+D	Overhead Bits (M_1-M_6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	ps_1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	ps_2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	sai	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

NT-to-Network superframe delay offset from Network-to-NT superframe by 602 quats (about 0.75 ms). All bits than the Sync Word are scrambled.

Symbols & Abbreviations:

"1" = reserve = reserved bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)
SW = synchronization word
ISW = inverted synchronization word
s = sign bit (first) in quat
m = magnitude bit (second) in quat

act = activation bit (set = 1 during activation)
ps_1, ps_2 = power status bits (set = 0 to indicate power problems)
ntm = NT in Test Mode bit (set = 0 to indicate test mode)
cso = cold-start-only bit (set = 1 to indicate cold-start-only)
crc = cyclic redundancy check: covers 2B+D & M4
1 = most significant bit
2 = next most significant bit
etc.
febe = far end block error bit (set = 0 for errored superframe)
sai = S/T interface activation bit. Used in restricted activation only (not used in this version)

Note: 8 x 1.5 msec Basic Frames 12 msec Superframe

1.3 DIGITAL INTERFACES.

The UID provides two selectable module interfaces, the DSI associated with the MICROWIRE serial control link, and the GCI parallel interface. The DSI interface is used for the transparent transfer of real-time user data on the B and D channels and also provides a number of optional framing structures, eg. GCI, COMBO etc. Interchange of low-speed Control and Status information is done via the MICROWIRE interchip serial link which provides for microprocessor control of various operational features of the device, eg. activation/deactivation control.
The alternative selectable Digital Interface, GCI, provides a single parallel interface for transparent exchange of 2B plus 1D Channel information, together with control and status information carried across the same interface.

1.3.1 The General Circuit interface (GCI)

The General Circuit Interface (GCI) is an interface specification developed jointly by Alcatel, Italtel, Plessey (now GEC Plessey Telecommunications Limited) and Siemens. GCI, used to control the subscriber line interface circuitry, is intended to serve as a standard interface between devices for subscriber access in ISDN environments.

Figure 1.5 shows the Frame structure of a GCI channel which comprises four sub-channels:

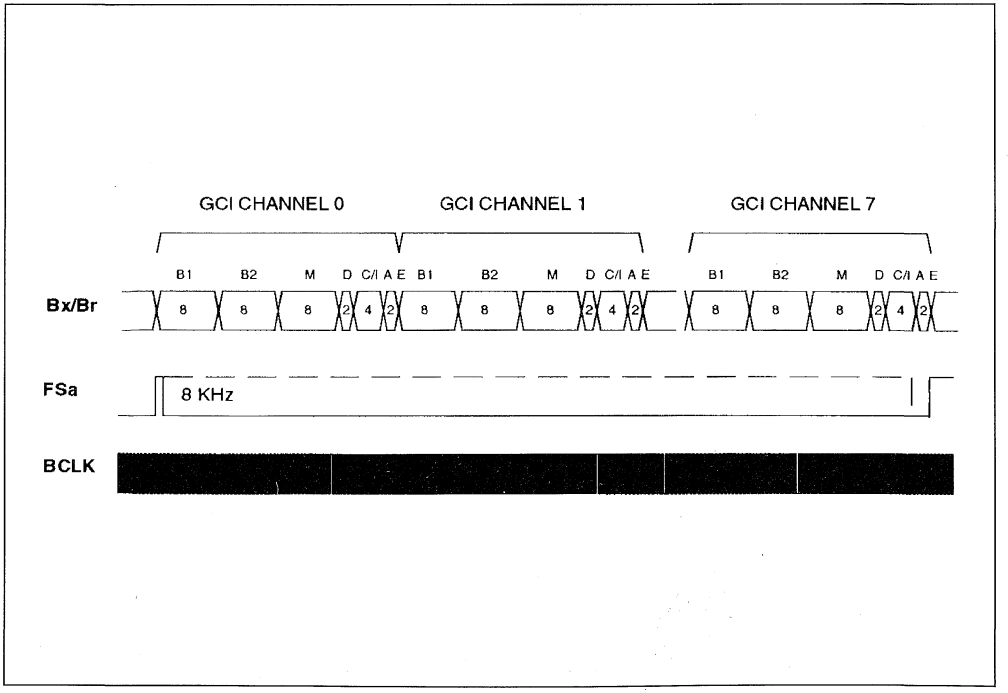
- B1 channel comprising 8 bits per frame
- B2 channel comprising 8 bits per frame
- Monitor channel comprising 8 bits per frame
- SC channel, structured as follows:
  - D channel of 2 bits per frame
  - C/I channel of 4 bits per frame
  - A bit associated with the Monitor channel
  - E bit associated with the Monitor channel.

The B1, B2, and D channels are used to transfer 2B+D basic access voice/data.

The Monitor channel is used to transmit maintenance information channel messages and to configure the UID. A serial protocol for byte exchange on the Monitor channel uses the E and A bits.

The C/I channel is used to exchange "real-time" primitives, such as activation/deactivation control and indication codes, between the UID and its associated controller, eg. ST5451 HDLC/GCI controller. Hence all activation/deactivation status indication is reported spontaneously on the C/I channel.

Figure 1.5: GCI Channel Frame Format



The interface is physically composed of 4 wires:

- Input Data wire: Bx
- Output Data wire: Br
- Bit Clock: BCLK
- Frame Synchronization: FSa

Data is synchronized by BCLK and FSa signals. FSa insures reinitialization of the time-slot counter at each frame beginning. The rising edge of FSa is the reference time for the first GCI channel bit of the first GCI channel.

Data is transmitted in both directions at half the BCLK frequency. Data is transmitted on the rising edge of BCLK and is sampled 1.5 periods after the transmit rising edge, on the falling edge. Unused channels are in the high-impedance state.

Note that up to 8 GCI channels may be connected on the same wires.

1.3.2 MICROWIRE (μW)

MICROWIRE is a serial communications interface from National Semiconductor. This system provides a standardized protocol which handles serial communications between a management control unity (microprocessor) and the configuration, command, status, and data registers of the UID.

All data transfers, consisting of two bytes corresponding to a device register address and a value, are shifted into the UID's Control Register via the CI pin. Similarly, two bytes representing a register address and the contents of that specified register are shifted out from the Status register via the CO pin. Each Data item, comprising a register address or a register value, shifts into CI on rising edges of CCLK, or out from CO on falling edges. Each such individual data item tranfer occurs when CS is pulled low for eight cycles of CCLK. Sixteen cycles of CCLK are hence needed to transfer a complete message.

An interrupt output, INT goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising edge CCLK edge after CS goes low.

If the microprocessor needs to send a command to the UID, it pulls CS pin low and transmits 16 bits of command on 16 rising edges of CCLK.

1.4 ACTIVATION/DEACTIVATION.

The subscriber loop between a customer terminal and a local office may contain several U-line sections as illustrated in figure 1.6, which relate to Version REVB. Note that REVA does not provide for a direct connection between UID's in RPT and NT1 equipments.
Each U-section may be terminated at both ends by an ST5410 UID chip. The UID chip at the subscriber end of each U-section (the Downstream devices) should be operated in NT mode, and the UID device at the opposite or Network end (the Upstream device) should be operated in LT mode.

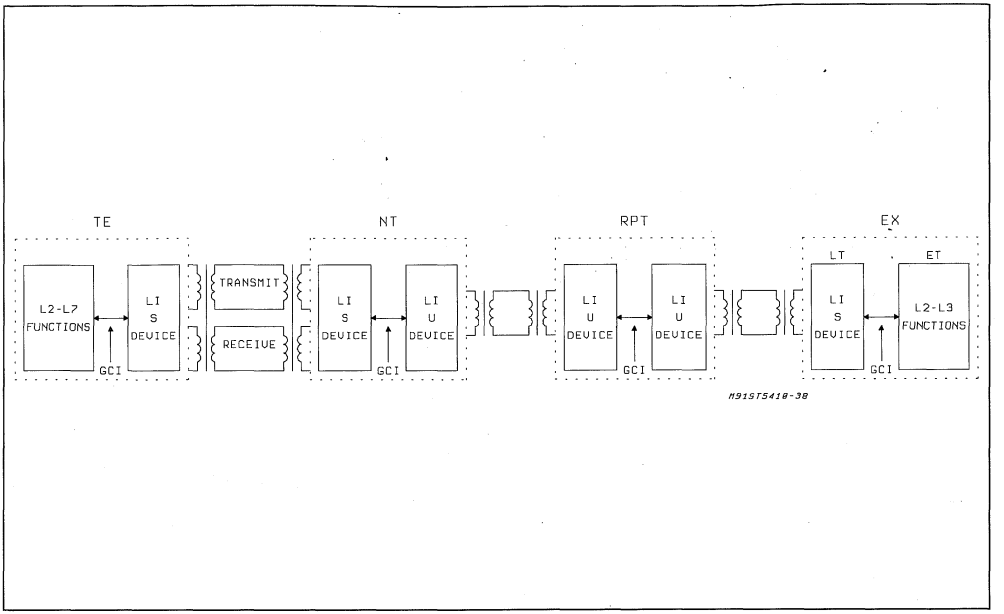
The U-line sections are connected by GCI or DSI and MICROWIRE links, which provide transparent transfer of the B and D channels. The transfer of activation/deactivation primitives between adjacent U-line sections may be accomplished by the use of a time-division multiplexed channel (GCI mode), or via the Management control unit (MICROWIRE mode). In order to provide transparent transfer of the B and D channels between subscriber and the Local Office all intermediate devices must be powered up and the signals must be synchronized at the bit, frame, and superframe (multiframe) levels. This is accomplished U-section by U-section, starting from the Network end. For each section and each direction of transmission the line must be equalised and echo-cancellation control algorithms converged. On completion of this phase of the subscriber loop Activation suitable synchronized signals and control/status may be transferred to the adjacent downstream U-line section via the GCI/DSI link as mentioned above. This Activation procedure may be initiated in response to requests originating either from the Network or User end of the Subscriber Loop.

The reverse process of Deactivating or powering down the Subscriber Loop proceeds in the same direction from Network to User but may only be initiated by the Network.

Deactivation may take place upon command or induced by fault conditions, eg. loss of power in an intermediate device, or loss of signal or loss of synchronization. In this case the Management Control unit in the affected section may issue error-status signals which travel downstream to the user, successively deactivating the U-line devices, and also upstream to the Local Office.

Both the Activation and Deactivation processes require the transmission of command and status information. Between adjacent U-line sections these primitives are implemented by means of 4-bit codes which are transferred via the MICROWIRE or GCI links. The transfer of these primitives along a U-section may be implemented by bits in the M-channel, if fully synchronized, or otherwise by special signals, eg. dialling tones.

Figure 1.6: U-Line Sections in Subscriber Loop



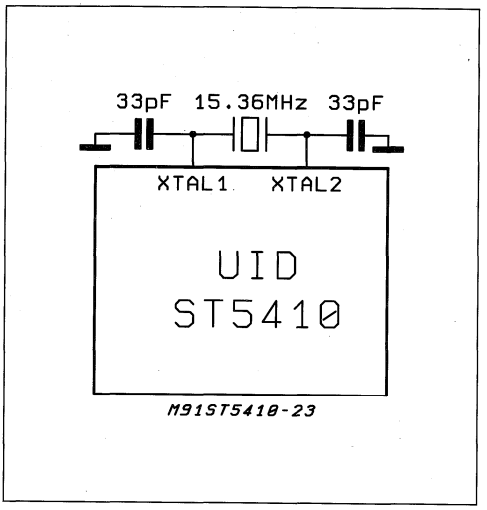
CHAPTER 2. Setting up the ST5410 UID Chip.

2.1 ST5410 UID LINE INTERFACE

This section deals with associated components which must be used in conjunction with the ST5410 to realize a complete system design. Choice of the appropriate components will lead to reliable equipment design and superior performance.

2.1.1. Crystal Oscillator

Figure 2.1: Clock Source for the ST5410



The clock source (figure 2.1) for the ST5410 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

2.1.2 Crystal Specification

The ST5410 UID clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36 MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of +/-100 ppm total to comply with the ANSI specification.

The crystal is connected between pin 21 (XTAL1) and pin 20 (XTAL2), with a total capacitance from each pin to ground of 30pF. The external capacitors must be mica or high-Q ceramic type. The use of NPO (Negative Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 30pF capacitance includes the external capacitor plus any trace and lead capacitance on the board.

2.1.3 ST5410 Crystal Requirements

Specification Details for the Crystal:

Nominal frequency of 15.36 MHz +/-50ppm.
Parallel resonant with Rs 20 ohms.
CO is < 7pF.
Manufacturer: Monitor Products Co. Inc., Oceanside, CA. 92054.

2.2 U-line TO ST5410 CIRCUIT INTERFACE

Two possible U-Line to interface circuits are shown in figure 2.2 where two alternative transformer couplings for the receiver input section are illustrated.

it is very important, for compliance with the ANSI and French standard, that the recommended line interface should be strictly adhered to. The channel response and dynamic range of this circuit have been carefully designed as an integral part of the overall signal processing system to ensure the performance requirements are met under all the specified loop conditions. Deviations from this design are likely to result in sub-optimal performance or even total failure of the system on some types of loops.

2.2.1 U-line Interface Transformer

Figure 2.3: U-line Interface Transformer.

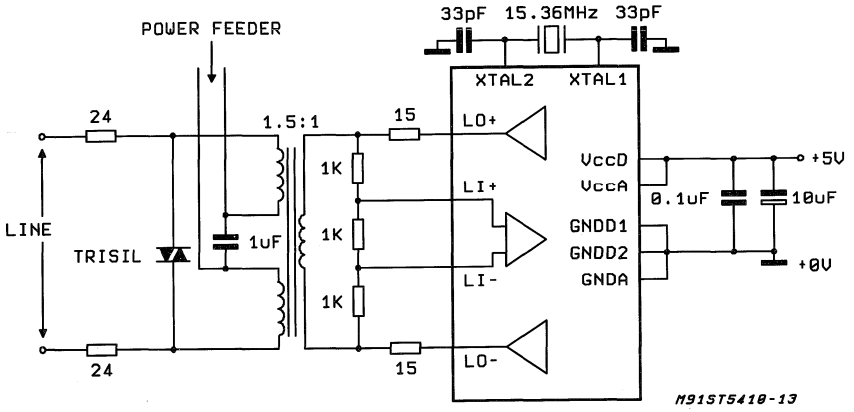
Specification details for the transformer, which is a highly critical component for effective use of the UID device are as follows:-

Turns Ratio:	Np:Ns = 1:1.5
Secondary Inductance	Lp = 27mH.
Winding Resistances:	30 ohms (2.25Rp + Rs) 10 ohms
Return Loss at 4kHz against 135 ohms:	26dB.

Saturation Characteristics:
THD -70dB when tested with 50mA D.C. through the secondary with a 40kHz sine-wave injected into the primary at a levelwhich generates 5V p-p into 135 ohms at the secondary.

Suppliers: SHOTT, PULSE ENGINEERING, AIE.

Figure 2.2: U-Line to ST5410 Interface



0.1% MATCHING IS REQUIRED TO MEET THE LONGITUDINAL BALANCE SPECIFICATION
THE 15ohm AND 1K RESISTORS IN THE INTERFACE CIRCUIT SHOULD BE 1%.

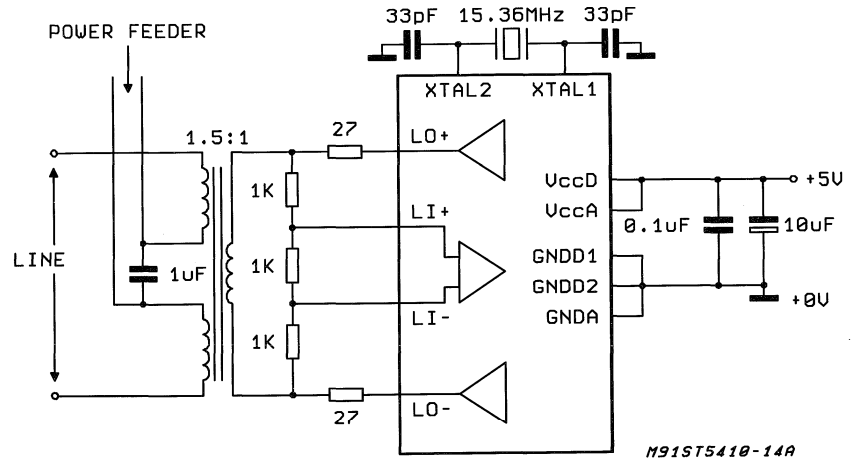
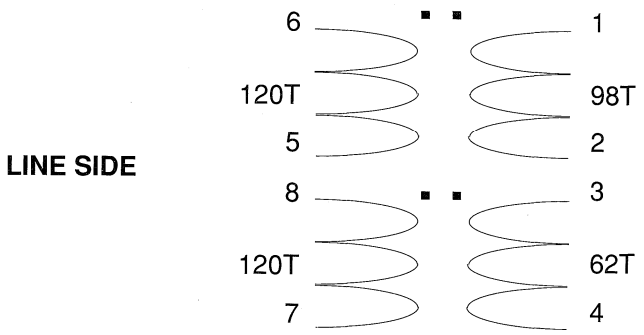


Figure 2.3: U-Line Interface Transformer



WINDING	NUMBER OF TURNS	WIRE GAUCE
1-2	98 Single	#34 AWG
6-5, 8-7	120+120 Bifilar	#36 AWG
3-4	62 Single	#34 AWG

WINDING	INDUCTANCE	RESISTANCE
1-2 + 3-4	12 mH	less than 5 ohms
5-6 + 7-8	27 mH	less than 10 ohms

Note: the split primary winding is designed to minimize leakage inductance.

2.3 MAIN MODES OF OPERATION.

Three main classes of mode operation may be identified:

a) NT/LT mode depending, respectively, on whether the U-Section is connected at the downstream (subscriber) or upstream (exchange) end of a U-line section.

b) Master/Slave mode depending on whether the bit (BCLK) and frame (FSa,b) timing references for the GCI/DSI interface are generated internally by the chip (and available as outputs) or are supplied by external circuits.

c) GCI/MICROWIRE mode: For the GCI Mode, access to the the configuration, data, and command/status registers of the device is made via the same link as the one used for (2B + D) date transfer. For the MICROWIRE Mode a serial communication link to an external controller provides for device register access.

2.3.1 NT/LT Modes of Operation.

The Activation/Deactivation requirements are different depending on whether the chip is connected upstream (LT) or downstream (NT) to the U-line section.

Similarly the framing, maintenance operation, clock recovery, and master clock transfer procedures are different for NT and LT modes of operation.

The appropriate mode may be selected by programming bit 6 of Configuration Register CR2 to 1 (NT mode) or 0 (LT mode).

2.3.2 Master/Slave Modes of Operation

In Slave mode the bit-rate (BCLK) and frame-rate (FS) signals for the digital interface (DSI or GCI) are supplied externally. In Master mode these signals are generated internally, and are synchronized to clock reference signals recovered from the line. This Master mode is significant only when NT mode is selected.

Selection of the required timing mode is accomplished in GCI mode by setting pin 27 (MO) High for Master or LOW for Slave modes.

In MICROWIRE mode, bit 1 (CMS) of configuration register CR1 selects the Master mode of operation when CMS = 1, or the Slave Mode when CMS = 0. When Master Mode is selected bits 3, 4, and 5 of Configuration Register CR1 are used to select one out of several options for the BCLK frequency.

2.3.3 GCI/MICROWIRE Modes of Operation.

In both these modes the B and D channels are transferred transparently. In GCI the UID register values may be transferred in Time-Division Multiplex format on the same link. In MICROWIRE mode these values must be serially transferred to the external management control entity.

Selection of the appropriate mode is by means of setting pin 28 (MW) LOW for GCI mode and HIGH for for MICROWIRE mode.

2.4 AVAILABLE CONFIGURATIONs

2.4.1 GCI Modes

The three available configurations for GCI mode are illustrated in figure 2.4, and are as follows:

GCI: NT1: NT Mode, Master Mode.
NT1-2: NT Mode, Slave Mode.
LT: LT Mode, Slave Mode.

The device pin input and configuration register programming requirements for GCI mode may be summarized as follows:

GCI Mode Pin Selection Requirements.

Pin MW = 0 volts selects GCI mode.

Pin MO = 5 volts selects Master mode.

Pin MO = 0 volts selects Slave mode.

Note that in Master mode only, pin CLS (pin 17) determines one of two possible frequencies for the BCCLK clock output:

CLS = 5 volts gives BCLK = 1536 kHz.

CLS = 0 volts gives BCLK = 512 kHz.

GCI Mode Configuration Register Programming Details.

Note that in Master mode (ie. when MO = 5 volts) the circuit is always in NT mode. For Slave mode the value of the NTS bit, CR2(6), specifies NT or LT operation.

NTS = 1 selects NT mode.

NTS = 0 selects LT mode.

Note that in NT mode the pin 22 output (SFS) is always an output. In LT mode, the specification of SFS pin as an input or as an output is determined by the value of SFS bit, bit CR2(7).

SFS = 1 selects SFS (pin 22) as output from the free-running Transmit Frame counter.

SFS = 0 selects SFS (pin 22) as an input that synchronizes the Transmit Frame counter.

2.4.2 MICROWIRE Modes

The three available configurations for MICROWIRE mode are illustrated in figure 2.5 and are as follows:

MICROWIRE/DSI: NT1: NT Mode, Master Mode.
NT1-2: NT Mode, Slave Mode.
LT: LT Mode, Slave Mode.
TEST: LT Mode, Master Mode

MICROWIRE Mode Pin Selection Requirements.

Note that in MICROWIRE mode the role of several pins is changed. Thus in GCI mode pin 27 served to define clocks as inputs or outputs (ie. Master/Slave specification). In MICROWIRE mode pin 27 serves as a Chip Select input for enabling the serial MICROWIRE input/output via the CI and CO pins. These latter input/outputs are effected via pins 18 and 19 respectively, and pins 17 and 26 are used for the MICROWIRE serial I/O clock input and Interrupt respectively.

Pin 7 is used in MICROWIRE for an additional 8kHz Frame Signal, Fsb, which defines the start of the frame on the Br output.

Because of these changes, selection of the various MICROWIRE options is for the most part effected by configuration register programming. However, the following pin assignment must be made.

Pin MW = 5 volts selects MICROWIRE mode.

MICROWIRE Configuration Register Programming Details.

Selection of Master or Slave mode is effected by setting the value of the CMS, Clock Master Select, bit, CR1(1), as follows:

CMS = 1 selects Master mode.

CMS = 0 selects Slave mode.

Selection of NT or LT mode is effected by setting the value of the NTS, bit, CR2(1), as follows:

NTS = 1 selects NT mode.

NTS = 0 selects LT mode.

Note that in NT mode the pin 22 output (SFS) is always an output. In LT mode, the specification of SFS pin as an input or as an output is determined by the value of SFS bit, bit CR2(7).

SFS = 1 selects SFS (pin 22) as output from the free-running Transmit Frame counter.

SFS = 0 selects SFS (pin 22) as an input that synchronizes the Transmit Frame counter.

In the Configuration Register CR1, valid for MICROWIRE only, the values of bits FF1 and FF0 determine the operating MICROWIRE format, as follows.

FF1	FF0	FORMAT
0	0	Format 1
0	1	Format 2
1	0	Format 3
1	1	Format 4

Also, in the Configuration Register CR1, valid for MICROWIRE only, the values of bits CK2, CK1, and CK0 determine the BCLK output frequency when DSI clocks are outputs.

CK2	CK1	CK0	BCLK Frequency
0	0	0	256kHz
0	0	1	512kHz
0	1	0	1536kHz
0	1	1	2048kHz
1	0	0	2560kHz

2.5 ST5410 DPLL SYSTEM.

The ST5410 contains two digital PLL's. Both these PLL's are used in LT Mode, whereas only a single unit is used in NT mode.

2.5.1 The DPLL System in NT Mode.

When the device is in NT Mode, synchronization is locked on the line side bit stream. This requires the use of one DPLL only (DPLL1), which is used to recover the bit clock and act directly on the sampling instant of the RX line signal. The phase error information is obtained from the decision feed-back equalizer in order to insure a sampling point that gives an optimal signal to noise ratio.

In the design of this unit care has been taken to minimize the amplitude of the discrete jumps of phase amplitude which would cause inacceptable noise in the echo canceller and the decision feedback amplifier. This has been accomplished by organizing the VCO as a ring oscillator with each stage yielding a 3.4 ns phase amplitude step. Note that only 65 ns steps would be obtainable using a 15.36Mhz clock.The stability of the ring oscillator is

assured by locking it to the crysal output using an analog PLL.

2.5.2 The DPLL System in LT Mode.

When the device is in LT Mode, the DPLL1 locks the device clock to the backplane 8kHz reference signal. The transmit signal is then synchronized to this clock, but the receive signal will be delayed because of the line round trip delay.The second DPLL (DPLL2) is used to effect his a proper sampling instant for the received signal at the analog to digital conversion point. The phase error for DPLL2 is also obtained from the decision feedback amplifier.

Cristal deviations from nominal frequency, provided they are within specification, will be compensated by the VCO. Note that this system handles jitter as specified in the ANSI spec.

Figure 2.4: GCI Modes of Operation

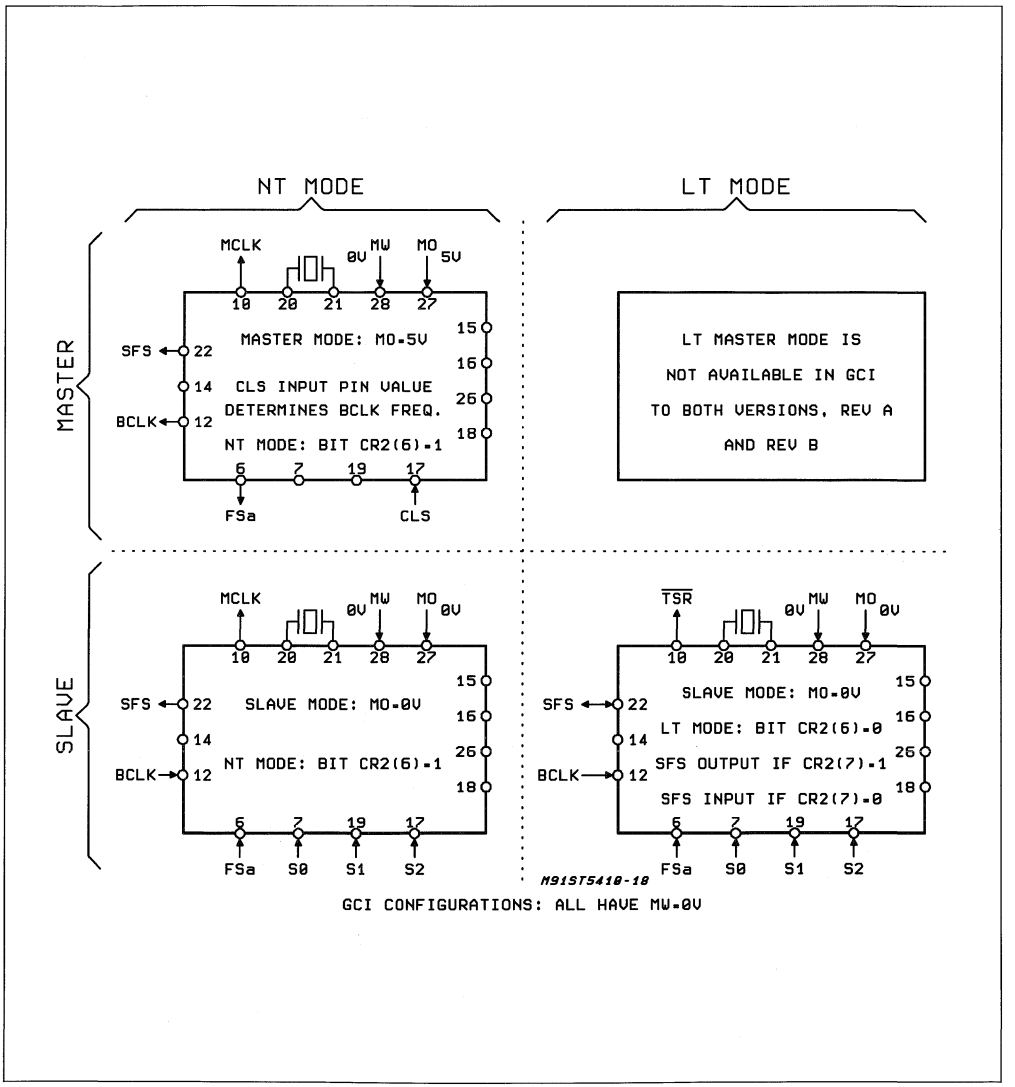
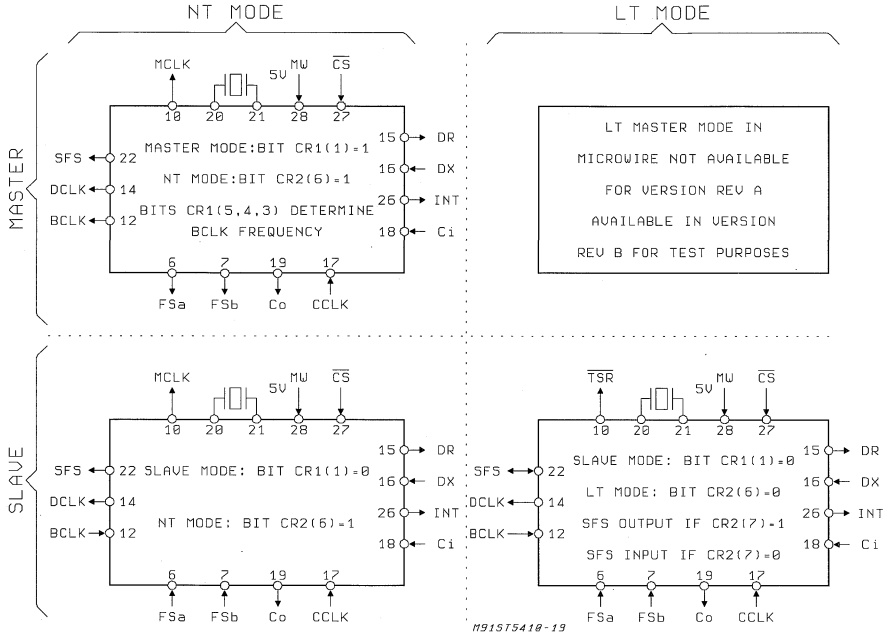


Figure 2.5: MICROWIRE Modes of Operation



MICROWIRE CONFIGURATIONS: ALL HAVE MW=5V

CHAPTER 3 Programming Principles for MICROWIRE/DSI Mode.

3.1 The MICROWIRE Control Interface.

The MICROWIRE interface, enabled when the MW control input is set equal to 1, enables the values of the UID's internal registers to be read or written by a control microprocessor. The MICROWIRE interface comprises 5 signals:

CI:	Data in
CO:	Data out
CCLK:	Data clock input
CS:	Chip Select Input
INT:	Interrupt Request

The microprocessor transmits serial data to the UID device on the CI line and the UID responds by sending data to the microprocessor via the CO line. Both data in and data out are synchronized by the same clock signal, CCLK, supplied by the microprocessor which hence acts as a MICROWIRE Master.

The serial transmission of data on CI and CO is enabled when the CS input is LOW. The appropriate sequence of CS, CCLK, and CI signals is generated in a service routine which is invoked by the microprocessor in acknowledgment of an interrupt request, INT, received from the UID device.

The MICROWIRE interface may be used to load initial values in the UID configuration registers using a write cycle, or to readback values contained in configuration and status registers. Read cycles are used to transfer values in the UID status registers to the external controller.

A Read or Write cycle always comprises the transmission of two bytes. The Data clock, CCLK, must be pulsed 16 times while CS is low. Data on the CI input is shifted into the UID serial Receive Input register on the rising edge of each CCLK pulse. At the same time, each data bit, apart from the first of such data bits, is shifted out from the UID serial Transmit register to the CO output on the falling edge of each CCLK pulse. Note however, that the first data bit is outputted on CO on the falling edge of the Chip select signal, CS.

Effectively each data transfer comprises simultaneous read and write operations. Dummy read or write operations are used when the UID or the microprocessor, respectively, have no useful information to transfer. If the UID has no message to send it forces the CO output to deliver sixteen zeroes (dummy read), when responding to a microprocessor write operation. Similarly, a message comprising 16 zeroes applied to input CI constitutes a NOP (No Operation) or dummy write operation. This may be used if the microprocessor has no write message to transmit while responding to a UID read request.

A write cycle is invoked in order to initialize or change the value stored in a UID register. The write request takes the form of a 2-byte (16-bit) message on the CI input comprising an 8-bit register address with the read/write bit (bit 0) set to 0. The following 8-bits define the value to be loaded into the specified UID register.

Read cycles are required when the UID has information to send to the external microprocessor controller. This may arise either because a status change has occurred in the UID chip or because of a readback request by the microprocessor. If the MICROWIRE interface is currently active, as indicated by an active Low value of signal CS, the event is stored on an interrupt queue, organized in order of priority.

Otherwise if CS is inactive High, the message is assembled in the UID Transmit register in the form of an 8-bit register address followed by an 8-bit data value. The UID then asserts the INT output to the active low condition. On recognizing this interrupt the microcontroller can service the read request by supplying the appropriate MICROWIRE CS, CO, and CCLK signals. Note that INT may only be asserted if CS is High.

Readback requests may be made at any time for any of the following registers: OPR, CR1, CR2, CR3, TXB1, TXB2, RXB1, RXB2, TXD, RXD, BEC1.

The readback request takes the form of a 2-byte (16-bit) message on the CI input comprising an 8-bit register address with the read/write bit (bit 0) set to 1. The remaining 8-bits have don't-care values which the user is recommended to set to 0.

The four remaining UID registers, RXACT, RXM4, RXEOC, and RXM56 cannot be accessed by readback requests from the external controller. These registers are updated internally by the UID after verification over 0, 1, 2 or 3 frames and then generate a MICROWIRE interrupt, as follows:

RXACT, after each status change of the state machine.

RXM4, at each validated change of a RXM4 spare bit according to the OPR verification programming.

RXEOC, at each validated change of the received eocmessage according to OPR verification programing.

RXM56, at each validated change of RXM56 spare bit orfebe or nebe bit according to OPR verification programming.

Interrupts may originate from 6 possible sources, ie. the 5 registers mentioned above together with a

readback request. These requests are stacked in an interrupt queue and are serviced in the following order of priority:

1. RXACT
2. RXM4
3. RXEOC
4. RXM56
5. BEC1
6. Readback register.

Provided that the CS line is high, the highest priority pending source is selected and the UID Transmit Shift register is loaded with the register address (1st byte) and register contents (2nd byte). At this point the output INT may be asserted Active Low and the transfer effected by the microprocessor interrupt service routine. On completion, after CS has been returned from Active Low to Inactive High, the next highest pending interrupt source will cause the UID Transmit register to be loaded and cause INT to be asserted.

Note that the capacity of the interrupt queue is six events where each event corresponds to a pending interrupt from one of the 6 sources listed above in order of priority. Multiple messages from any one source cannot be queued even if the stack is not full since each position in the interrupt queue is assigned to a unique register source and a fixed priority level. Thus if a readback request occurs at a time when a previous readback request is still queued awaiting service then the new request will displace the earlier one which will hence be lost.

If the UID needs a Read cycle (status change has occurred in the UID or a read-back cycle has been requested by the microprocessor controller), it pulls the INT output low (provided always that CS is High).

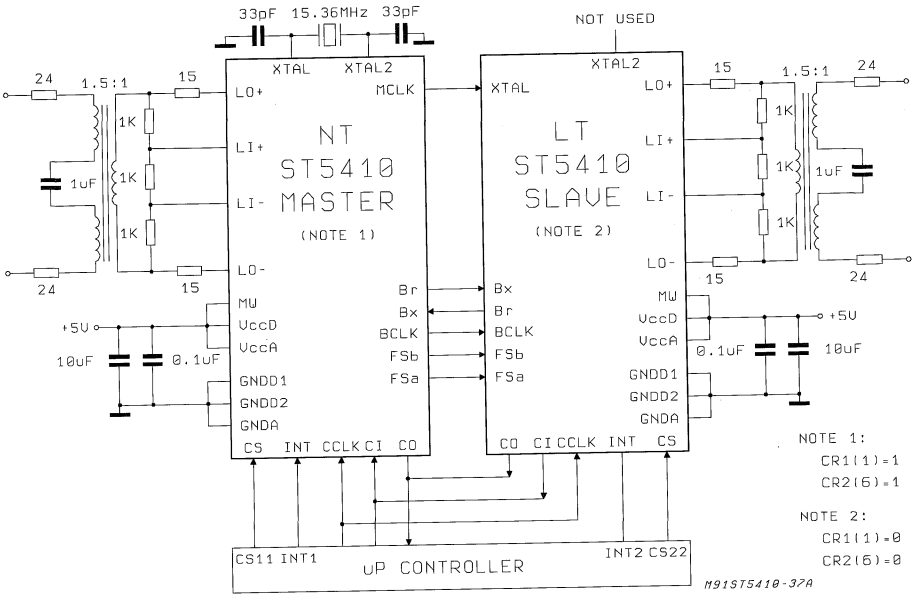
The microprocessor controller responds by loading a register address and data (or NOP) into its serial I/O register and driving the Chip Select output low. The UID then responds to CS low by setting the INT line high.

Note that a further high to low transition on INT is not allowed when CS is low (the UID waits for CS high if a pending interrupt occurs while CS is low). Effectively therefore each MICROWIRE message transfer is of length two bytes, corresponding to the read of, or write to, a single UID register.

3.2 MICROWIRE Controller Design Example.

An outline schematic for a MICROWIRE control application in a Repeater is shown in figure 3.1. In this example the two UID devices in MICROWIRE mode are connected via their MICROWIRE Serial Input/Output lines to a suitable microprocessor.

Figure 3.1.: MICROWIRE Design Example



3.2.1 Microprocessor Requirements.

A suitable microprocessor is one which contains an 8-bit serial I/O unit conforming to the following specification:

8-bit shift register with serial data input and output connections, MSB first.

Serial Shift Clock output synchronized to the serial data, with data changes occurring on falling edges, and input data latched internally on the rising edges of the clock. The IDLE state of the clock should be zero, eg. Mode a) in figure 3.2.

UID Chip select output available through specification of a parallel port I/O pin.

2 Interrupt channels (one for each UID circuit)

1-bit Software control of Shift Register IDLE/BUSY state.

Software polling facility for testing Shift Register IDLE/BUSY state.

A microprocessor conforming to the above general specification may be selected from the extensive SGS-THOMSON ST8/ST9 range.

3.2.2 UID Power-up State.

At switch-on time the ST5410 will enter the power-down, deactivated state in MICROWIRE mode since the MW input is hardwired to zero. The MICROWIRE interface is enabled even though all other circuits including the master oscillator are inactive. The internal status and configuration registers of the ST5410 will be set to their default values.

At power-on the microprocessor should be programmed to enter a RESET routine which will perform various initialization tasks relating to the configuration of the microprocessor . This should include the INIT routine described in Section 3.2.3 which initializes the Serial I/O circuit.

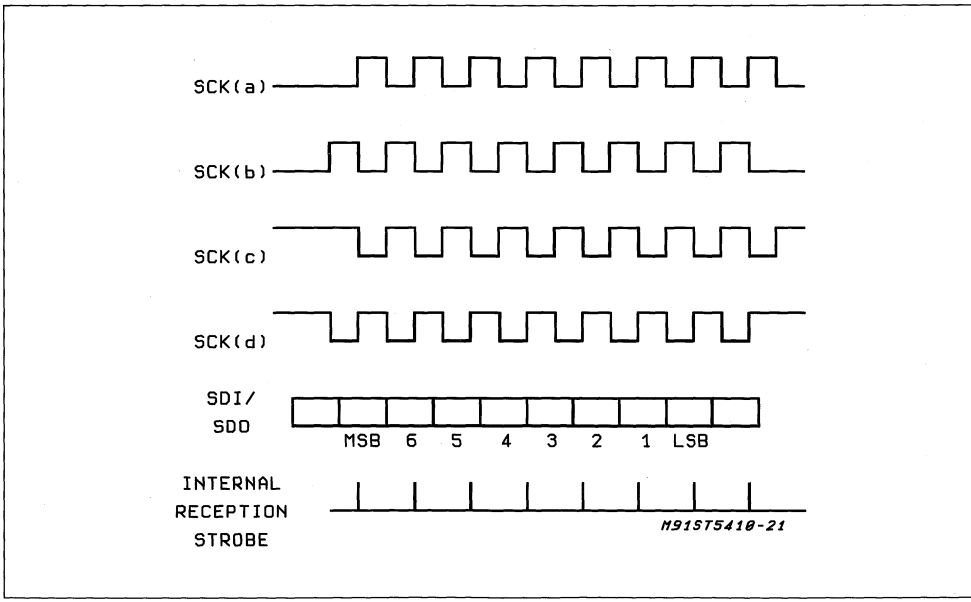
A series of successive calls may then be made to the Write routine described in Section 3.2.4 in order to initialize the ST5410 circuits by loading the configuration registers, OPR, CR1, CR2, CR3, and, in DSI MICROWIRE Format 3, TXB1, TXB2, RXB1, RXB2, together with TXD and RXD. The Power-up state of the UID circuits may then be invoked by loading the Activation code, PUP (0000), in the Activation Command Register.

3.2.3 The MICROWIRE INIT Routine.

An outline of a suitable routine to be included in the microprocessor Power-up (RESET) routine is shown in figure 3.3 in flow-diagram form.

After disabling both UID Interrupt lines the control/configuration registers of the microprocessor are loaded to specify input/output connections for

Figure 3.2: Clock-edge Phasing



the five MICROWIRE signals, CI, CO, CCLK, CS, INT. If necessary, depending on the microcontroller used, parallel-port pins may be assigned to some of these signals.

The Serial I/O operational mode and clock signal freqency and format should then be specified. This would normally include the specification of the division ratio for the CPU clock, the number of bits (eight) shifted out in each operation before the IDLE flag is set, and the clock edge phasing and Idle state characteristics, eg. mode a) in figure 3.2. Additionally, one bit of the Serial I/O should be assigned to IDLE/BUSY identification. in a typical case, this bit would be set by software to initiate the shift operation, and reset by hardware when the operation is complete.

Finally, for both UID circuits, input Read and output Write buffers should be defined and cleared, and Register tables defined and initialized to the standard Reset values.
The format of these buffers and the Register Tables are shown in figures 3.4, 3.5, and 3.6. The two UID alines can then be enabled and a return made to the Main Program.

Figure 3.3: MICROWIRE INIT Routine

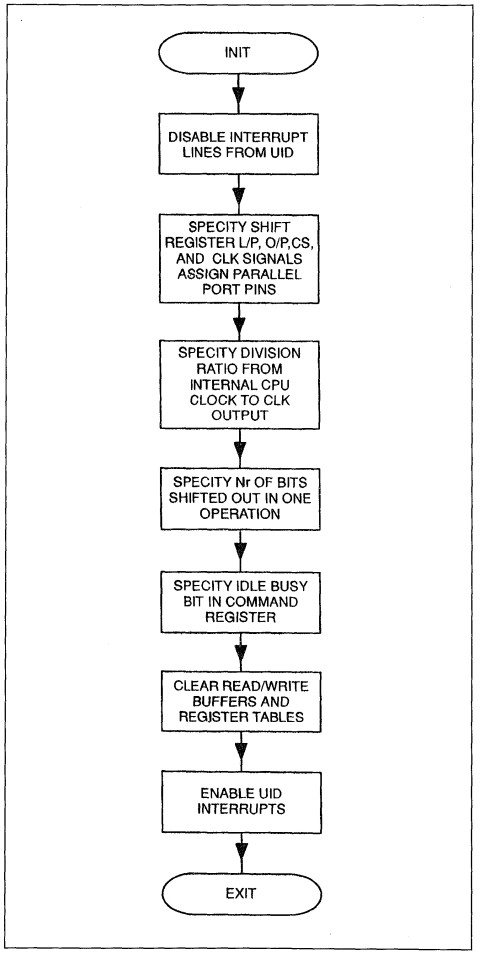


Figure 3.4: Send Buffer

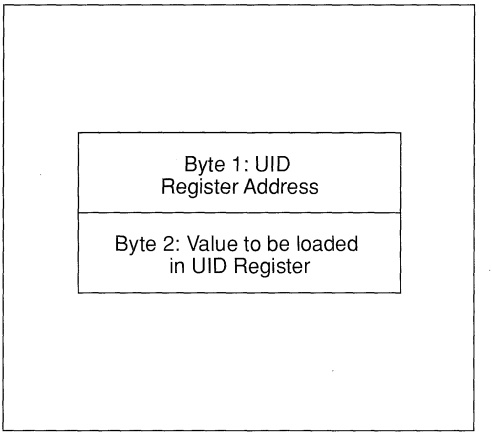
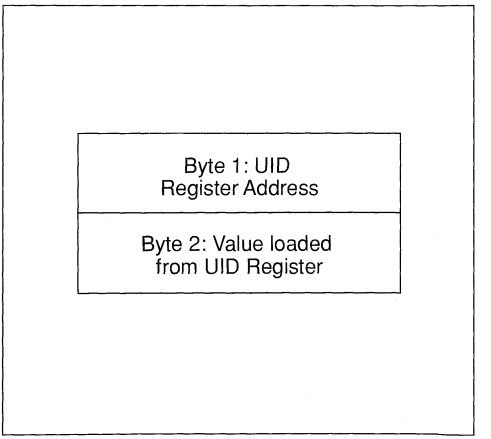


Figure 3.5: Receive Buffer



3.2.4 The MICROWIRE Readback and Write Routines.

The Readback and Write routines both operate in the same way by loading the Send buffer and then making a call to the Write request routine, WRITEREQ, described in Section 3.2.5 (see figures 3.7 and 3.8).

For a Write operation the Send buffer should be loaded with the register address (1st byte) and the value to be loaded (2nd byte). For a Readback request both bytes of the Send buffer should be cleared to zero, equivalent to a NOP operation.

Figure 3.6: Register Table.

OPR
CR1
CR2
CR3
TXB1
TXB2
RXB1
RXB2
TXD
RXD
RXN4
RXN56
RXACT
BEC1
RXEOC

3.2.5 The MICROWIRE WRITEREQ Routine.

The WRITEREQ subroutine is called from the Readback and Write routines, as well as from the Read Interrupt routine (Section 3.2.6). Its organization, illustrated by the flow-diagram of figure 3.9, is as follows.

The 1st byte of the Send buffer (register address) is loaded into the Serial I/O unit Shift Register, and the Chip Select output is set to Active Low. The BUSY/IDLE flag is set to one, initiating the serial shift of the contents of the shift register onto the CI line, and the replacement of the shift register contents by the serial byte on input CO.

The BUSY/IDLE flag is tested until a 0 value is returned, indicating the completion of the 8-bit shift operation. The contents of the shift-register are loaded into the first byte of the Receive buffer, and the second byte of the Send buffer (register value) is loaded into the shift-register.

The BUSY/IDLE flag is set to 1, and tested until it returns a value of 0. At this point the shift-register contents have been shifted out and replaced by the byte received on the CO line.
This latter byte is then loaded into the 2nd byte of the Receive register.

Finally, the Chip Select signal, CS, is returned to the inactive High level, and a return from subroutine can be effected.

Figure 3.7: READBACK Routine

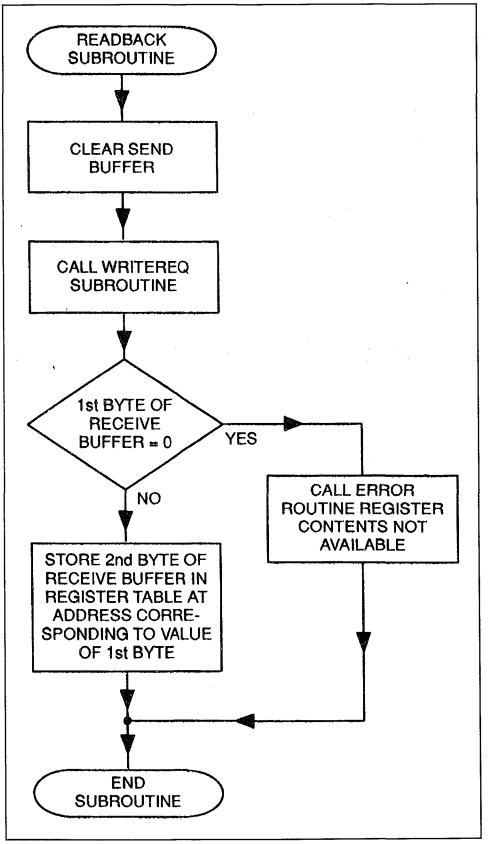


Figure 3.8: WRITE Routine

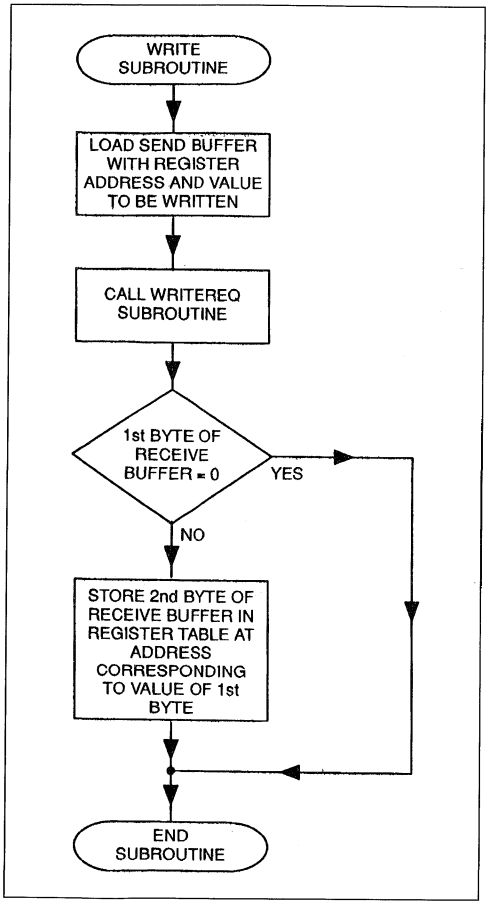
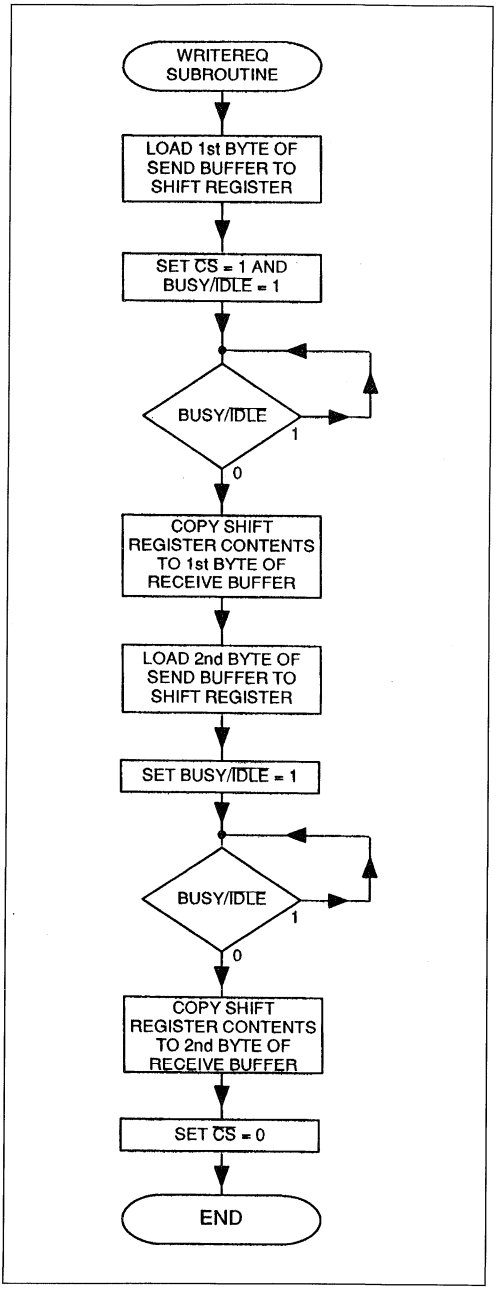


Figure 3.9: WRITEREQ Routine



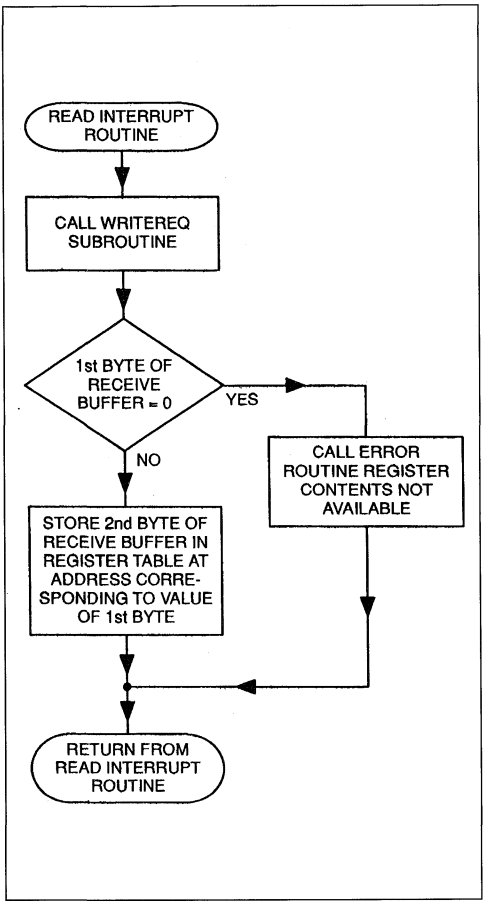
3.2.6 The MICROWIRE Read Interrupt Routine.

The Read Interrupt routine, illustrated in figure 3.10, disables the UID interrupt inputs and clears the Send buffer.

A call is then made to the READREQ subroutine which executes a dummy write (NOP) to the respective UID circuit, and returns with the Receive buffer containing the register address and contents received from the CO line.

At this point the Register Table is updated, using the 1st byte of the Receive buffer to direct the contents of the 2nd byte to the appropriate location. The UID interrupts can then be re-enabled, and a return from interrupt made.

Figure 3.10: MICROWIRE READ INTERRUPT Routine



CHAPTER 4 Programming Outlines for GCI Mode.

4.1 The GCI Data/control Interface.

The GCI is a European standard interface for the interconnection of dedicated ISDN components in the different equipments of the subscriber loop. This interface, enabled when the MW control is set equal to 0, enables the values of the UID's internal registers to be multiplexed with the B1, B2, and D channels into 4 contiguous bytes per 8 kHz frame. A maximum of 8 such GCI channels may be multiplexed into a composite GCI frame with a combined bit-rate from 256 kb/s to 3088 kb/s.

In a typical example, eg. Line card or TE application, the UID GCI interface is connected to the GCI port on an SGS-THOMSON ST5451 HDLC device. The HDLC device is connected via its 8-bit wide parallel port to a microprocessor which may thus access control and maintenance information conveyed by the GCI interface.

The microprocessor may thus be used to process Activation/deactivation or Embedded Operation signals transmitted by the C/I or Monitor channels respectively.

The GCI interface comprises four wires:

Bx:	Transmit Data to line
Br:	Receive Data from line
BCLK:	Bit clock at 2 cycles/bit
FSa:	Frame Synch. at 8kHz.

Each individual GCI channel using a bandwidth of 256 kbit/s comprises the following channels time-division multiplexed in an 8 kHz frame (see figure 4.1):

B1 channel:	8 bits per frame
B2 channel:	8 bits per frame
M Monitor channel:	8 bits per frame

SC Signalling/Control channel structured as follows:

D channel:	2 bits per frame
C/I channel:	4 bits per frame
A/E bits:	Monitor channel control bits.

The GCI Monitor channel (byte 3) is used to access all the UID command registers with the exception of the Activation Control Register, and all the Status Registers with the exception of the Activation Indication Register. Each access to or from one of these registers requires a 2-byte message transfer. The message format specifies the register address as the first byte and the contents of the register as the second byte.

Monitor channel transmit messages may arise either because a status change has occurred in the UID chip or because of a readback request received via the Monitor channel. If the GCI Monitor channel is currently active, the message is assigned a priority and stored in a message queue.

If no messages of higher priority are awaiting transmission the message is transmitted in the form of an 8-bit register address followed by an 8-bit data value. The message is transmitted subject to the A/E bit protocol as described in Section 4.1.1.

Figure 4.1: GCI Channel Frame Structure

Octet 1 8	Octet 2 8	Octet 3 7 6 5 4 3 2 1 0	Octet 4 1 2 4 3 2 1 1 1	
B1	B2	M	D	C / I A E

Octet Number	Mnemonic	ISDN Description
1 2	B1 B2	Two 64Kbit/s Voice/Data channels. For ISDN basic access these channels carry the 2B user channels transparently.
3	M	Monitor channel used for operation and maintenance facilities
4	SC	Signalling and Control channel.
	D bits	These two bits carry the 16Kbit/s ISDN basic access D channel transparently.
	C /I bits	This 4 bit Command / Indication channel is used for activation/deactivation of ISDN lines and control functions.
	A, E	These bits are used to control the transfer of information on the Monitor Channel.

Readback requests may be made at any time for any of the following five registers:

OPR, CR1, CR2, CR3, BEC1.

The following registers are not available for readback: RXM4, RXM56, RXACT, RXEOC. The values of these registers are updated after verification over 0, 1, 2, or 3 cycles and generate GCI Monitor Channel Messages which are stacked on the message queue in the following order of priority:

1. RXM4
2. RXEOC
3. RXM56
4. BEC1
5. Readback register.

Note that verified changes in the contents of register BEC1 generate a queued channel message of priority level 4. Furthermore, the contents of this register may be polled at any time using a readback request, in which case the request is queued at priority level 5.

A further point is that, it is not a change in the contents of BEC1 which induces an interrupt message but the fact that the error counter 1 gives an overflow.

The contents of the Activation register are transferred continuously in the C/I channel. Any change in the value of this register does not set up a GCI Monitor Channel Message. This register is also not available for readback.

Note that the capacity of the message queue is five events where each event corresponds to a pending interrupt from one of the 5 sources listed above in order of priority. Multiple messages from any one source cannot be queued even if the stack is not full

since each position in the message queue is assigned to a unique register source and a fixed priority level. Thus if a readback request occurs at a time when a previous readback request is still queued awaiting service then the new request will displace the earlier one which will hence be lost.

4.1.1 Monitor Channel Exchange Protocol in GCI Mode.

The exchange protocol is identical for both directions. The sender uses the E bit to indicate that it is sending a Monitor byte while the receiver uses the A bit to acknowledge the received byte. Note that all messages are two bytes long, even if other messages are queued on the message stack.

When no Monitor Channel message is being transferred the E bit and the A bit in the reverse direction are both inactive High.

To initiate a transmission the transmitter must first verify that it has received the A bit High for at least 2 consecutive GCI frames. It then sends the first byte in the Monitor channel with the associated E bit set to Low, indicating that this is the first byte in a two byte message. The receiving device verifies receipt of the same byte in 2 consecutive frames and sends acknowledgement by setting A Low for at least two frames. If verification of consecutive identical bytes is not possible the receiver aborts the message by sending A Low for only one frame.

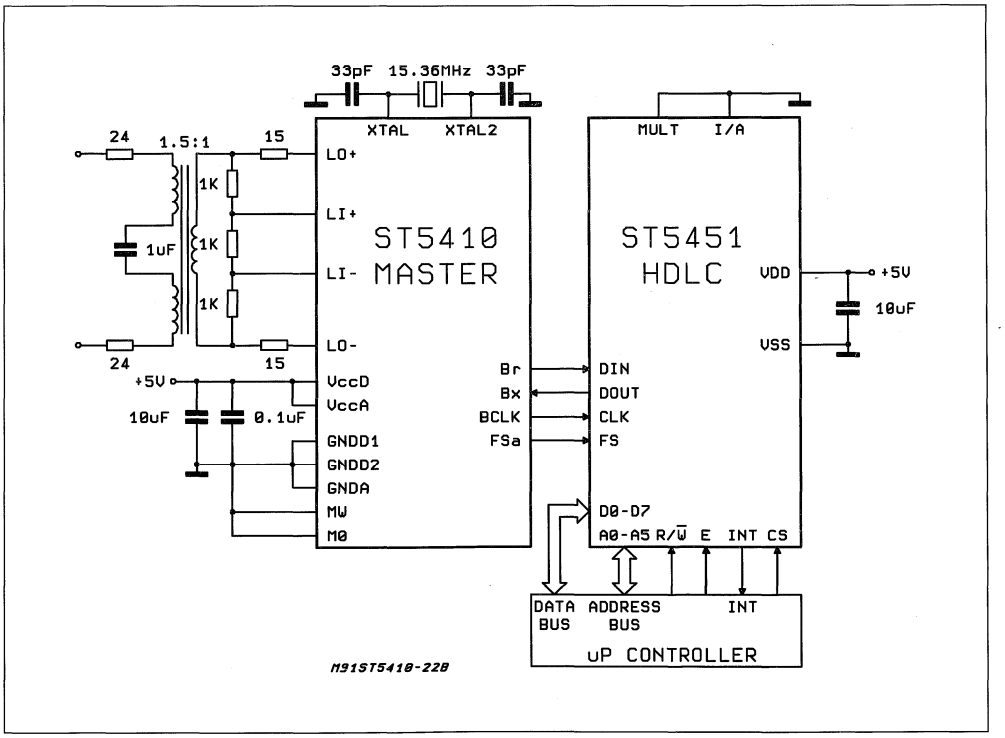
On detecting the acknowledgement the transmitting device then sends the second (and final byte) in 2 consecutive frames (or until acknowledged or aborted). The E bit is set to High indicating that this is the 2nd byte of a 2-byte message. The receiver acknowledges receipt of consecutive identical frames by setting A Low for one frame only before setting A High. Alternatively the message is aborted with a load of by retaining A at the High level.

If an abort message is received at any time the sending device will again send the complete message until receiving an acknowledgement.

4.2 GCI INTERFACE DESIGN EXAMPLE.

In this example (figure 4.2) the UID GCI interface is connected to the GCI port on an SGS-THOMSON

Figure 4.2: GCI Design Example



ST5451 HDLC/GCI controller. The HDLC/GCI device is connected via its 8-bit wide parallel port to a suitable microprocessor. A suitable microprocessor is one which offers 8-bit parallel access via a bus which can be operated either in Motorola-compatible mode (1 Data Strobe, 1 R/W Control) or Intel-compatible (separate Read and Write Strobes).

The address lines may be either separate or multiplexed.

4.2.1 Microprocessor Requirements.

Suitable microprocessors include the SGS-THOMSON ST9, and members of the INTEL 51 and 188 families. An SGS-THOMSON ST9, used in Motorola-compatible mode would show the following characteristics:-

6-bit address lines permitting access to the HDLC/GCI registers in the address range 00H to 3FH.

8-bit parallel data bus.

1-bit CS Chip Select line.

1-bit R/W control line.

1-bit DS Data Strobe line.

1-bit E Enable signal.

2 Interrupt lines (INT1 and INT2).

The ST5451 HDLC/GCI device services two separate GCI Monitor and C/I channels.

For each channel there is an associated Interrupt Status Register, ISTA1 and IAST2, and Mask Register, MASK1 and MASK2. There are also two registers, ISTA0 and MASK0, which contain Global Interrupt Status and Masking bits for the two Monitor channels.

Confining our attention to Monitor Channel 1 and associated registers ISTA1 and MASK1, there are six conditions relating to events in this channel which can raise an interrupt which will be signalled by an appropriate bit in ISTA1, provided that the corresponding bits in MASK1 have been reset to zero.

At the same time the global interrupt status bit, EXI1, in ISTA0 will be set to 1 provided that the corresponding bit, Bit 2, in MASK0 has been set to 0.

4.2.2 The HDLC/GCI Register Set.

Figure 4.3: HDLC/GCI Interrupt Status Registers

	it Positions							
	7	6	5	4	3	2	1	0
ISTAO	RME	RPF	RFO	XPR	XDU	EXJ1	EXJ2	O
ISTA1	O	O	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1
ISTA2	O	O	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

In detail the relevant ST5451 registers are the following:

ISTA0, Interrupt Status Register 0: Device address = 20H.

Relevant Bits:

ISTA0(2), EXI1: this bit indicates a Global Channel 1 interrupt specified by the contents of register ISTA1.

ISTA0(1), EXI2: this bit indicates a Global Channel 2 interrupt specified by the contents of register ISTA2.

ISTA1, Interrupt Status Register 1: Device address = 21H.

Bit 7: unused: Value = 0.

Bit 6: unused: Value = 0.

CIC1 Command/Indicate Change (Bit 5).

A change in the value of CIC1 is detected.

EOM1 End of Message 1 (monitor channel) (Bit 4).
MON1 has received an end of message

XAB1 Monitor Transmit ABORT (Bit 3).

The received byte has not been detected in two successive frames.
MON1 has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register 1 ready (Bit 2).
A byte has been received in register MONR1.

RAB1 Receive ABORT (Bit 1).
MON1 received an ABORT from the remote transmitter.

XMR1 Transmit Monitor Register 1 ready (bit 0)
A byte can be stored in register MONX1.

MASK0, Interrupt Mask Register 0: Device address = 20H.

Each interrupt source in ISTA0 register can be selectively masked by setting to "1" the corresponding bit in MASK0.

MASK1, Interrupt Mask Register 1: Device address = 21H.

Each interrupt source in ISTA1 register can be selectively masked by setting to "1" the corresponding bit in MASK1.

MONX1/0, Monitor Transmit Register 1: Device address = 2EH.

The value written in MONX1/0 is transmitted in the outgoing Monitor Channel according to GCI transfer protocol. An XMR1 interrupt indicates when MONX1 is again available.

MONX1/1, Monitor Transmit Register 1: Device address = 2FH.

The value written in MONX1/1 is transmitted in the outgoing Monitor Channel according to GCI transfer protocol, and is followed by an End of Message signal. An XMR1 interrupt indicates when MONX1 is again available.

MONR1, Monitor Receive Register 1: Device address = 2EH.

The value read from MONR1 gives the value of the byte received in the monitor channel according to the GCI transfer protocol. RMR1 interrupt indicates when a new byte is available in MONR1 register.

Initialization routines for Monitor channel or C/I channel read or write involve the enabling of the appropriate input interrupts after clearing or setting up the input/outout buffers.

For a read operation the appropriate interrupts and corresponding masking bits RMR1, EOM1, and XAB1 (bits 2,4, and 3 in registers ISTA1 and MASK1) are cleared. In addition the global interrupt and masking bits, EX1 (Bit 2) in ISTA0 and MASK0 are cleared. For a C/I channel read operation bit CIC1 (bit 5) in ISTA1 and the corresponding MASK1 bit should be cleared.

For a write operation the required bits to be cleared include RAB1 and XMR1 (bits 0 and 1) in registers ISTA1 and MASK1. A write operation to the C/I channel does not involve the interrupt mechanism since the C/I codes are transmitted continuously once the C/I register has been loaded.

4.2.3 Common Interrupt Service Routine.

The organization of a common interrupt service routine for the control microprocessor is shown in figure 4.4. The service routine first copies the HDLC/GCI device interrupt status registers, ISTA0, ISTA1, and ISTA2, into the microprocessor memory before clearing these registers to zero. The routine then clears the microprocessor interrupt pending bit and proceeds to poll the copied values of the HDLC/GCI interrupt status bits, EXI1, EXI2, etc. A complete test of all the possible interrupt sources is carried out, according to the organization shown in figure 4.4, and a branch is taken to the appropriate servicing routine for each bit which is set to 1. If any further HDLC/GCI interrupt events occur during this time they will set the corresponding bit in the ISTAn registers. This will cause a further microprocessor interrupt to occur when the return from the routine of figure 4.4 is taken.

4.2.4 Monitor Channel Transmit Routines.

In the example illustrated by figures 4.6, 4.7, and 4.8 each transmission is limited to the transfer of a new value to one only UID register. For this purpose we use a transmit buffer (figure 4.5) comprising a 1 byte header containing the number of bytes to be sent (two in our example, ie. register address and register contents), the number of bytes actually sent, and a Transmission Channel available flag bit, T. A value of T = 1 indicates that the Transmit Buffer is currently in use. The routine to transmit a register message should hence first test the T-flag and proceed only if T = 0.

In the initialization routine (figure 4.6) the RAB1 and XMR1 interrupts are masked in the MASK1 register. The transmit buffer is loaded with the destination register address (byte 2) and the value to be loaded (byte 3), and the 1 byte header is initialized (no. of bytes to send = 2, no. of bytes already sent = 0, and T-flag = 1). The RAB1 and XMR1 interrupts are then enabled and a return from interrupt is effected.

When the Transmit registers in the HDLC/GCI device are available an interrupt RAB1 occurs and a call to the Transmit routine (figure 4.7) is made. The transmit buffer header is examined to see if 0, 1 or 2 bytes have been sent. In the first two cases the appropriate byte is copied from the buffer to either MONX1/0 or MONX1/1 respectively, and a return from interrupt is then taken.

If the byte counts, number to be sent and number already sent,are equal then the transmission of the two byte message is complete. In this case the Transmit buffer header can be cleared (in particular, T-flag = 0), and a return from interrupt made.

Figure 4.4: Common Interrupt Service Routine

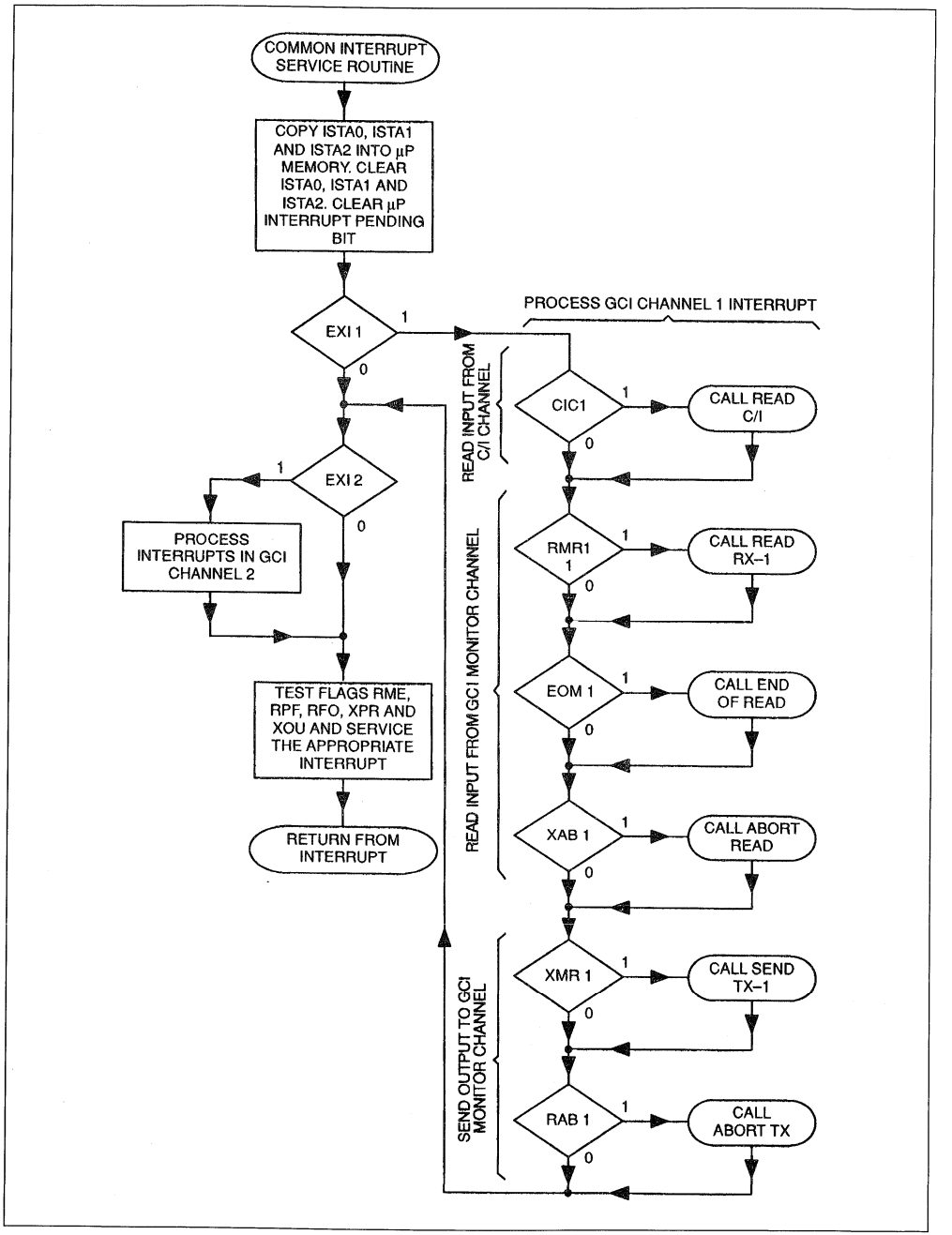


Figure 4.5: Transmit Buffer

BIT POSITIONS

7	6	5	4	3	2	1	0

Number of Bytes to Send	**Number of Bytes to Send**	**T**	**X**	**X**	**X**
lst Byte to Transmit Register			UID Address		
2ed Byte to Transmit be loaded in USD			Value to Register		

If the transmission of the 2-byte register message via the GCI Monitor Channel to the UID device is aborted, the interrupt bit RAB1 is set and the Transmission Abort Routine of figure 4.8 is entered. In the example shown an attempt is made to retransmit the current byte by reloading it into MONX1/0 or MONX1/1 as appropriate. As an alternative the Send buffer could be reinitialized and the entire message retransmitted.

Figure 4.6: Transmitt Initialization Routine

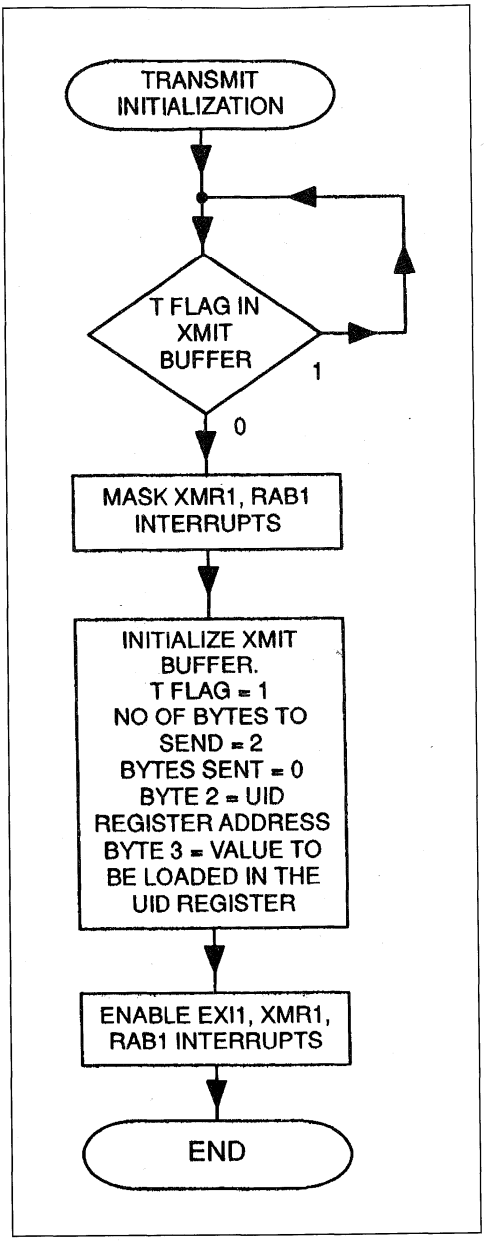


Figure 4.7: Routine to Transmit 1 Byte.

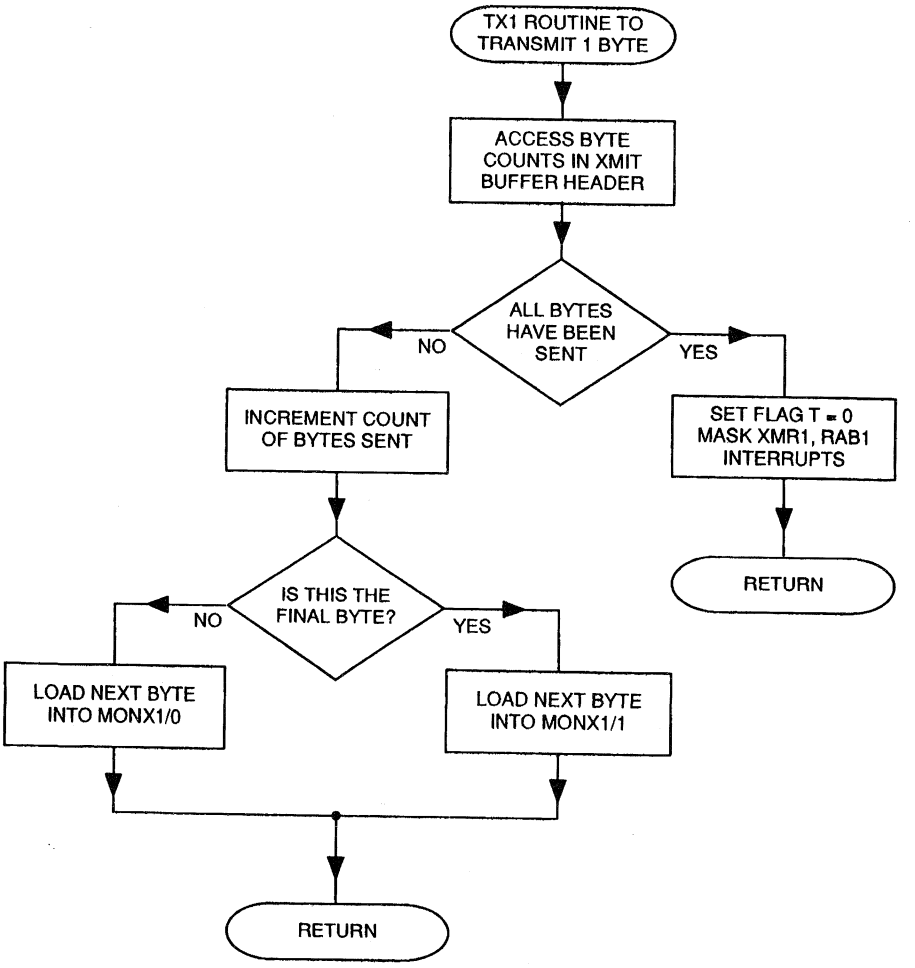
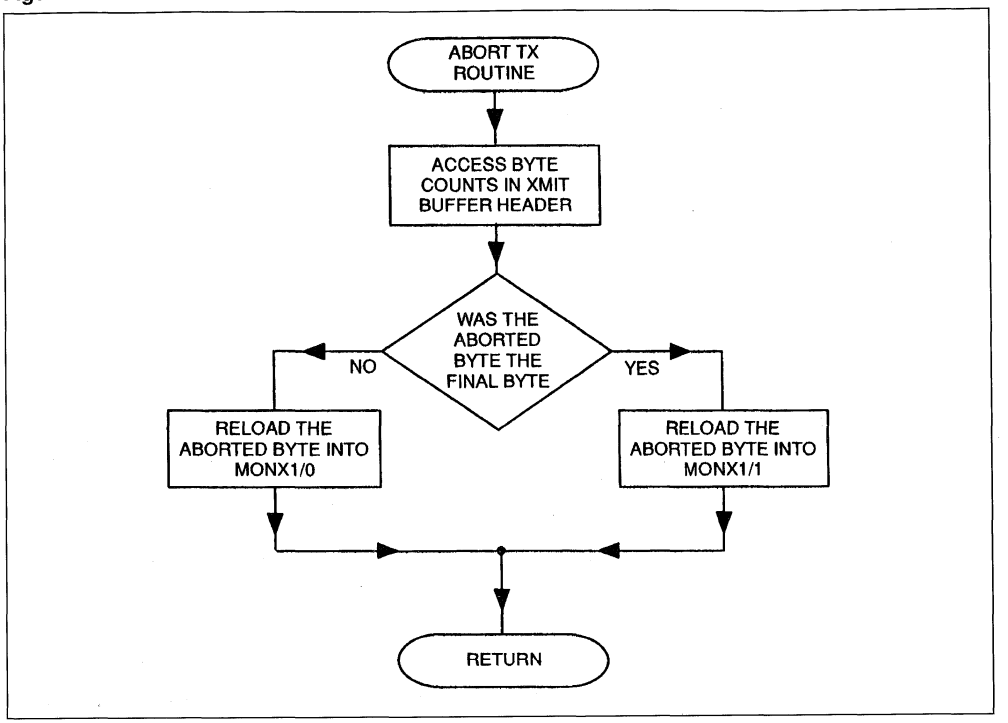


Figure 4.8: Routine for Transmit Abort



4.2.5 Monitor Channel Read Routine.

Figure 4.9: Receive Buffer.

Bit positions

7	6	5	4	3	2	1	0

Byte Count	X	X	F	X	X	X
Ist Byte Reccived.				UID Register Address		
2nd Byte Reccived.				UID Register Contents		

A suitable Monitor Channel Read Routine needs to handle read calls originating from the UID device as well as readback requests originating from the control microprocessor.

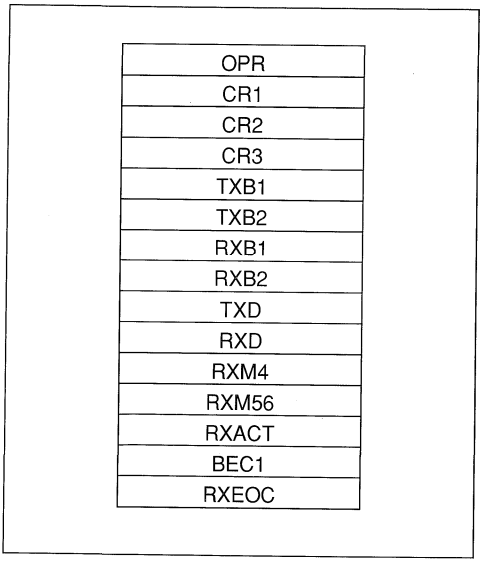
Readback requests are used to access the contents of the following eleven UID registers, OPR, CR1, CR2, CR3, TXB1, TXB2, RXB1, RXB2, BEC1, TXD, and RXD. In order to read the contents of one of these registers a Monitor Channel message of two bytes must be transmitted to the UID device. The first byte contains the register address (with Read/write bit = 1) and the second byte is all zeroes. The UID device responds by generating a 2-byte message, register address byte and register content byte, and placing this message on the message queue. The UID will also place a message on the message stack each time a validated change of contents occur corresponding to U-line activity in any of the following registers: RXM4, RXM56, BEC1, or RXEC0.

Messages are transmitted via the GCI Monitor channel in the following order of priority:

1) RXM4
2) RXEOC
3) RXM56
4) BEC1
5) Readback Register

The lowest level of priority, Readback Register, refers to one of the eleven registers mentioned above. Note that only one readback register request may be pending at any given time since a new readback request will displace any previous pending request on the message stack.

Figure 4.10: UID Register Table.



As the GCI Monitor Channel becomes available the highest priority pending request is transmitted to the HDLC/GCI device. Each byte is verified by the Monitor Channel protocol (Section 4.1.1) and then raises an interrupt to the controlling microprocessor. The organization of the microprocessor interrupt routine must reflect the following considerations: a) read interrupts can be produced from two sources, ie. the UID processor status registers and readback requests, and b) these messages may occur at any time and hence the corresponding interrupts must be permanently enabled.

One possible organization to handle this situation is illustrated in figures 4.11, 4.12, 4.13, and 4.14. A 15-byte UID register table (figure 4.10) is established in the microprocessor RAM in which a copy is maintained of the latest updated UID register contents. In addition a 3-byte Receive buffer (figure 4.9) is set up containing the number of bytes received since the last EOM, End of Message. The second and third bytes respectively contain the latest register address (odd byte number) and register contents (even byte number).

After each read of consecutive odd-numbered and even-numbered bytes comprising a register read the result is written into the register table. On completion of the Read operation the second byte of the register buffer may be used as a pointer to place the third byte in the register table.

4.2.6 Read Initialization Routine.

A suitable Initialization routine is shown in figure 4.11. This routine may be called to initialize a READBACK operation, or it may be used as a general initialization routine to enable autonomous requests from the UID device to be serviced. In both cases the Receive buffer must be cleared; for a READBACK operation the Transmit buffer must also be initialized with byte 2 specifying the address of the register to be read.

The first byte of the read buffer contains a 2-bit field which stores the number of bytes received since the last End of Message, EOM.

This byte also stores a Buffer Available Flag, F, which is reset to zero when a Read operation commences and is maintained at zero until the buffer contents have been transferred to the Register Table. This flag serves also to indicate to any higher-level routine attempting to access the Register Table that an update of one of the entries in this table is in process.

4.2.7 Read Interrupt Routine.

The organization of the basic interrupt routine to read a single byte is shown in figure 4.12. This routine first increments the count received field in the Receive Buffer. Note that this count value can then be used to identify the received byte as a register address or as a value.

After copying the received byte into the Receive Buffer in the appropriate location a return from interrupt is effected.

4.2.8 End of Message Interrupt Routine.

An End of Message received from the UID device confirms that the 2-byte message stored in the Receive Buffer represents a correctly verified Monitor Channel message. The END_OF_READ routine (figure 4.13) uses the second byte stored in the

Figure 4.11: Read Initialization Routine.

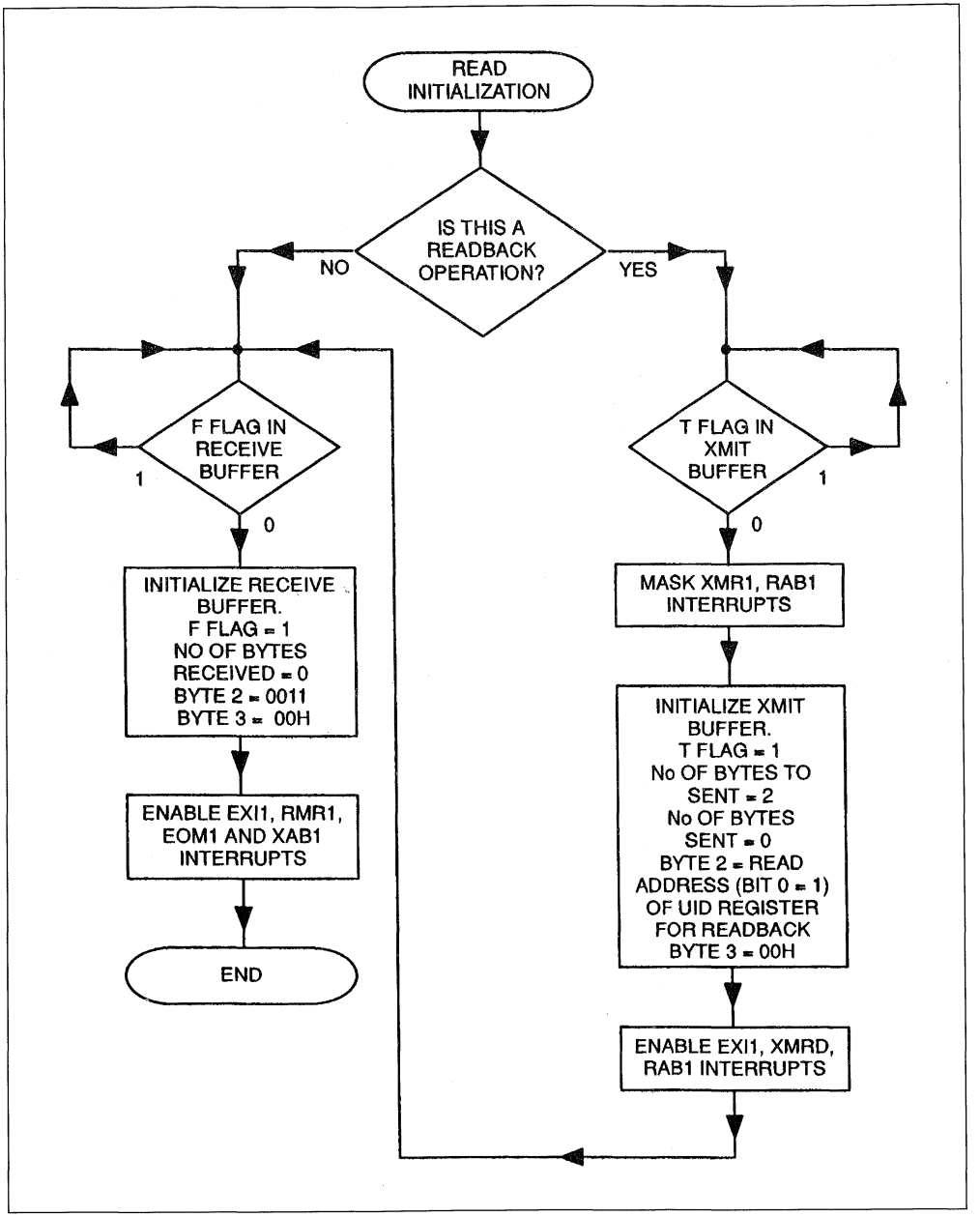
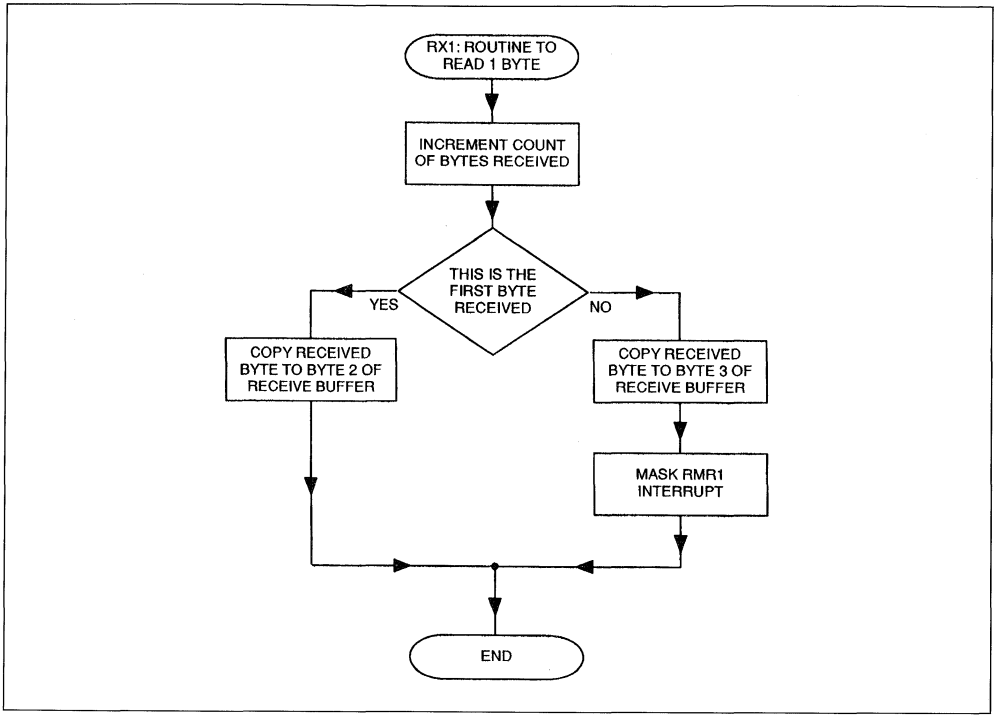


Figure 4.12: Routine to Read 1 Byte



Receive buffer as a pointer to place the third byte in the Register Table as a verified updated value of a UID register value. The routine then clears the Receive Buffer, and resets the first byte (count to zero, and Buffer Available flag to 0). After re-enabling the receive interrupts, RMR1, EOM1, and XAB1, a return from interrupt may be made.

4.2.9 Read Abort Interrupt Routine.

This routine (figure 4.14) is entered if a Monitor Channel Abort signal is received. In this case the Receive Buffer first byte is reinitialized (count = 0, F = 0), and any values stored in the second or third bytes discarded. A return is effected after re-enabling the receive channel interrupts.

4.2.10 Read and Transmission of C/I bytes.

The contents of the CIX1 register in the ST5451 HDLC/GCI device are continuously transferred in the C/I channel of the GCI interface. Hence the transfer from the microprocessor of a new C/I value to the UID device ACT register may be accomplished (figure 4.15) by a simple 8-bit transfer (normally with 4 leading "0" values) to CIX1.

A CIC1 interrupt may be used to capture a new C/I value received, validated, and loaded into register CIR1 of the ST5451 device. The associated interrupt service routine (figure 4.16) can be used to transfer the value directly into the Register Table at the location reserved for the Activation Register.

Figure 4.13: Routine for END–OF–READ

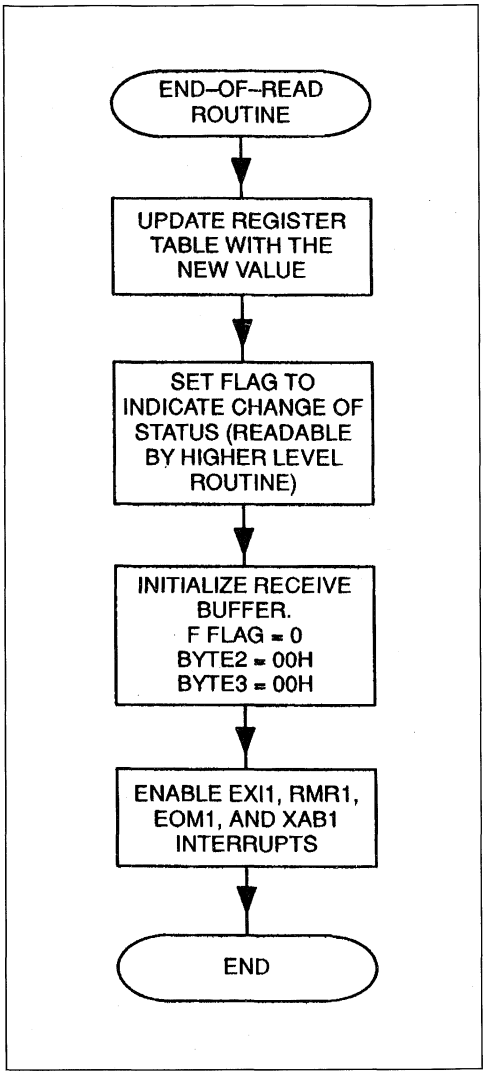


Figure 4.14: Read Abort Routine

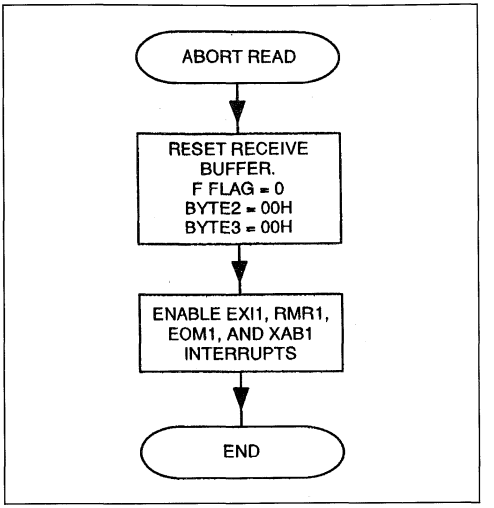


Figure 4.15: Routine to Send C/I Byte.

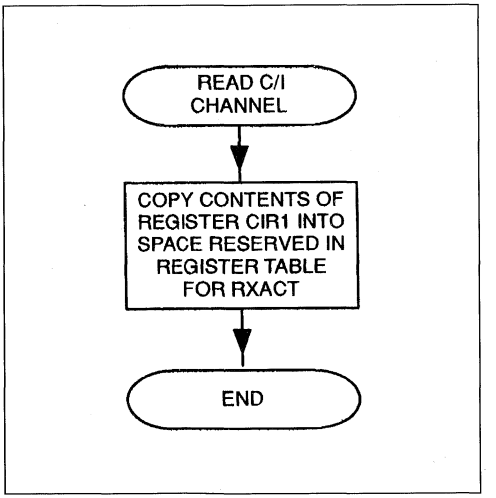
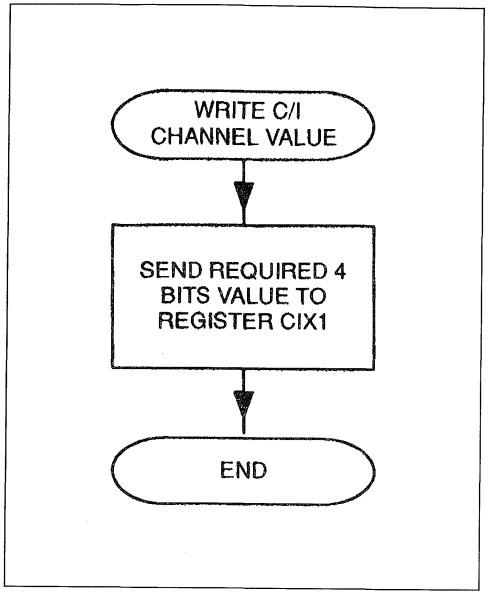


Figure 4.16: Routine to Read C/I Byte.



CHAPTER 5 Activation/Deactivation Level 2 Routines.

5.1 INTRODUCTION.

The ST5410 contains automatic sequencers for the complete control of the start-up Activation sequences in LT and NT modes as specified in the French and ANSI standards. Interaction with an external control unit requires only Activate and Deactivate Request commands, with the option of inserting breakpoints in the sequence for additional internal control allowing, for instance, easy design of a Repeater application.

Except for the Power up and Power down control features which are slightly different, the Activation/Deactivation procedures are identical in GCI and MICROWIRE modes, and the same command codes or indication codes are used. In MICROWIRE mode, Activation Control is done by writing in the Activation Control Register ACT and by reading the Activation Indication Register RXACT. In GCI mode, these registers are accessed directly by the Command/Indicate channels.

Activation/Deactivation State Machines for LT and NT modes are shown in figures 5.1 and 5.2 respectively.

The software design principles for external circuits capable of implementing the complete Activation/Deactivation handshake with the ST5410 internal state-machines are described in this chapter. Two main examples are chosen, corresponding to the ST5410 operating in GCI/LT and MICROWIRE/NT modes.

5.1.1 The Full Reset State (J1), LT Mode.

The Full Reset State (J1 in figures 5.1a/5.1b) is a state of the Finite State Machine Controller in which the UID device is neither sending nor receiving line signals. Note that the "signals" SL0 and SN0 represent null send and receive signals, respectively.

The ST5410 contains two circuit states (effectively sub-states of the Full Reset State) corresponding to Power Down and Power Up conditions.

Similar remarks apertain to the Full Reset State of the State Machine in NT mode (state H1 in figures 5.2a/5.2b).

5.1.2 The Power Down State.

In the power-down state all the internal circuits of the UID with the exception of the Line signal (TN) are inoperative and in a low power state. All digital outputs and the analogue Line outputs, Lo+ and Lo-, are in the low impedance state. The programmable registers all retain previously entered values, including any default values arising at Power Switch on.

The Power Down State may be entered in two different ways:-

a) At Power Switch on. In this case the configuration registers are loaded with their default values (refer to Data Sheet). In any subsequent attempt to activate the subscriber loop complete algorithms must be used to compute all DSP coefficient values, used for echo-cancellation and line-equalization. Hence only cold-starts are possible, requiring up to 15 seconds.

b) From the Power Up State using a PDN command. The PDN command has no effect on the contents of the internal registers. Hence, under certain conditions the adaptive circuit coefficient values are frozen at the values appropriate for the given subscriber loop. This ensures that the next Activation Request will automatically sequence through a warm-start procedure, which normally achieves complete loop activation within 300 msecs. The required conditions are firstly that the loop had previously been successfully activated and then deactivated, and secondly that power had subsequently been maintained uninterrupted in either Power-up or Power-down states.

Figure 5.1: Activation/Deactivation State Machine: LT Mode

EVENT	STATE NAME	Power Off	Full Reset	Alertg	Awake	EC Training	WAIT SN2	CHECK SN2	EC Covrg'd	SW Sync	ISW Sync	Active	Deact'n Alert'n	Tear Down	Pending Deact'n	Recv Reset
	STATE CODE	J0	J1	J2	J3	J4	J4. 1	J4.2	J5	J6	J7	J8	J9	J10	J11	J12
	TX	SL0	SL0	TL	SL0	SL1	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL2 dea = 1 act = 0	SL3 dea = 1 no change (*)	SL3 dea = 1 act = 1	SL3 dea = 0 act = 0	SL0	SL0	SL0
POWERON		J1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0	J0
ACTIVATION REQUEST (AR)		/	ST T5 J2	-	-	-	-	-	-	-	-	-	-	-	-	-
DEACTIVATION REQUEST (DR)		/	-	-	-	-	-	-	-	-	J9	J9	-	-	-	-
END OF TONE TL (3 ms)		/	/	J3	-	/	/	/	/	/	/	/	/	/	/	/
RECEIVED TONE TN and ACTIVATION REQUEST (AR)		/	ST T5 J3 AP	-	-	/	/	/	/	/	/	/	/	/	/	ST T5 STP T7 J3 AP
LOSS OF SIGNAL ENERGY		/	-	-	J4	-	-	J4.1	/	/	/	/	/	/	/	/
ECHO CANCELLER CONVERGED		/	-	-	-	J4.1	-	-	-	-	-	-	-	-	-	-
B-ASIC FRAME SYNC (SW)		/	/	/	/	/	/	/	J6	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	/	STP T5 J7 SYNC	-	-	-	-	-	-
RECEIVED act = 0		/	/	/	/	/	/	/	/	/	-	J7 EI	-	-	-	-
RECEIVED act = 1		/	/	/	/	/		/	/	/	J8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	/	J10 EI	J10 EI	-	-	-	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	/	/	/	/	ST T7 J12 EI	ST T7 J12 EI	ST T7 J12 EI	-	/	/	/
END OF THE LAST SUPERFRAME WITH dea = 0 (4th)		/	/	/	/	/	/	/	/	/	/	/	J11	/	/	/
EXPIRY OF TIMER (**) T5 (15 seconds)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	/	-	/	-	/	/
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	/	/	/	/	/	/	/	ST T7 J12	J1 D1	-
EXPIRY OF TIMER (**) T7 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	J1 D1
DETECTION OF SIGNAL ENERGY		/	-	-	-	-	J4.2	J5	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	J10 EI	-	-	-	-	-	-

(*) FAO command is needed to send act = 0
(**) When timer is enabled (default)

Figure 5.2: Activation/Deactivation State Machine: NT Mode

EVENT	STATE NAME	Power Off	Full Reset	Alertg	EC Training	WAIT SL	CHECK SL	EC Covrg'd	SW Sync	ISW Sync	Pending Active	Active	Pending Deact'n	Tear Down	TE Inactive	Recv Reset
	STATE CODE	H0	H1	H2	H3	H3.1	H3.2	H4	H5	H6	H7	H8	H9	H10	H11	H12
	TX	SN0 INFO0	SN0 INFO0	TN INFO0	SN1 INFO0	SN0 INFO0	SN0 INFO0	SN0 INFO0	SN2 INFO0	SL3 act = 0 INFO2	SN3 act = 1 INFO2	SN3 act = 1 INFO4	SN3 no change	SN0 INFO0	SN3 act = 0 INFO2	SN0 INFO0
POWERON		H1	-	-	-	-	-	-	-	-	-	-	-	-	-	-
LOSS OF POWER		-	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0	H0
RECEIVED S/T INFO 1 SIGNAL (Received AR)		/	ST T4 H2	-	-	-	-	-	-	-	-	/	/	-	/	-
RECEIVED S/T INFO 3 SIGNAL (Received AI)		/	/	/	/	/	/	/	/	H7	-	-	-	-	H7	/
RECEIVED S/T INFO 0 SIGNAL (Received EI)		/	-	-	-	-	-	-	-	-	H11	H11	-	-	-	-
END OF TONE TN (9 ms)		/	/	H3	-	-	-	/	/	/	/	/	/	/	-	/
RECEIVED TONE TL and ACTIVATION REQUEST (AR)		/	ST T4 H2 LSD	-	/	/	/	/	/	/	/	/	/	/	-	ST T4 STP T6 H2 LSD
ECHO CANCELLER CONVERGED		/	-	-	H3.1	-	-	-	-	-	-	-	-	-	-	-
BASIC FRAME SYNC (SW)		/	/	/	/	/	/	H5	-	-	-	-	-	-	-	-
SUPERFRAME SYNC (ISW)		/	/	/	/	/	/	/	STP T4 H6 AP	-	-	-	-	-	-	-
RECEIVED dea = 0		/	/	/	/	/	/	/	/	H9 DP	H9 DP	H9 DP	-	-	H9 DP	-
RECEIVED act = 0 and dea = 1		/	/	/	/	/	/	/	/	/	-	H7 EI	-	-	-	-
RECEIVED act = 1 and dea = 1		/	/	/	/	/	/	/	/	/	H8 AI	-	-	-	-	-
LOSS OF SYNC (> 480 ms)		/	/	/	/	/	/	/	/	H10 EI	H10 EI	H10 EI	-	-	H10 EI	-
LOSS OF SIGNAL (> 480 ms)		/	/	/	/	ST T6 H12 EI	/	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	ST T6 H12 EI	/	/	ST T6 H12 EI	-
EXPIRY OF TIMER (*) T4 (15 seconds)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	/	/	/	/	-	/	-
LOSS OF SIGNAL (< 40 ms)		/	-	/	/	/	H3.1	/	/	/	/	/	ST T6 H12	ST T7 J12	/	/
EXPIRY OF TIMER T6 (40 ms)		/	/	/	/	/	/	/	/	/	/	/	/	/	/	H1 DI
DETECTION OF SIGNAL ENERGY		/	-	-	-	H3.2	H4	-	-	-	-	-	-	-	-	-
RESET COMAND (RES)		/	-	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	H10 EI	-	-	-	-	-	-	-

(*) When timer is enabled (default)

5.1.3 Power Up Control.

In MICROWIRE mode and GCI Slave mode the device may be powered up by writing a PUP command. The PUP command has no influence on the contents of the configuration registers. In GCI Master mode two methods are available for powering up the device.

a) the Bx data input can be pulled low (local power-up command).

b) a 10 kHz wake-up tone may be received from the far-end.

5.2 ACTIVATION/DEACTIVATION OF THE ST5410 IN GCI/LT MODE.

The circuit schematic diagram for an ST4510 operating in GCI/LT mode, e.g. in a Central Office line-termination application, is shown in figure 5.3. Notice that the C/I command/indication signals are transferred from the microprocessor controller via an HDLC/GCI device, as described in chapter 4.

Figure 5.4 illustrates the logical interface between the U-device and the Level 2 software. The Level 2 controller transmits commands via an 8-bit buffer register, PH_RQ, and receives status information via a second buffer register, PH_IND. The UID chip likewise communicates status, and accepts commands, via two buffer registers, CI_IND and CI_REQ, respectively.

5.2.1 LT Activation Sequence from the Power Down State.

A proposed Activation Sequence is shown in figures 5.5a to 5.5f starting from State A which corresponds to the Power Down sub-state of the Finite State Machine state J1. This Activation sequence may be invoked either on receipt of a Level 2 request, or from downstream on detection of a wake-up tone at 10 kHz. This latter condition causes the AP code to be entered in the C/I Indication Register.

Prior to initiating Activation in the Line the device must be powered up using a PUP command. At the same time an external software timer, Timer A, is started up. If at any time this timer times out a fatal error can be signalled back to the Management Control Entity (PH_IND = ERR1).

Figure 5.3: Microprocessor Control for GCI/LT

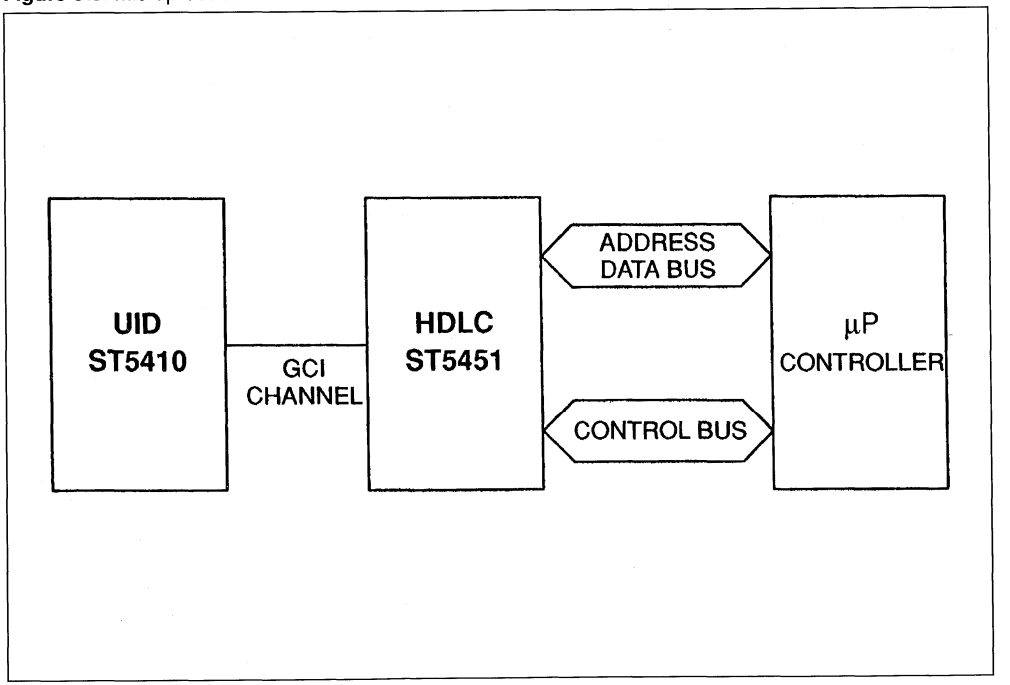
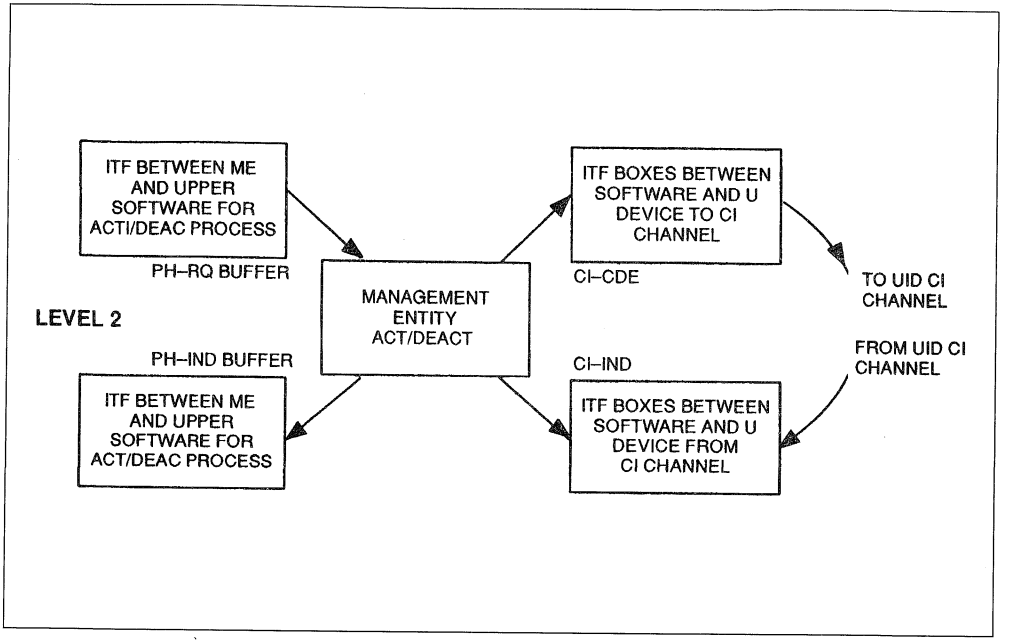


Figure 5.4: Logical Interface: UID Device/Level 2 Controller



If the UID device powers up successfully it returns the code CI_IND = TIM indicating that the UID circuit is now in the Power-up state, indicated by label B on figure 5.5a. Alternatively if this is not successful the time-out of Timer A occurs.

Note: The Timer A will occurs only if the timer T5 is disabled in other case a EI indication may be receive

5.2.2 LT Activation Process continued: from the RESET PUP State.

The continuation of the Activation sequence from the RESET Power-up state is illustrated by the flow diagram of figure 5.5b. Note that the C/I Indication signal, SYNC indicate that the U-line is fully activated up to and including the U-interface in the subscriber terminal equipment. Full synchronization of the U-line and subscriber terminal equipment is indicated by receipt of the AI indication.

5.2.3 LT Activation/Deactivation: The Fully Activated State.

In this section of the flow-diagram, (left-hand section of figure 5.5c), the control program searches for the presence of the following Level 2 commands:

a) PH_REQ = UAR. This command corresponds to a request from the exchange to deactivate the terminal (e.g. S/T interface) whilst retaining activation of the U-line.
The expected response, tested as shown in the right-hand section of figure 5.5c, is the receipt of the UAI Indication code. Failure responses include a software timeout, or receipt of the EI code, indicating loss of signal or loss of synchronization.

b) PH_REQ = RES. This command is intended to cause a Reset of the LT UID device with associated reset of the adaptive circuit coefficient values.

c) PH_REQ = DR. This command corresponds to a Level 2 request to completely deactivate the U-line and terminal. This is effected, in the routine DEACT of section 5.2.5, by transmitting a signal to the U-line with the dea bit = 0.

In addition, the control program searches for the presence of the following C/I Indication code:

d) CH_IND = EI. This code indicates either loss of signal or loss of synchronization. A call is made to the EI routine (figure 5.5f and section 5.2.6) to determine the appropriate response.

5.2.4 LT Activation/Deactivation: U-Line only Activated State.

In this section of the flow-diagram, (left-hand section of figure 5.5d), the control program searches for the presence of the following Level 2 commands:

a) PH_REQ = AR. This command corresponds to a request from the exchange to activate the terminal (e.g. S/T interface) as well as the U-line. The expected response, tested as shown in the right-hand section of figure 5.5d, is the receipt of the AI Indication code. Failure responses include a software timeout, or receipt of the EI code, indicating loss of signal or loss of synchronization.

b) PH_REQ = RES. This command is intended to cause a Reset of the LT UID device with associated reset of the adaptive circuit coefficient values.

c) PH_REQ = DR. This command corresponds to a Level 2 request to completely deactivate the U-line and terminal. This is effected, in the routine DEACT of section 5.2.5, by transmitting a signal to the U-line with the dea bit = 0.

In addition, the control program searches for the presence of certain C/I Indication codes:

d) CH_IND = AP. This Indication code corresponds to the receipt of a signal from the U-line with the bit sai = 1, indicating that the terminal requires activation. The expected response, and the fail response, are as in a) above.

e) CH_IND = EI. This code indicates either loss of signal or loss of synchronization. A call is made to the EI routine (figure 5.5f and section 5.2.6) to determine the appropriate response.

5.2.5 LT Activation/Deactivation: RESET/DEAC/POWER-DOWN.

The RESET routine, figure 5.5e, causes a Full reset of the LT UID devices, and ensures that any subsequent restart will be a "cold-start". Tests for the PH_REQ = RES command should be placed throughout the control program (selective examples only have been included in figures 5.5a to 5.5f).

The G (DEACTivate) routine also yields a Full reset, in this case without resetting the adaptive circuit coefficient values. Hence, in this case, a subsequent warm-start is not precluded.

The P (Power-down) routine is also called from various parts of the control program, and just place the UID in power down state, a cold start or warm start will append later depending the UID precedent events

5.2.6 LT Activation/Deactivation: EI Processing Routine.

This routine is used to distinguish between two cases:

a) U-line signal received with the act bit = 0. In this case a subsequent return to the fully-activated state is possible, and is indicated by receipt of the CI_IND = AI signal. Alternatively, receipt of CI_IND = DI gives a Full reset with possibility of a subsequent warm-start.

b) Loss of U-line signal, or loss of synchronism of the U-line signal.
In this case a RESET is produced with subsequent possibility of a cold-start only.

5.3 ACTIVATION/DEACTIVATION OF THE ST5410 IN MICROWIRE/NT MODE.

The circuit schematic diagram for an ST5410 operating in MICROWIRE/NT mode, e.g. in a subscriber terminal application, is shown in figure 5.6.

Notice that the C/I command/indication signals are transferred from the microprocessor controller via a MICROWIRE Serial Port, as described in chapter 4.

The logical interface between the UID device and the Level 2 software is implemented in the manner illustrated in figure 5.4.

5.3.1 NT Activation Sequence from the Power Down State.

A proposed Activation Sequence is shown in figures 5.7a to 5.7f starting from State A which corresponds to the Power Down sub-state of the Finite State Machine state H1.
This Activation sequence may be invoked either on receipt of a Level 2 request, or from the exchange direction on detection of a wake-up tone at 10 kHz. This latter condition causes the LSD code to be entered in the C/I Indication Register.

Prior to initiating Activation in the Line the device must be powered up using a PUP command. After a short period of time, determined by a software timeout and chosen to allow the PUP command to take effect, the CI_REQ = AR command is applied and a Timer, Timer A of 30 seconds, is started up. If at any time this timer times out a fatal error can be signalled back to the Management Control Entity (PH_IND = ERR1). In normal operation, the UID State Machine should progress to State B, Full-Reset (PUP), equivalent to state H1 in figure 5.2.

Figure 5.5a: GCI/LT Mode: Activation/Deactivation: (State A)

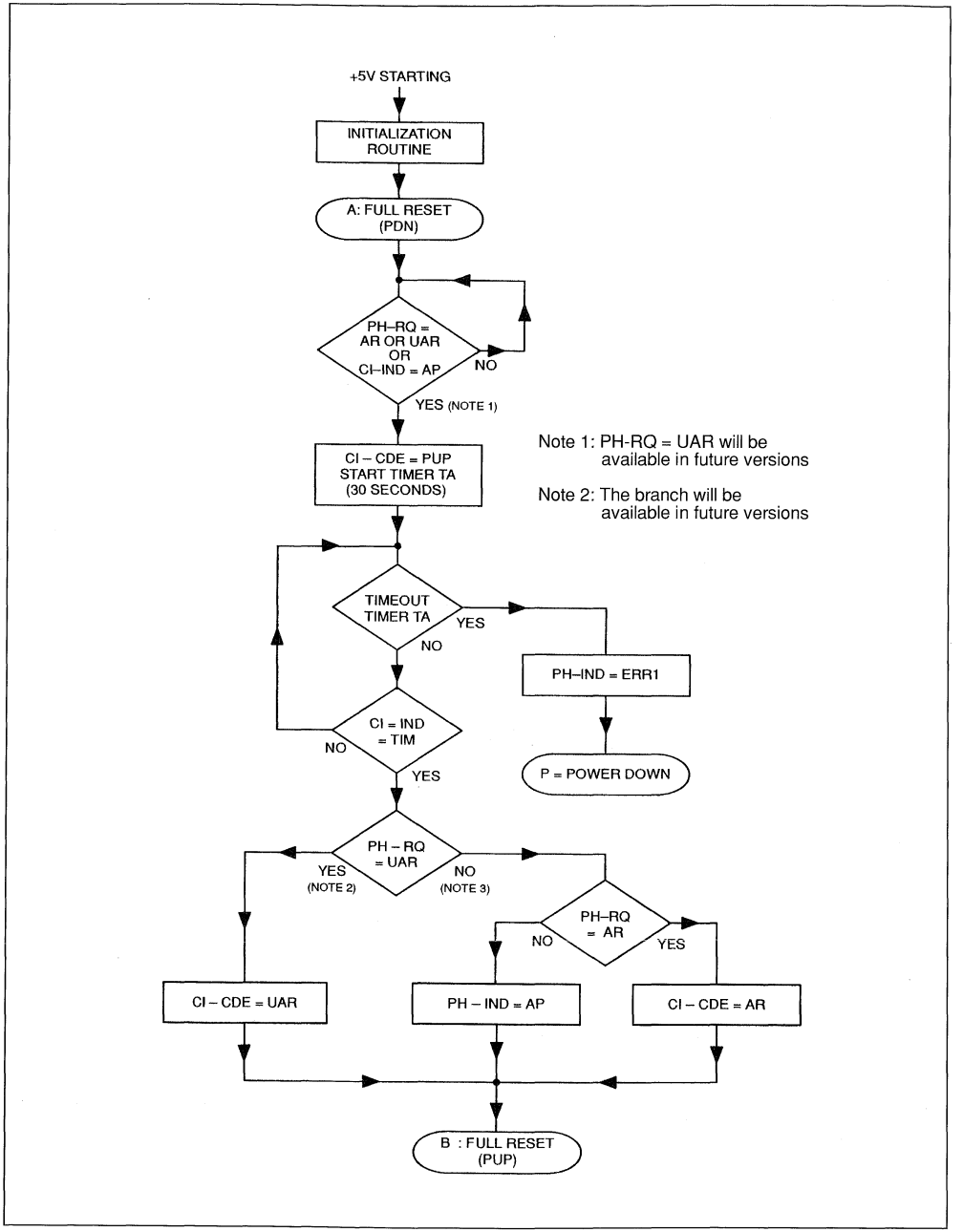


Figure 5.5b: GCI/LT Mode: Activation/Deactivation: (State B)

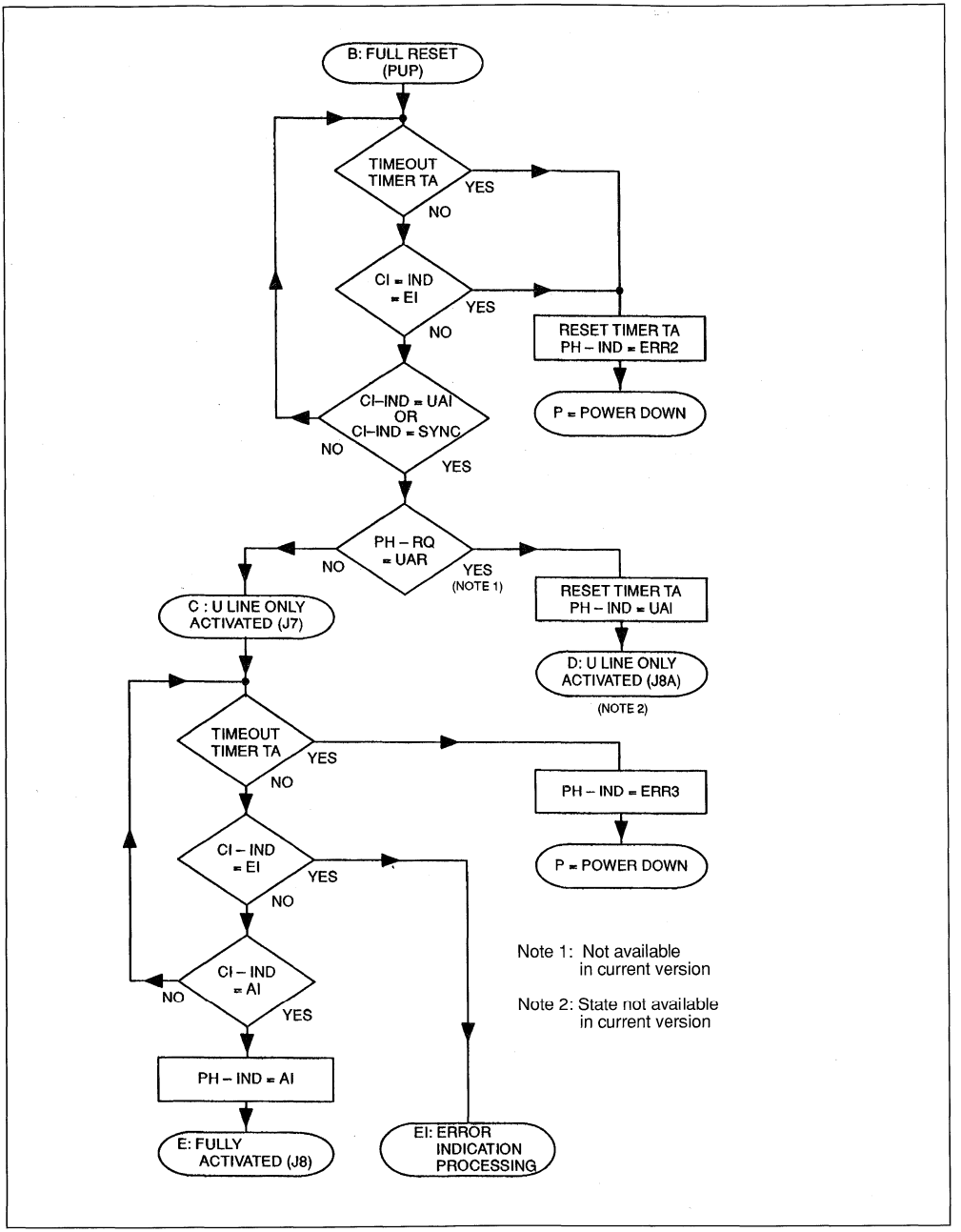


Figure 5.5c: GCI/LT Mode: Activation/Deactivation: (State E)

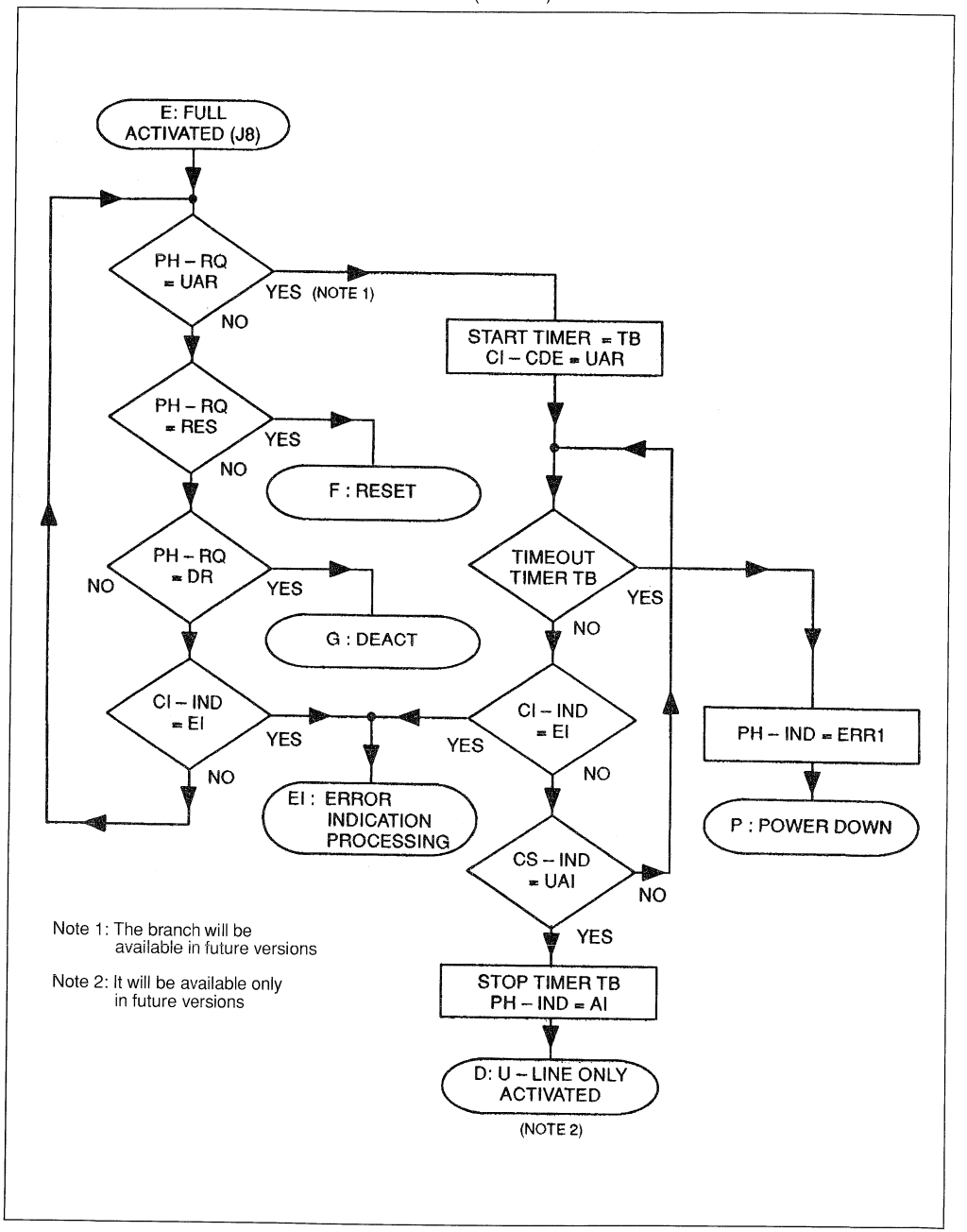


Figure 5.5d: GCI/LT Mode: Activation/Deactivation: (State D)

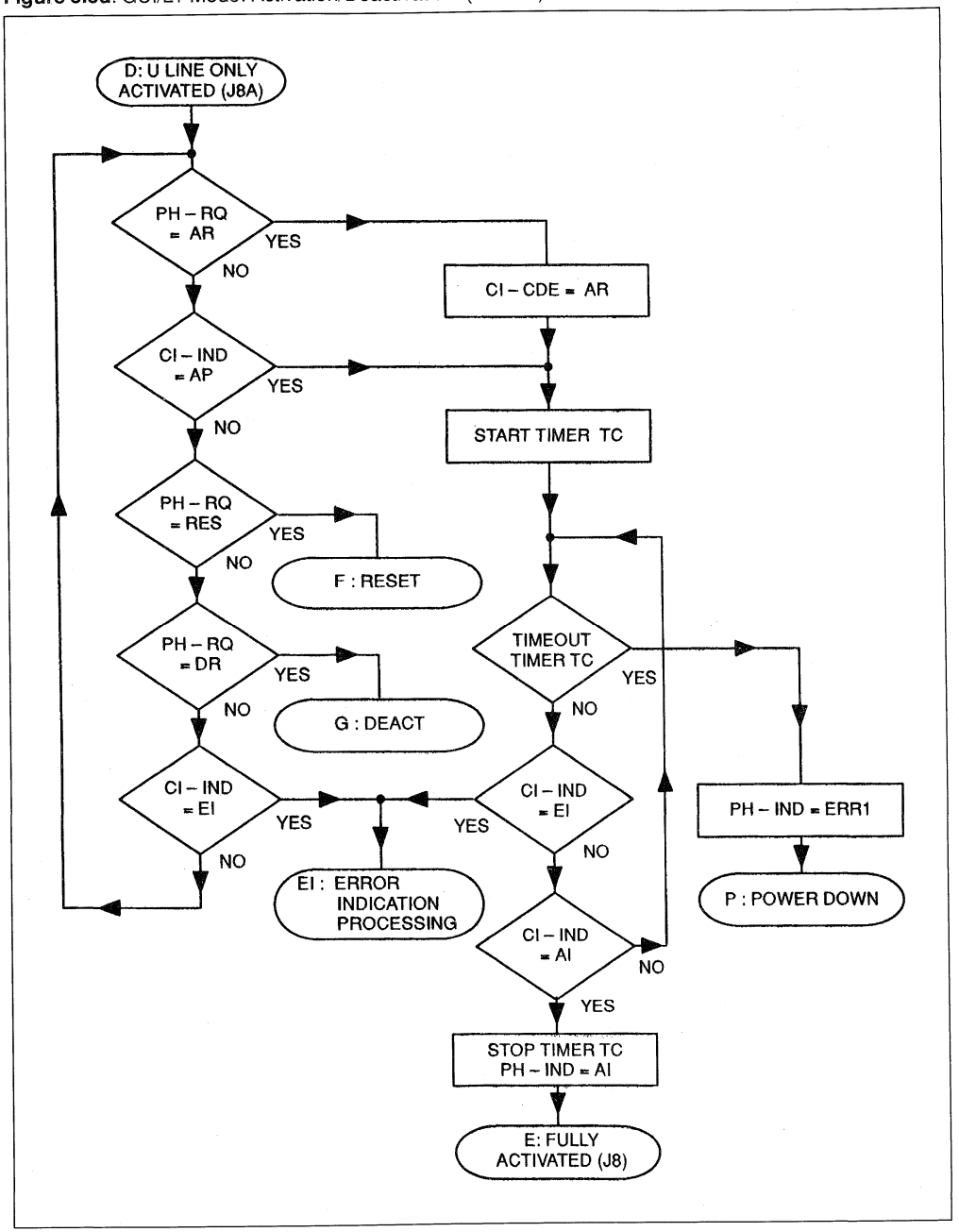


Figure 5.5e: GCI/LT Mode: Activation/Deactivation: (State E)

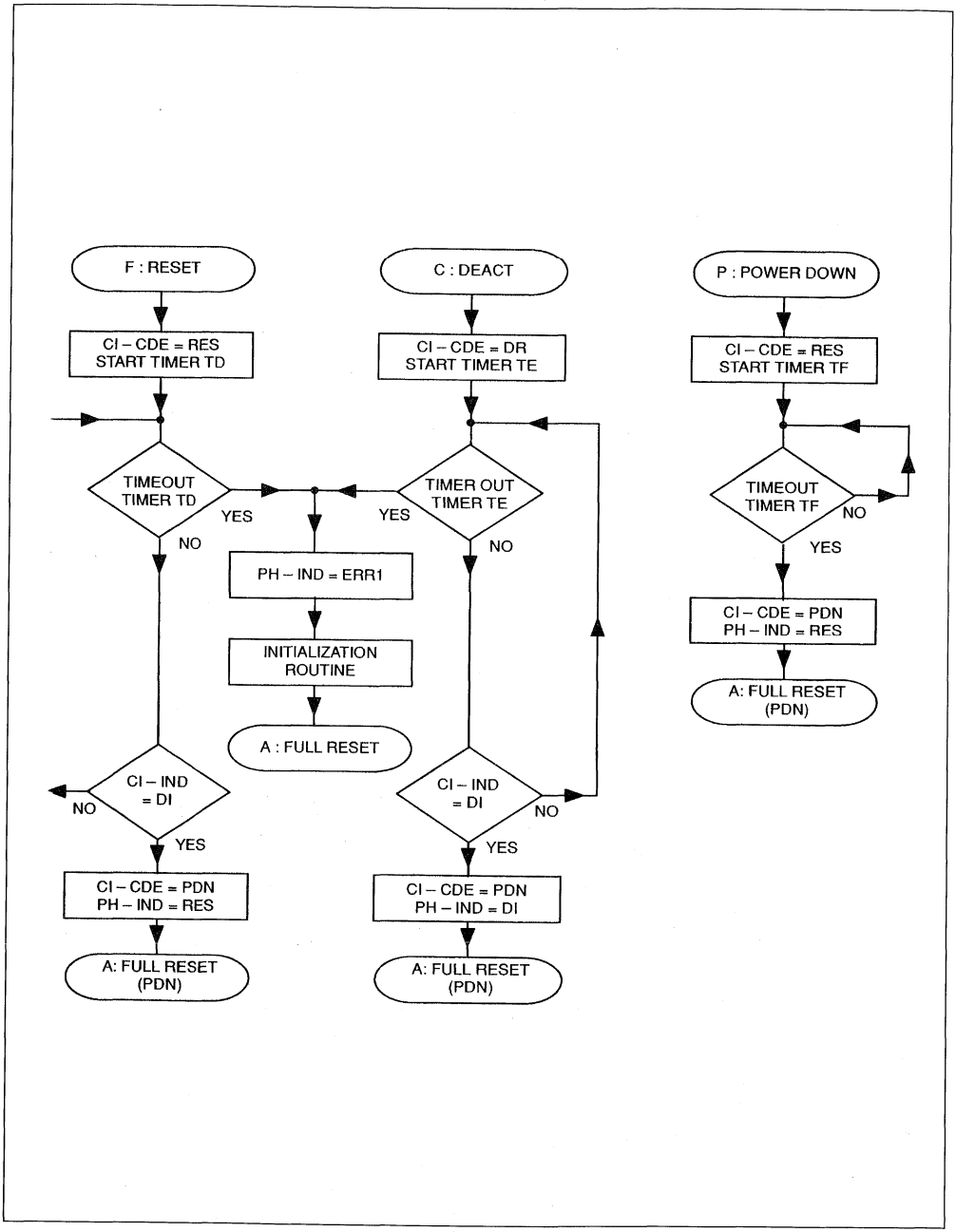


Figure 5.5f: GCI/LT Mode: Activation/Deactivation: (State EI)

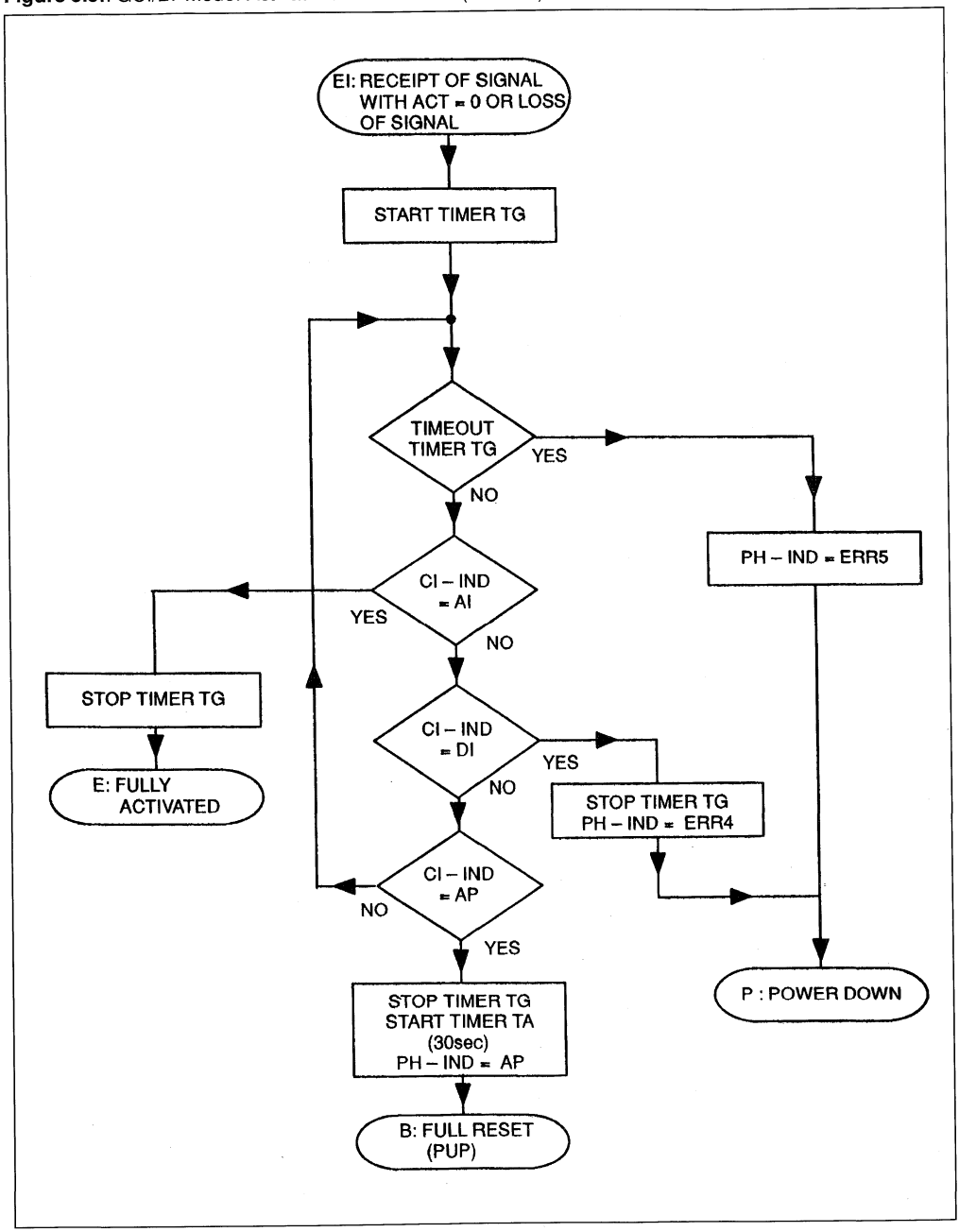
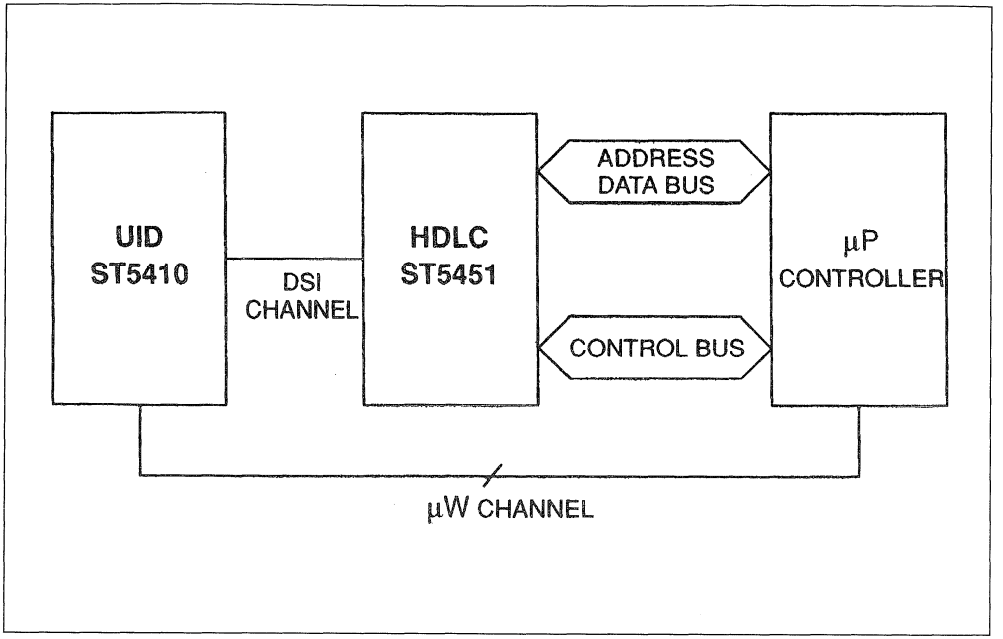


Figure 5.6: Microprocessor Control for MICROWIRE/NT



5.3.2 NT Activation Process continued: from the RESET PUP State.

The continuation of the Activation sequence from the RESET Power-up state is illustrated by the flow diagram of figure 5.7b. The control program searches for the appearance of the C/I Indication codes AP, (versions 1 or 2), or UAP (version 2 only).

In either event U-line synchronization, both frame and superframe, has been achieved, and the UID State Machine is now either in state H6 (AR request), or H8A (UAR request).

Failure to reach either of these states may produce a timeout, software or internal UID chip hardware, or an EI signal.

From state H6 further progression is shown in figure 5.7c. Successful completion of Activation will be indicated by the receipt of the AI Indication signal. A fault condition, eg. loss of synchronization, loss of signal, or timeout, will be indicated by the EI signal.

5.3.3 NT Activation/Deactivation: The Fully Activated State.

In this section of the flow-diagram, figure 5.7d, the control program searches for the presence of the following Level 2 commands:

a) PH_REQ = RES. This command is intended to cause a Reset of the LT UID device with associated reset of the adaptive circuit coefficient values.

b) PH_REQ = EI. This command causes the subscriber terminal equipment to send a U-line signal upstream with the act bit reset to zero. The normal consequence of this is the receipt of DP (Deactivate signal).
Alternative responses are the EI signal, corresponding to a loss of signal or loss of synchronization, or a timeout.

In addition, the control program searches for the presence of certain C/I Indication codes:

c) CH_IND = DTP (if implemented). This code corresponds to the receipt of a U-line signal from the exchange with the uoa bit = 0. The effect of this command should be to retain activation of the U-line while deactivating the terminal. This requires that the U-interface should remain operative

d) CH_IND = DP. This code corresponds to the receipt of a U-line signal from the exchange with the dea bit = 0.
The effect of this command should be to deactivate both the U-line and the terminal. In this case the U-interface may be turned off, and the UID device can be fully reset.

e) CH_IND = EI. This code indicates either loss of signal or loss of synchronization, or receipt of a U-line signal with the act bit = 0. A call is made to the EI routine (figure 5.7f and section 5.3.6) to determine the appropriate response.

5.3.4 NT Activation/Deactivation: U-Line only Activated State. I n this section of the flow-diagram, figure 5.7e, the control program searches for the presence of the following Level 2 command:

a) PH_REQ = AR. This command is intended to cause complete activation of the U-line and subscriber terminal. The normal response to this command is the AP Indication code. Fault condition responses include a timeout, or the receipt of the EI Indication code.

In addition, the control program searches for the presence of certain C/I Indication codes:

b) CH_IND = DP. This code corresponds to the receipt of a U-line signal with the dea bit =0. The effect of this command should be to deactivate both the U-line and the terminal. In this case the U-interface may be turned off, and the UID device can be fully reset.

c) CH_IND = AP. This code corresponds to the receipt of a U-line signal with the uoa bit = 1. This Indication code signals an attempt by the exchange to cause complete activation of the U-line and subscriber terminal.

d) CH_IND = EI. This Indication code indicates loss of U-line signal or loss of synchronization.

5.3.5 NT Activation/Deactivation: RESET/DEAC/POWER-DOWN.

The RESET routine, figure 5.7g, causes a Full reset of the NT UID device, and ensures that any subsequent restart will be a "cold-start". Tests for the PH_REQ = RES command should be placed throughout the control program (selective examples only have been included in figures 5.7a to 5.7f).

The G (DEACTivate) routine also yields a Full reset, in this case without resetting the adaptive circuit coefficient values. Hence, in this case, a subsequent warm-start is not precluded.

The P (Power-down) routine is also called from various parts of the control program, and just place the UID in power down state, a cold start or warm start will append later depending the UID precedent events.

5.3.6 NT Activation/Deactivation: EI Processing Routine.

This routine (figure 5.7f) is used to distinguish between two cases:

a) U-line signal received with the act bit = 0. In this case a subsequent return to the fully-activated state is possible, and is indicated by receipt of the CI_IND = AI signal. Alternatively, receipt of CI_IND = DP gives a Full reset with possibility of a subsequent warm-start.

b) Loss of U-line signal, or loss of synchronism of the U-line signal.

Figure 5.7a: µW/NT Mode: Activation/Deactivation: (State a)

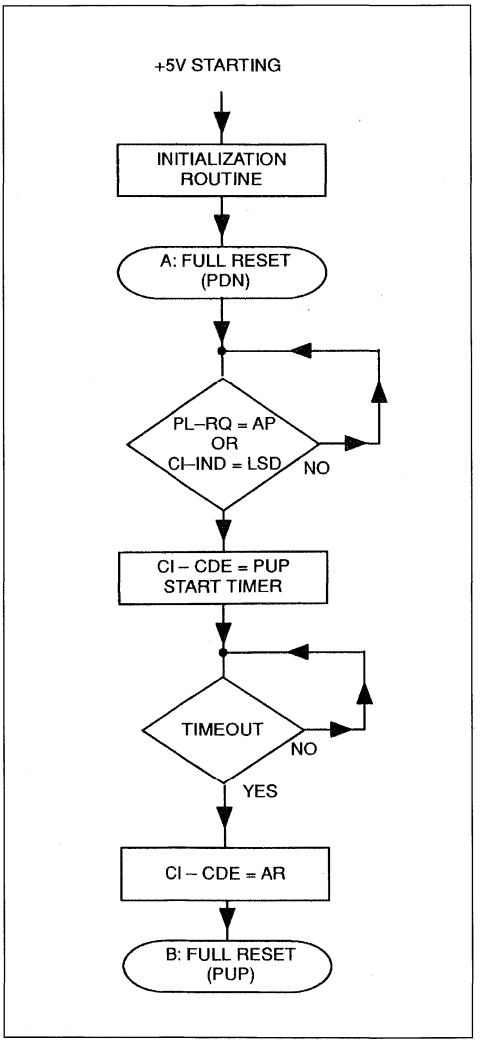


Figure 5.7b: µW/NT Mode: Activation/Deactivation: (State B)

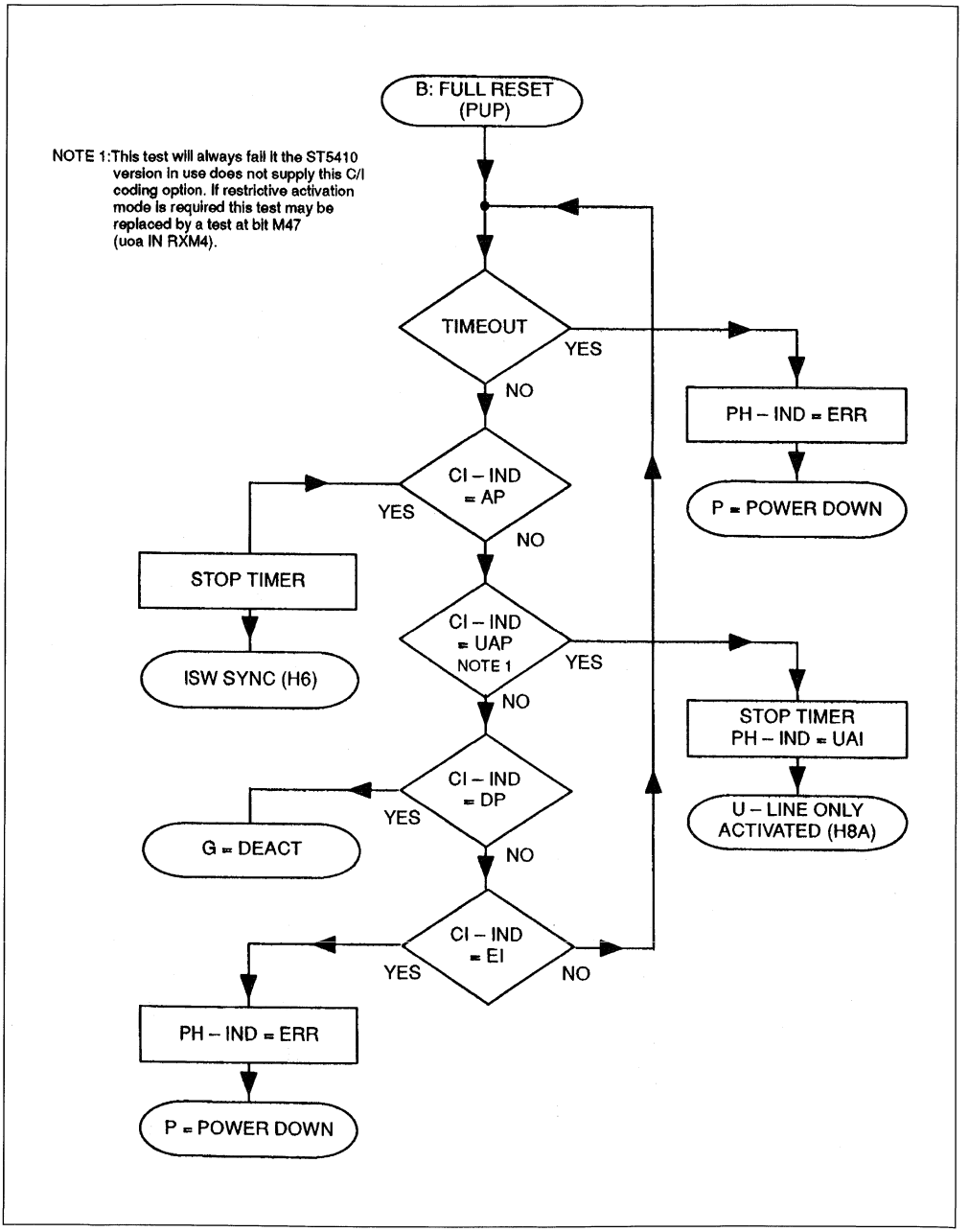


Figure 5.7c: µW/NT Mode: Activation/Deactivation: (State H6)

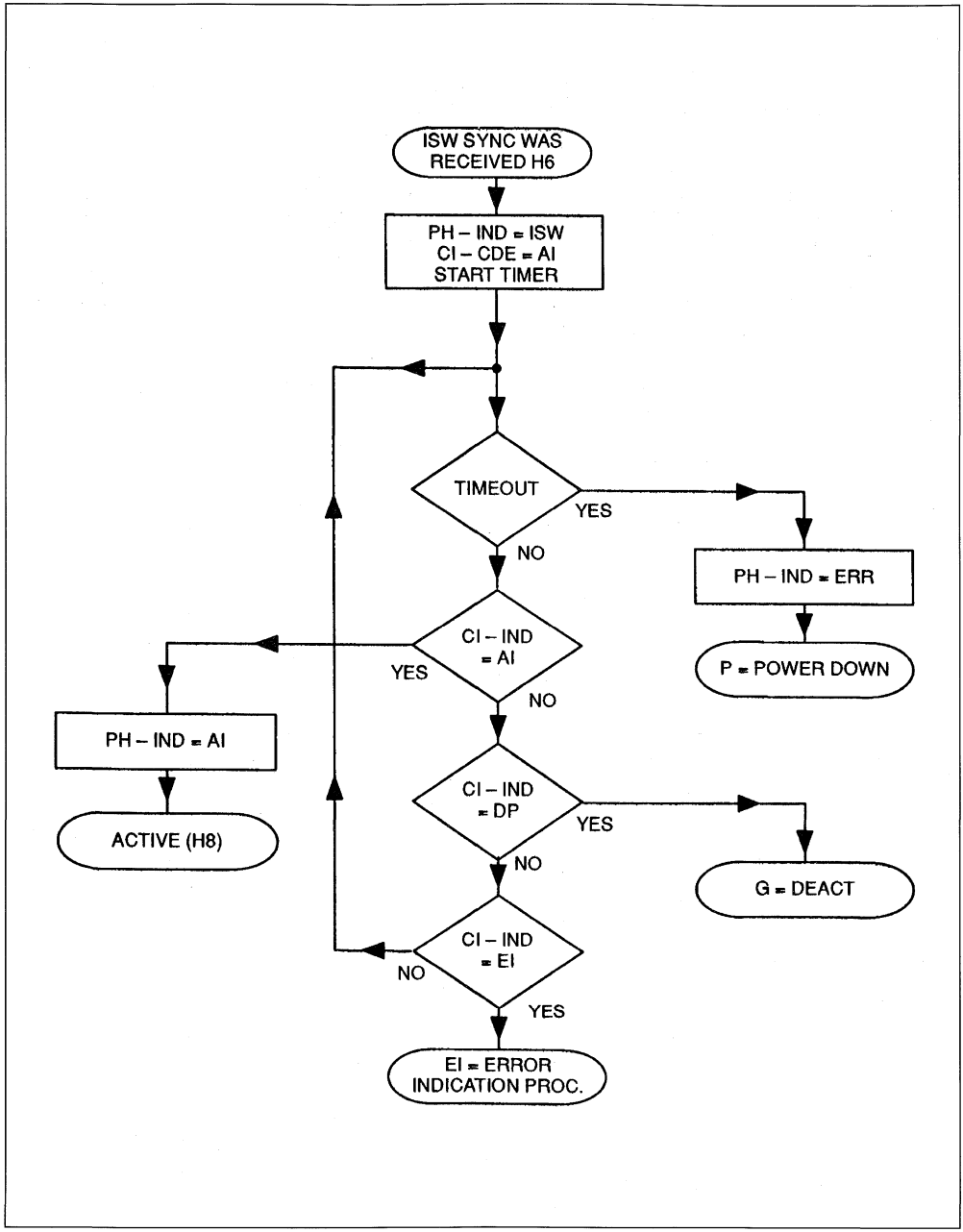


Figure 5.7d: µW/NT Mode: Activation/Deactivation: (State H8)

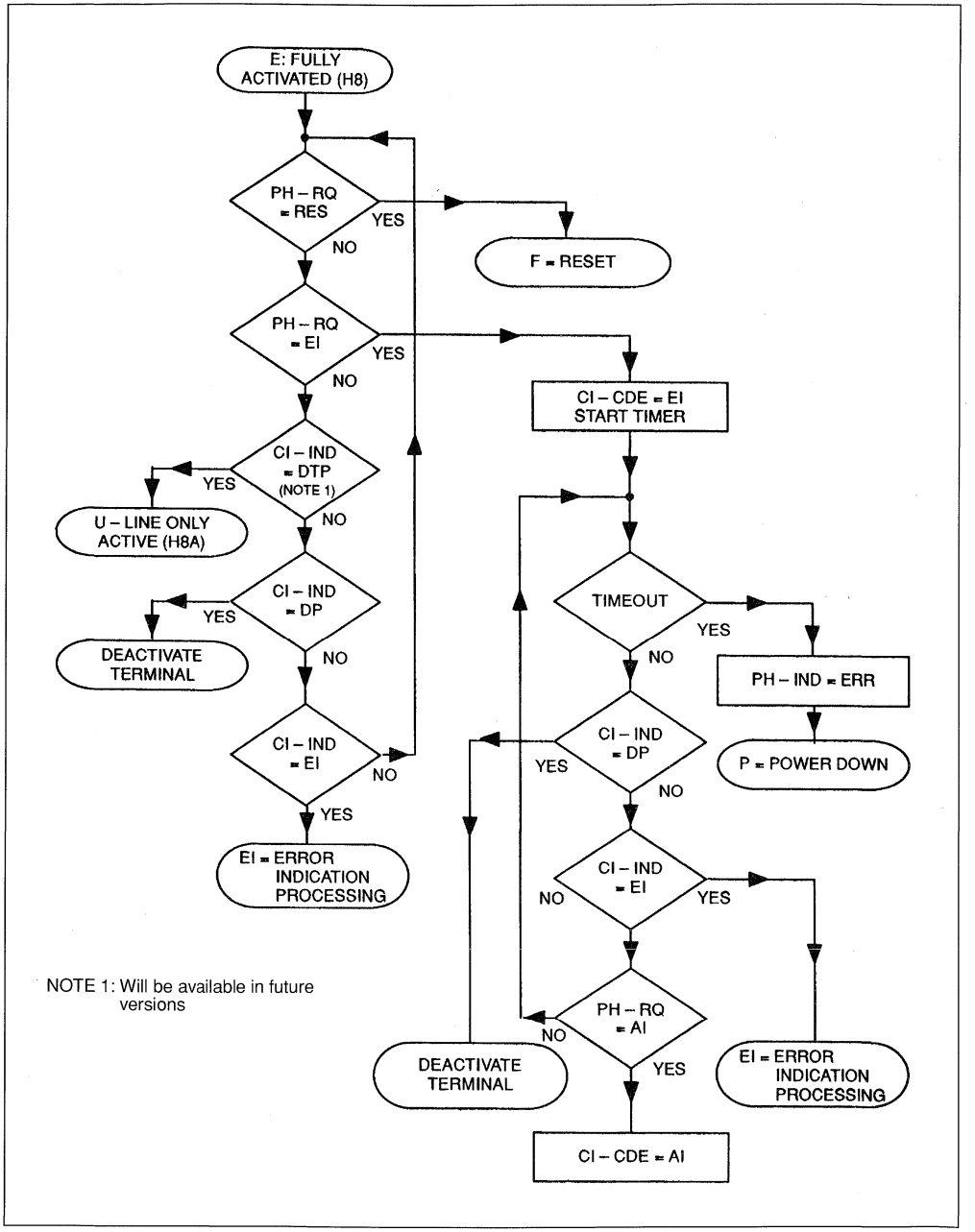


Figure 5.7e: μW/NT Mode: Activation/Deactivation: (State H8A)

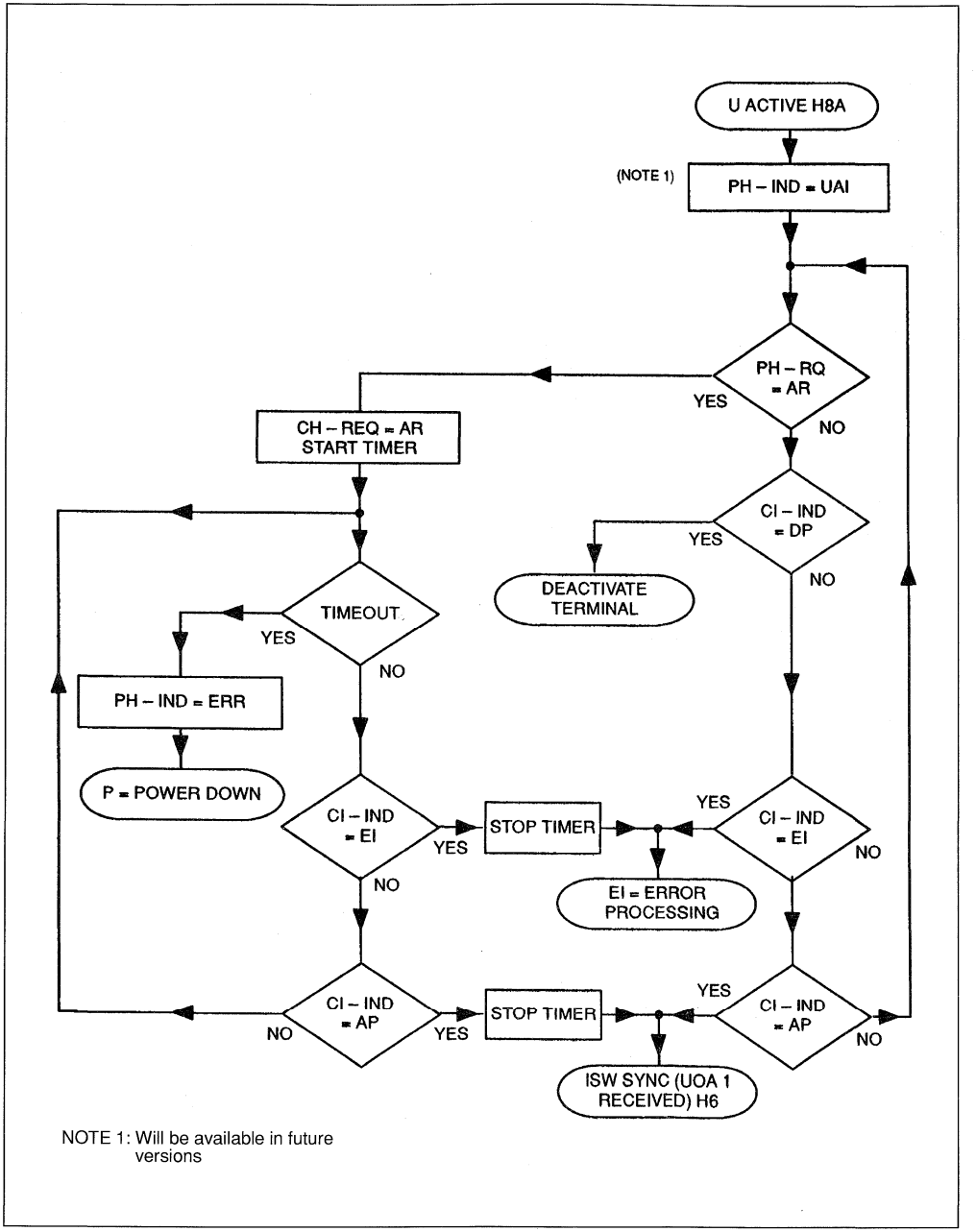


Figure 5.7f: µW/NT Mode: Activation/Deactivation: (State EI)

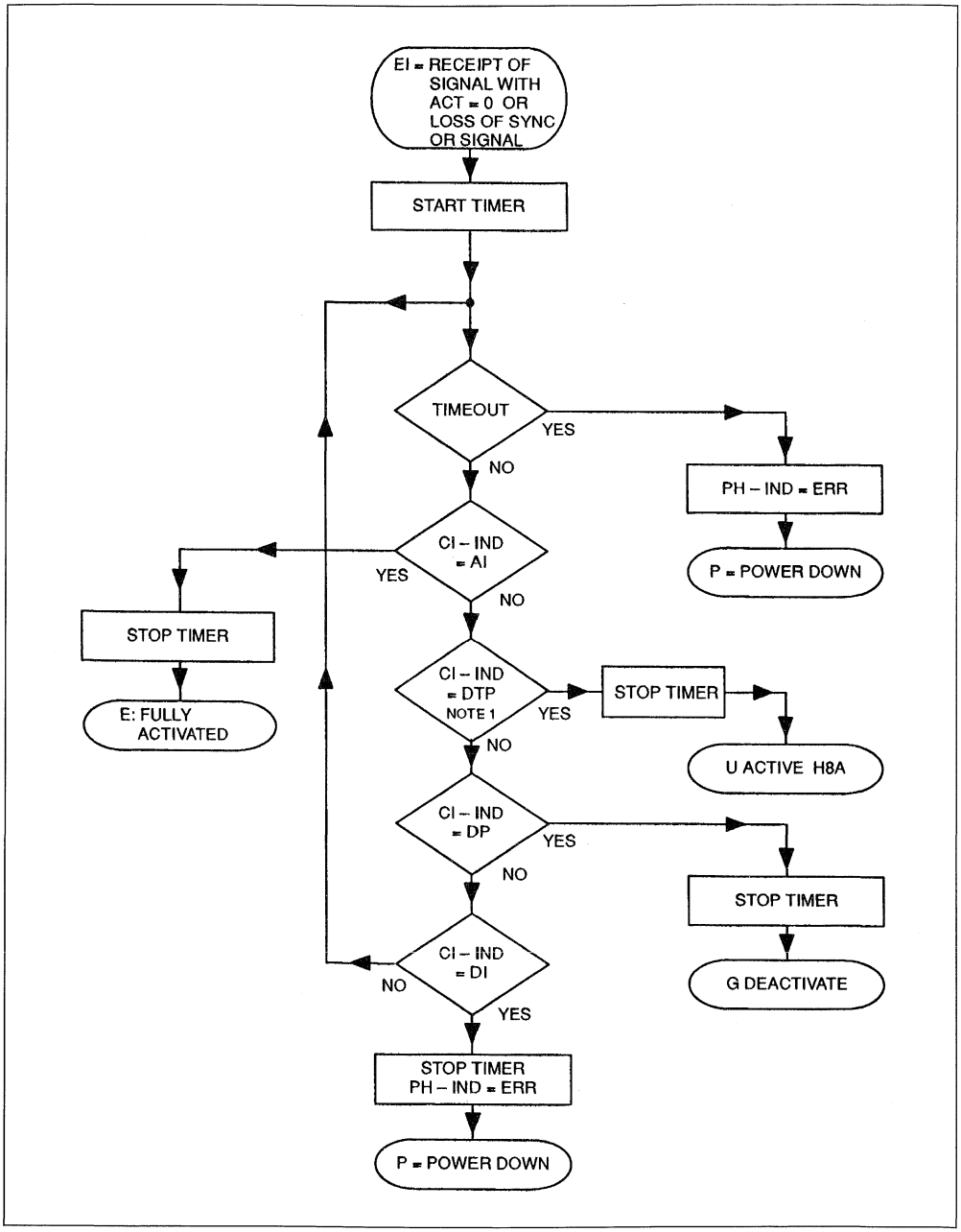
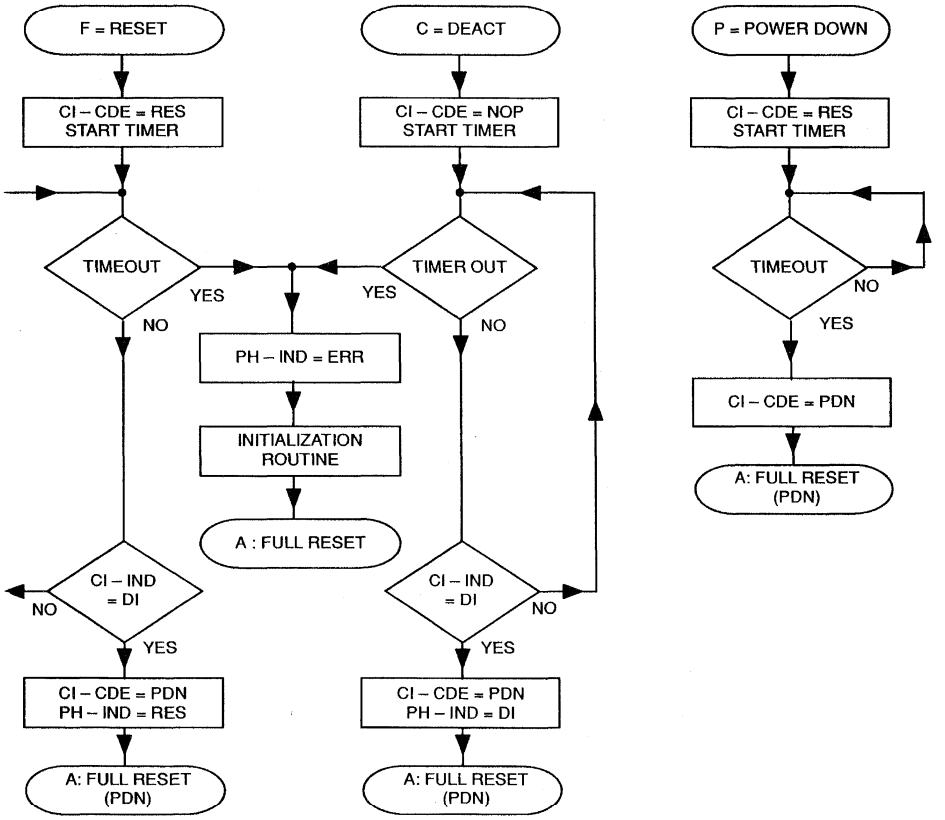


Figure 5.7g: µW/NT Mode: Activation/Deactivation: (State F, G, P)



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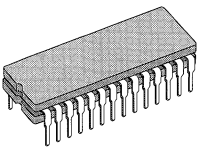
SGS-THOMSON MICROELECTRONICS

STU2071

4B3T U INTERFACE CIRCUIT

PRELIMINARY DATA

- 4B3T TWO-WIRE U INTERFACE CIRCUIT FOR LT AND NT APPLICATION
- 120 kbaud LINE SYMBOL RATE (120 SYMBOLS PER FRAME)
- SCRAMBLER AND DESCRAMBLER ACCORDING TO CCITT REC V.29
- BARKER CODE (11 SYMBOLS) SYNCHRONIZATION WORD
- UNSCRAMBLED 1 KBIT/S HOUSEKEEPING CHANNEL
- ADAPTIVE ECHO CANCELLATION WITH TRANSVERSAL FILTERING
- ADAPTIVE DECISION FEEDBACK EQUALIZATION
- AUTOMATIC GAIN CONTROL
- PDM AD CONVERTER
- AUTOMATIC ACTIVATION AND DEACTIVATION WITH POLARITY ADAPTION
- AUTOMATIC CODE VIOLATION DETECTION
- POWER FEED UNIT CONTROL
- ADVANCED CL3 1.5µm CMOS PROCESS
- 28 PIN DUAL-IN-LINE CERAMIC PACKAGE
- V* DIGITAL INTERFACE



Ceramic DIP28

ORDERING NUMBER:
STU2071F1

SYSTEM OVERVIEW

STU2071 (UIC) provides two transparent 64 kbit/s B channels, a transparent 16 kbit/s D channel, a transparent 1 kbit/s service channel and a 1 kbit/s maintenance channel for loop and error messages on subscriber lines.

UIC enables full duplex continuous data transmission via the standard twisted pair telephone cable. Adaptive Echo cancellation is used to restore the received data. An equalizer, done with an adaptive filter, restores the data which are distorted by the transmission line.

The coefficient of the equalizer and echo canceller are conserved during a power down. An all digital PLL performs both bit and frame synchronization.

The analog front end consists of receive path RX and transmit path TX, providing a full duplex analog interfacing to the twisted pair telephone cable. Before data are converted to analog signals, they pass through a digital filter (TX-filter) to reduce the high frequency components. After D/A conversion the signal is amplified and sent to the hybrid.

The received signal is converted back to digital data and passed through the RX matching filter to restore the line signal. The A/D convertor is a second order sigma/delta modulator which operates with a clock of 15.36 MHz. After timing recovery, achieved by a digital PLL, the received signal is equalized, in an adaptive digital filter, to correct for the frequency and group delay distortion of the line.

Power supply status can be read via PFOFF. The UIC can disable its power supply (DISS), and two relay drivers outputs are provided (accessible via B2*) to control the power feed unit (RD1,RD2).

PIN CONNECTION (Top view)

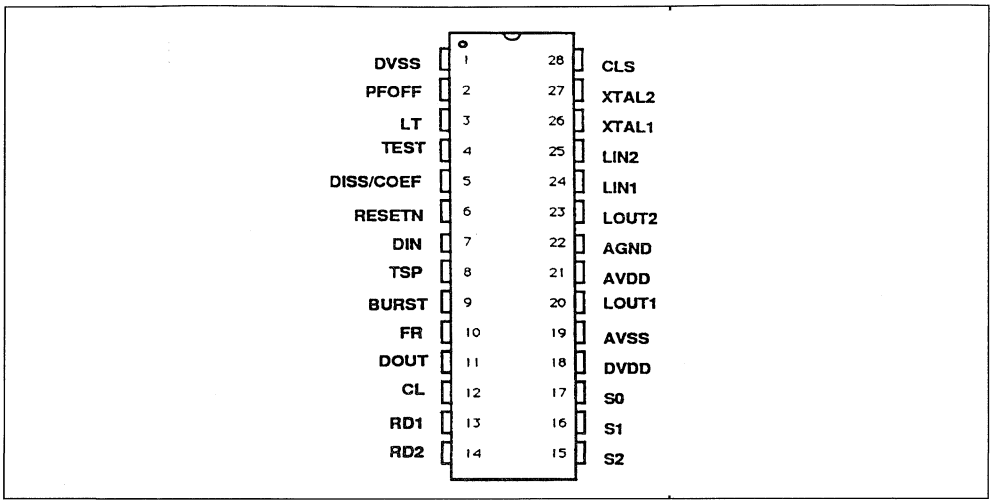
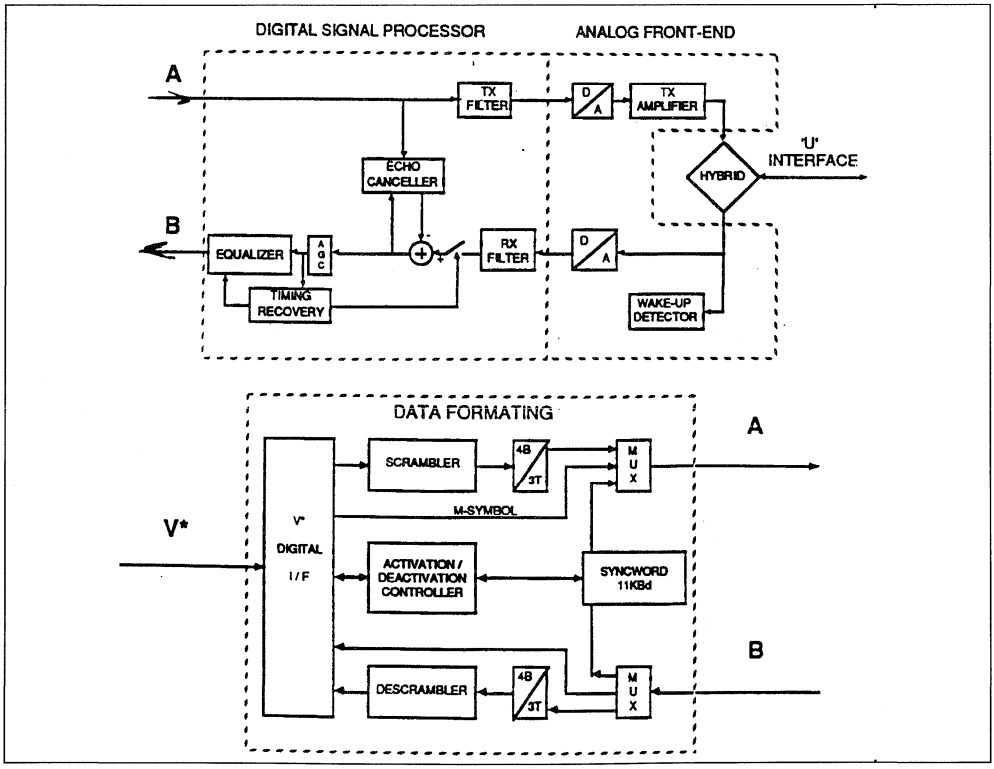


Figure 1: UIC Schematic Block Diagram



PIN DESCRIPTION

Pin	Name	Function
1	DVSS(input)	Digital Ground.
2	PFOFF(input)	Power feed off. PFOFF=HIGH is coded by the A-bit indication HI accessible on DOUT. Active in LT mode only.
3	LT(input)	LT/NT mode selection.
4	TEST(input)	Test Mode.
5	DISS(output)	A bit channel driven pin. Active in LT mode only.
6	RESETN(input)	Hardware Reset.
7	DIN(input)	Digital interface input.
8	TSP(input)	Transmit single pulse. 1 KHz single pulse alternating positive and negative polarity is transmitted.
9	BURST(input)	Burst mode selection. Active in LT mode only.
10	FR(in/out)	8KHz Digital interface frame clock; input in LT and output in NT mode.
11	DOUT(output)	Digital interface output.
12	CL(in/out)	Digital interface bit clock; input in LT and output in NT mode.
13	RD1(output)	Power feeder relay driver.
14	RD2(output)	Power feeder relay driver.
15, 16, 17	S2,S1,S0	Time slot pin strap (. Active in LT mode only.
18	DVDD(input)	5V +/-5% positive digital power supply.
19	AVSS(input)	Analog Ground.
20	LOUT1(output)	Output to the line.
21	AVDD(input)	5V +/-5% positive analog power supply.
22	AGND(input)	Analog Ground.
23	LOUT2(output)	Output to the line.
24,25	LIN1,LIN2(input)	Inputs from the line (UK0).
26, 27	XTAL1,XTAL2(inputs)	System clock input;nominal frequency is 15.36MHz.
28	CLS(output)	Clock output synchronous to the line receive clock at 7.68MHz.

APPLICATION AND MODES

The UIC can be used in LT, LT-burst and in NT mode.

Hereafter a list of the pin bias to set up the desired mode is given.

In LT mode:

Pins	Value
LT	1
BURST	0
S0	0
S1	0
S2	0

In LT burst:

Pins	Value
LT	1
BURST	1
S0	time slot
S1	time slot
S2	time slot

In NT:

Pins	Value
LT	0
BURST	0
S0	0
S1	0
S2	1

Test pins should always be tied to GND

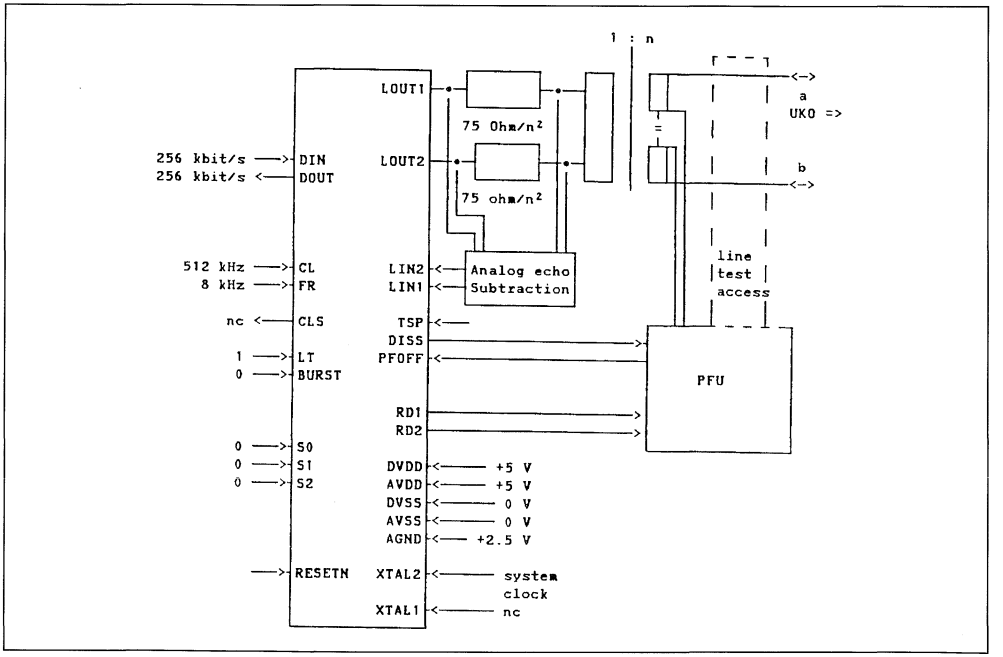
MODE DEPENDENT FUNCTIONS

PIN		MODE		
		LT burst	NT	LT
LT	input	1	0	1
BURST	input	1	0	0
S2, S1, S0	input	static	1 0 0	0 0 0
DIN DOUT	input output	2048 kbit/s	256 kbit/s	256 kbit/s
CLS (MHz)	output	7.68	7.68	7.68
CL (KHz)	input output	4096 –	– 512	512 –
FR (KHz)	input output	8 –	– 8	8 –

RECOMMENDED APPLICATIONS

LT mode

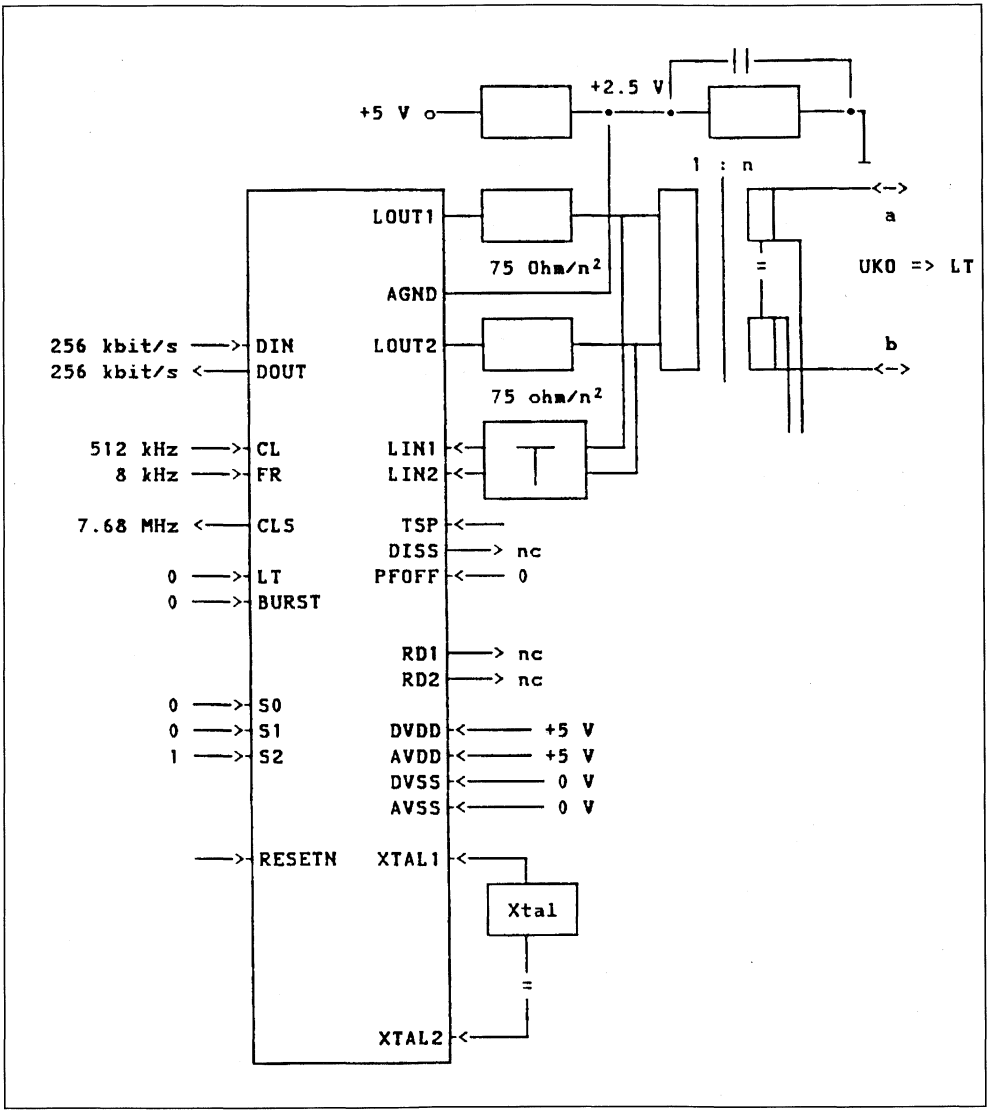
Figure 2: LT Schematic Application Diagram



DIN: Data input, datarate = 256 kbit/s, continuous
DOUT: Data output, datarate = 256 kbit/s, continuous
CL: Data clock input, f = 512 KHz
FR: Frame clock input, f = 8 KHz (1:1)
XTAL2: System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS: Clock output, 7.68 MHz

NT mode

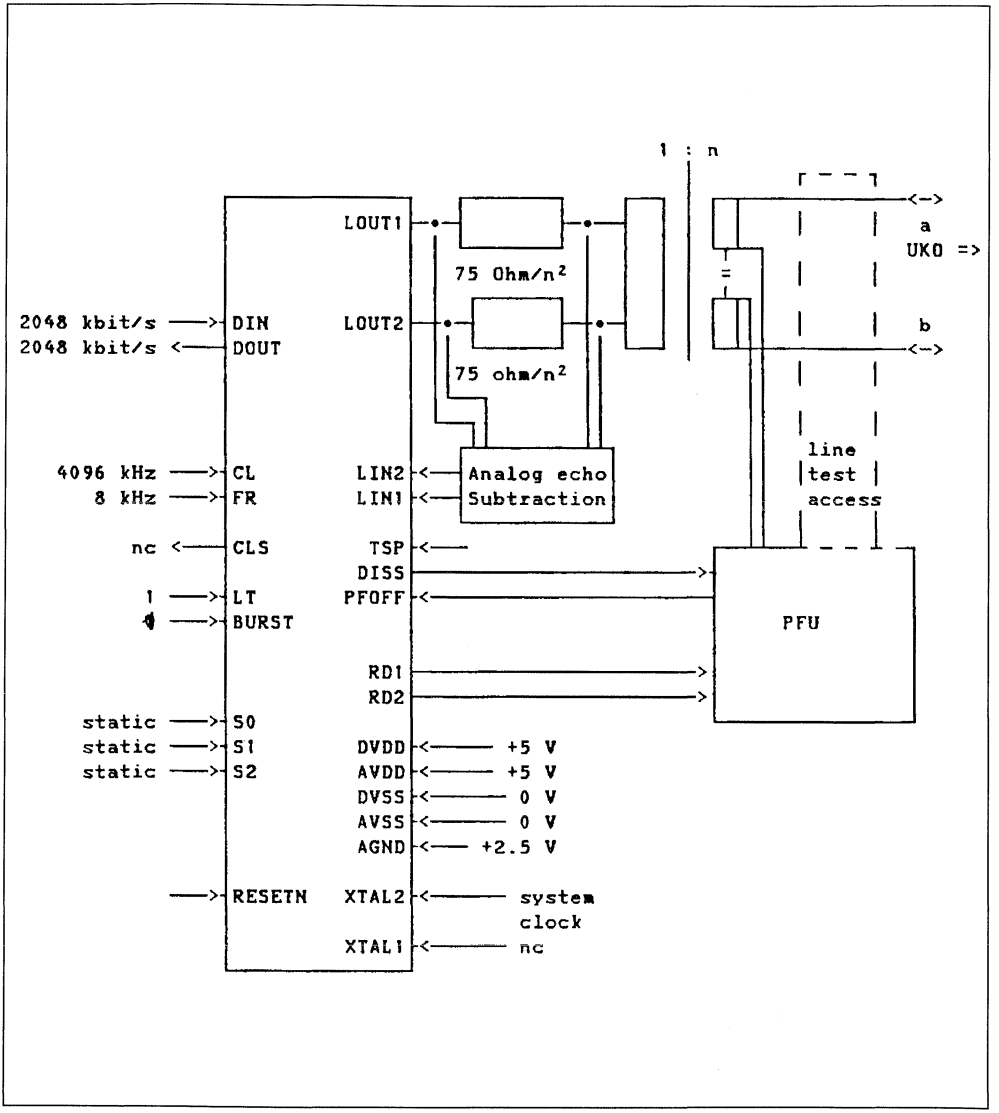
Figure 3: LT Schematic Application Diagram



DIN:	Data input, datarate = 256 kbit/s, continuous
DOUT:	Data output, datarate = 256 kbit/s, continuous
CL:	Data clock input, f = 512 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL1/2:	15.36 MHz Xtal connection (Clock not synchronous to system clock)
CLS:	Clock output, 7.68 MHz (used to synch S interface)

LT burst mode

Figure 4: LT Burst Mode Schematic Application Diagram.



DIN:	Data input, datarate = 2048 kbit/s, continuous
DOUT:	Data output, datarate = 2048 kbit/s, continuous
CL:	Data clock input, f = 4096 KHz
FR:	Frame clock input, f = 8 KHz (1:1)
XTAL2:	System clock input, f = 15.36 MHz (Tx clock synchronous to system clock)
CLS:	Clock output, 7.68 MHz

DIGITAL INTERFACE

UIC is provided with a digital serial interface, named V*, which operates in two modes.

In Fig. 5 the frame format for both modes is shown.

The base frame consists of:

B1 : 64 kbit/s transparent data channel

B2 : 64 kbit/s transparent data channel

B2* : Monitor channel

B1* : 8 bits so set

D1/D2 : 16 kbit/s D channel

A1..A4 : Command/Indicate channel

T : Transparent service channel

E : Extension bit

In Fig. 6 and 7 the timings in Continuous and in Burst mode are given.

Figure 5: V* Frame Format.

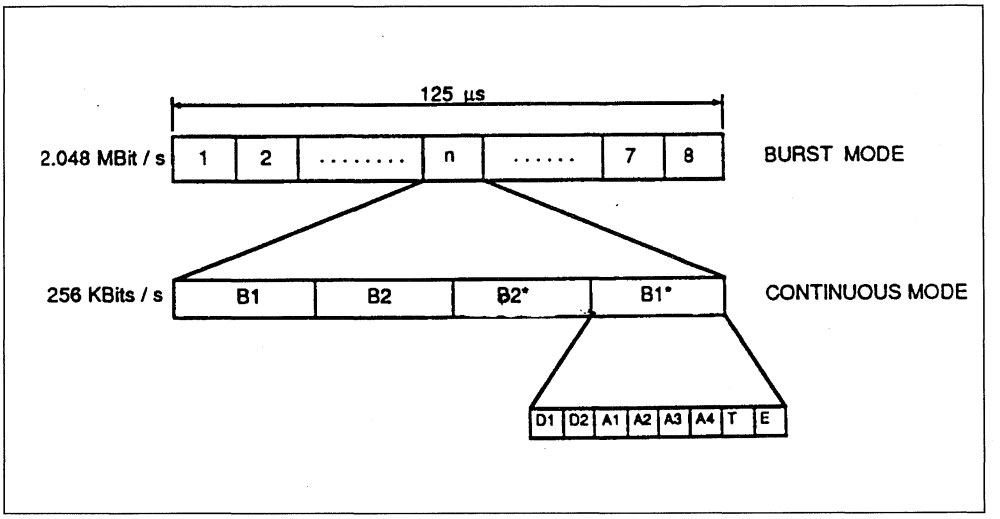


Figure 6: Continuous Mode.

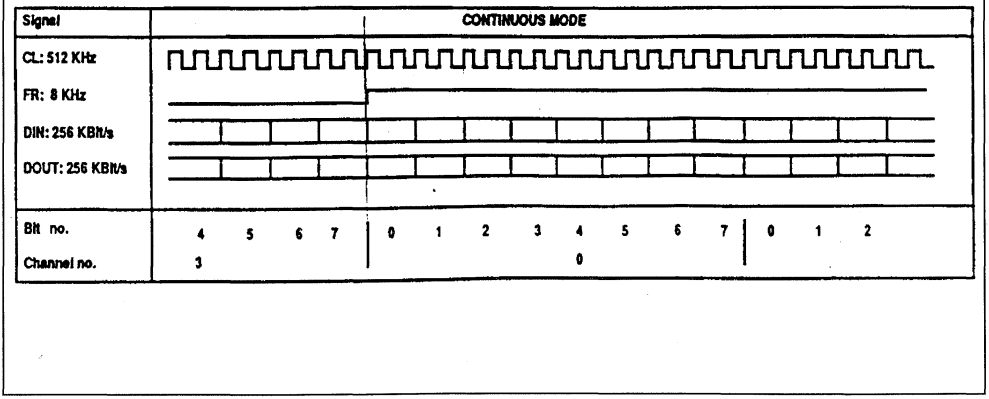
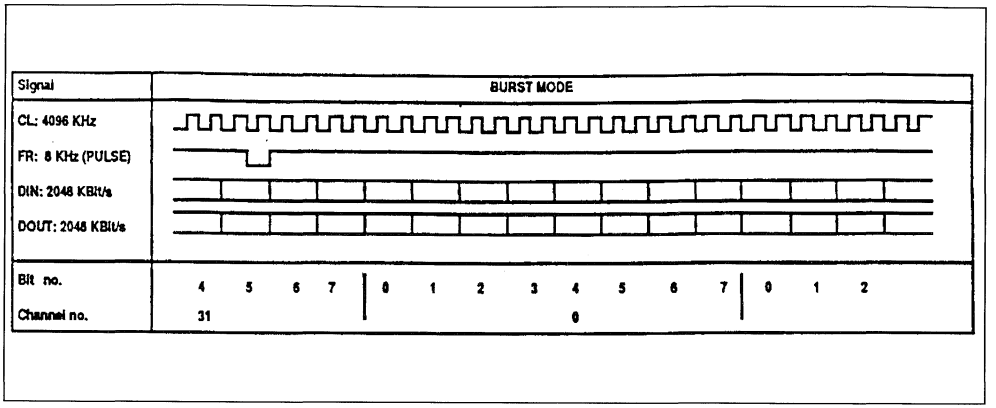


Figure 7: Burst Mode.



LINE FRAME STRUCTURE.

The information flow across the subscriber line uses the frame structure here below. The length of one frame corresponds to 120 ternary symbols being transmitted within 1 ms.

1	2	3	4	5	6	7	8	9	10	11	12		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1		
T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	T1	24	
T1	T1	T1	T2	T2	T2	T2	T2	T2	T2	T2	T2	36	
T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	T2	48	
T2	T2	T2	T2	T2	T2	T3	T3	T3	T3	T3	T3	60	LT ⇒ NT
T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	T3	72	
T3	T3	T3	T3	T3	T3	T3	T3	T3	T4	T4	T4	84	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	96	
T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	T4	108	
T4	SW1											120	

1	2	3	4	5	6	7	8	9	19	11	12		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5		
T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	T5	24	
M2	T5	T5	T5	T6	T6	T6	T6	T6	T6	T6	T6	36	
T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	T6	48	
T6	SW2											60	NT ⇒ LT
T6	T6	T6	T6	T6	T6	T7	T7	T7	T7	T7	T7	72	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	T7	84	
T7	T7	T7	T7	T7	T7	T7	T7	T7	T8	T8	T8	96	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	108	
T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	T8	120	

Agenda:

T1. . . . . T8 B + B + D - Data (ternary)
M1, M2 Service Data (ternary)
SW1, SW2 Synchronizing Word

Maintenance and service channel.

The ternary symbols M1 and M2 represent non-scrambled data that can be transmitted at a rate of 1 kBaud. Those symbols are used for various purposes:

- Maintenance Channel (control test loops (LT → NT) and frame errors (LT → NT)
- Service channel (transparent user data and transmit messages from NT to LT)

Encoding.

The encoding of a binary bit stream is made such that 4 binary bits correspond to 3 symbols of ternary symbol stream. The encoding follows the rules of modified monitoring state 43 (MMS43).

COMMAND / INDICATE CHANNEL (A bits)

Command/Indicate codes are define depending on the mode selected (LT or NT).

NT mode COMMANDS (DIN)

ACT	1 0 0 0	Activate. Layer 1 is activated at the UK0 interface starting with a 'wake-up' signal INFO U1W, followed by INFO U1A during synchronization and closed by INFO U1 when synch is gained.
AW	0 0 0 0	Awake. Set the module interface from the power-down to the power-up state. No signal is emitted at UK0 interface. Even DIN pin pulled LOW can have the same effect.
DC	1 1 1 1	Deactivation confirmation. The module interface is deactivated. The transmitter is disabled but the receiver is still enabled to recognize an awake signal. THe UIC is set in power down state.
RES	1 1 0 1	Reset. Reset the UIC to the initial state.
SY	1 1 0 0	Synchronize. Drive the UIC in connect through from module interface to line interface.

Remark: Executing the command RES (1101) is functionally equivalent to pulling the RESETN pin (6) LOW, with one exception:

a) RES command set pin DISS to HIGH (+5V)
b) pulling RESETN LOW set pin DISS to LOW (0V).

NT mode INDICATION (DOUT)

ACT	1 0 0 0	Activate. The synchronous state of the receiver is reached.
DC	1 1 1 1	Deactivation confirmation. The transmitter is disabled but the receiver remains enabled to detect awake signals at UK0 UIC is set in power down state.
DEAC	0 0 0 0	Deactivate. A request to deactivate INFO U0 has been detected.
CT	1 1 0 0	Connection Through. The UIC is fully activated.
CTL2	1 1 1 0	Connection through with loop 2. A loop 2 command has been detected at UK0.
L2	1 0 1 0	Loop 2. Synchronization has been reached during a Loop 2 activation procedure.
RSYN	0 1 0 0	Resynchronization. The receiver has lost framing and is attempting to resynchronize.

LT mode COMMANDS (DIN)

ACT	1 0 0 0	Activate. UIC is set in power-up state, executing the complete activation of Layer 1. The transparent channel transmission is enabled.
AL	1 0 0 1	Analog Loop. The analog transmitter output is looped back to the receiver input which is disconnected from UK0 interface. A pseudo wake-up procedure is executed.
L2	1 0 1 0	Loop 2. Command to close Loop 2 in NT.
LTD	0 0 1 1	Line Transmission Disabled. UIC stops transmitting signals on the line and is powered down.
DEAC	0 0 0 0	Deactivate. Request to deactivate UK0.
RES	1 1 0 1	Reset. Reset the UIC to the initial state.
SSP	0 1 0 1	Send Single Pulse. The UIC transmits single pulse at 1 ms time intervals with alternate polarity.

LT mode INDICATION (DOUT)

ACT	1 0 0 0	Activation running. UIC is powered-up and the activation procedure is running.
RDS	0 1 1 1	Running Digital Sum. Given during activation procedure. The receiver has reached synchronization.
CT	1 1 0 0	Connection Through. Layer 1 activation procedure has been completed. B and D channels are transparently connected.
DEAC	0 0 0 1	Deactivation running. UIC is deactivating in response of a DEAC, RES or LTD command.
DC	1 1 1 1	Deactivation confirmation. UIC has completed the deactivation procedure.
RSYN	0 1 0 0	Resynchronization. The receiver has lost framing and is attempting to resynchronize.
HI	0 0 1 1	High Impedance. When pin PFOFF is HIGH indication HI is output and UIC starts transmitting INFO U0. Normally used to indicate that remote feeding has been switched off.

POWER DOWN STATE

Power consumption of most functions is reduced; module interface is not active; C/I messages cannot be exchanged.

ACTIVATION DEACTIVATION

The ACTIVATION procedure consists of three steps: AWAKE, SYNCHRONIZE and CONNECT THROUGH.

Activation times are (max):

COLDSTART 1 sec

WARMSTART 170 msec

The DEACTIVATION procedure consists of two steps: line DEACTIVATION and POWER DOWN.

Deactivation time is (typ) 4 ms.

OSCILLATOR

Oscillators of 15.36 MHz are required. When in NT a tollerances of +/-30 ppm is allowed, it is advisable to use in LT a tollerances of +/-20 ppm.

LINE RANGE

The LINE RANGE depends on the cable section. Typically:

up to 4.2Km with 0.4mm cable

- 5.5Km - 0.5mm -
- 8.0Km - 0.6mm -

Assumed noise level for such performances is 10uV/SQRT(Hz) on a 200KHz bandwidth.

LT CLOCK JITTER

The phase jitter between Master Clock (15.36MHz) and interface clock (4.096MHz) should not exceed 50ns.

ELECTRICAL CHARACTERISTICS

Supply Voltages:

DVDD = 5V +/- 5%

AVDD = 5V +/- 5%

AGND = 2.5V +/- 5% (max curr 0.25mA)

Power consumption

Active = max 280mW (line loaded at 150Ohm)

Power down = max 30mW

DIGITAL INTERFACE STATIC CHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		3.5			V
V_{IL}	Low Level Input Voltage				1.0	V
V_{OH1}	High Level Output Voltage all outputs except DOUT	I_{OH1} = 0.4mA	V_{DD}-0.66			V
V_{OH2}	High Level Output Voltage DOUT, (Open Drain)	R to DV_{DD} R = 1KΩ	4			V
V_{OL1}	Low Level Output Voltage all outputs except DOUT	I_{OL1} = 0.4mA			0.33	V
V_{OL2}	Low Level Output Voltage DOUT, (Open Drain)	I_{OL1} = 0.7mA			0.4	V
C_{IN}	Inputs Capacitance, all inputs at DOUT if output is off				10 10	pF pF
C_{OUT}	Load Capacitance at all outputs except at DOUT				25	pF
C_{OUT}	Load Capacitance at DOUT				150	pF
I_{IN}	Input Leakage Current				1	µA

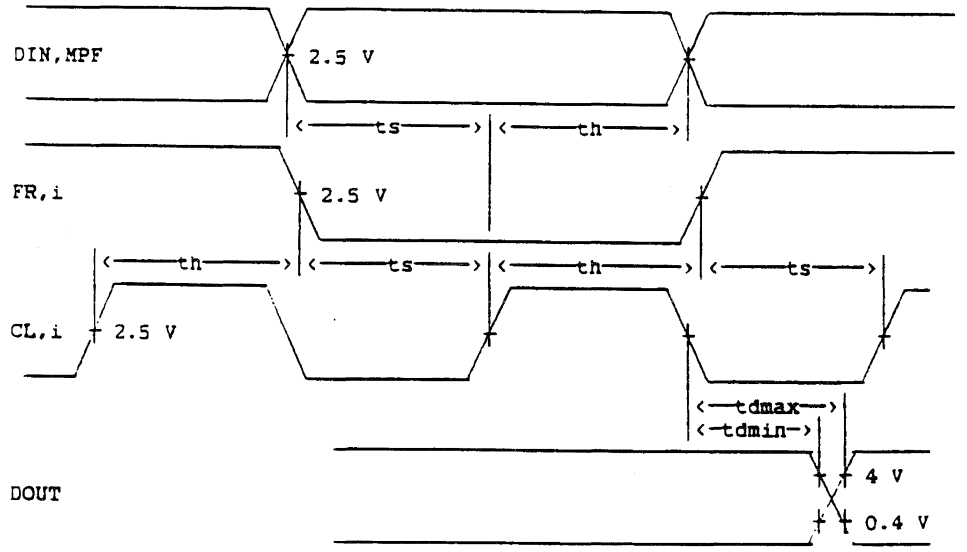
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS

Burst mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL	1.0V	3.5V	10			30
Fall Time tf	FR, CL	3.5V	1.0V	10			30
Setup Time ts	FR	FR, i –	CL, i +			30	
Setup Time ts	FR	FR, i +	CL, i +			30	
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Hold Time th	FR	CL, i +	FR, i –			50	
Hold Time th	FR	CL, i +	FR, i +			50	
Hold Time th	DIN	CL, i +	DIN +/–			60	
Hold Time th	MPF	CL, i +	MPF +/–			60	
Delay Time td	DOUT	CL, i –	DOUT +/–	50	1	0	150
Delay Time td	DOUT	CL, i –	DOUT +/–	150	1	0	200
Clock Width tc	CL, i	CL +/–	CL +/–			239	249
Clock Width tc	CL, i	CL +/–	CL –/+			100	144

+ = rising edge

– = falling edge



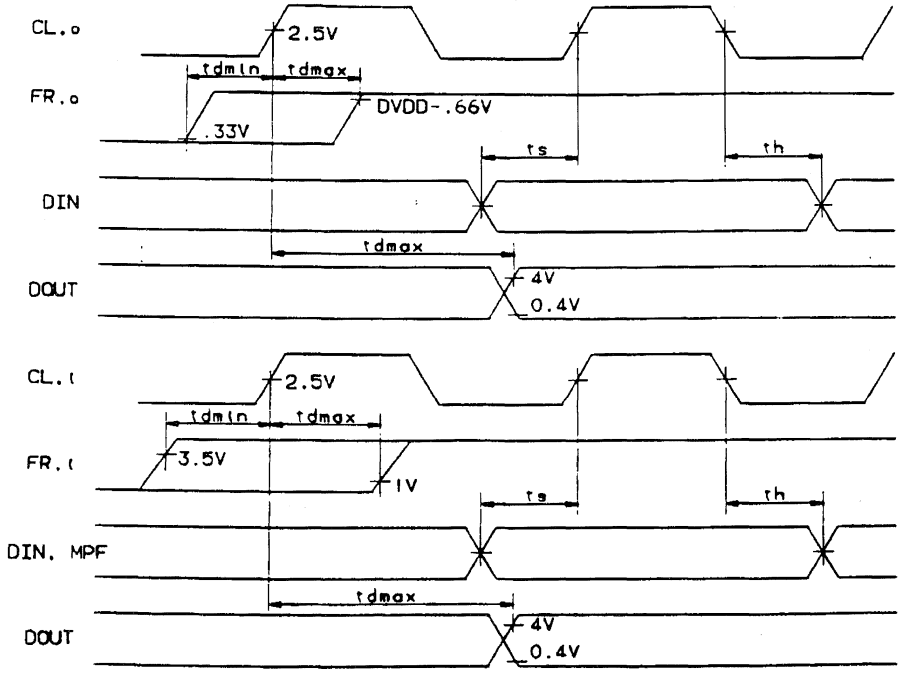
DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Continuous mode.

Parameter	Port	from	to	Conditions		Min.	Max.
				C	R to DVDD		
				pF	KΩ	ns	ns
Rise Time tr	FR, CL, i	1.0V	3.5V	10			30
Fall Time tf	FR, CL, i	3.5V	1.0V	10			30
Rise Time tr	FR, CL, o	10%	90%	25			30
Fall Time tf	FR, CL, o	90%	10%	25			30
Setup Time ts	DIN	DIN +/–	CL, i +			50	
Setup Time ts	MPF	MPF +/–	CL, i +			50	
Delay Time td	FR	CL, i +	FR, i +			-200	200
Hold Time th	DIN	CL, i –	DIN +/–			100	
Hold Time th	MPF	CL, i –	DIN +/–			100	
Delay Time td	DOUT	CL, i +	DOUT +/–	25	10		500
Setup Time ts	DIN	DIN +/–1	CL, o +			50	
Setup Time th	DIN	CL, o –	DIN +/–			100	
Delay Time td	DOUT	CL. o +	DOUT +/–	25	10		500
Delay Time td	FR	CL, o +	FR,o +	25		-150	150
Clock Width tc	CL, i	CL +/–	CL +/–			1830	2080
Clock Width tp	CL, i	CL +/–	CL +/–	25		1830	2080
Pulse Width tp	CL, i	CL +/–	CL –/+			850	1100
Pulse Width tp	CL, i	CL +/–	CL –/+	25		850	1100

+ = rising edge

– = falling edge



DIGITAL INTERFACE DYNAMIC CHARACTERISTICS (continued)

Master clock.

Parameter	Port	from	to	Conditions		Min.	Max.
				C			
				pF		ns	ns
Rise Time tr Fall Time tf	XTAL2 XTAL2	1.0V 3.5V	3.5V 1.0V	10 10			15 15
Rise Time tr Fall Time tf	CLS CLS	10% 90%	90% 10%	25 25			15 15
Pulse Width	CLS	CLS +/–	CLS –/+	25		20	

+ = rising edge

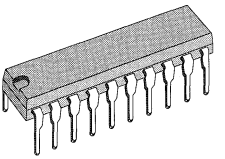
– = falling edge

Setup Time ts Hold Time th Delay min. td Delay max. td	DIN, FR, i +/– CL, i + CL, i + CL, i – CL, i + CL, i –	2.5V 2.5V 2.5V 2.5V	CL, i + DIN, FR, i +/– DOUT +/– DOUT +/–	2.5V 2.5V 0.4 / 4V 4 / 0.4V
Delay min. td (negative) Delay max. td	CL, i + CL, i +	2.5V 2.5V	FR, i + FR, i +	3.5V 1V
Setup Time ts Hold Time ts Delay max. td Delay min. td (negative) Delay max. td	DIN, +/– CL, o + CL, o + CL, o + CL, o +	2.5V 2.5V 2.5V 2.5V 2.5V	CL, o + DIN +/– DOUT +/– FR, o + FR, o +	2.5V 2.5V 4 / 0.4V 0.33V VDD - 0.66V
Pulse Width tp Clock Width tc	CL, o +/– CL, o +/–	2.5V 2.5V	CL, o –/+ CL, o +/–	2.5V 2.5V
Pulse Width tp Clock Width tc	CLS, MXCL +/– CLS, MXCL +/–	2.5V 2.5V	CL, o –/+ CL, o +/–	2.5V 2.5V

SID-μW : S/T INTERFACE DEVICE WITH MICROWIRE/DSI

ADVANCE DATA

- SINGLE CHIP 4 WIRES 192 KBIT/S TRANSCEIVER, PROVIDES ALL CCITT I.430 LAYER 1 FUNCTIONS
- ISDN BASIC ACCESS HANDLING 144KBIT/S 2B + D TRANSMISSION
- 4 SELECTABLE DIGITAL SYSTEM INTERFACE (DSI) FORMATS
- MICROWIRE™ μW COMPATIBLE SERIAL CONTROL INTERFACE
- EXCEEDS I.430 RANGE : AT LEAST 1.5KM POINT-TO-POINT AND 200M POINT-TO-MULTIPOINT
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S&Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- OPERATING POWER CONSUMPTION < 75mW
- STAND-BY POWER CONSUMPTION < 3mW
- EASILY INTERFACEABLE WITH ST5075/6, ST5451



DIP20

DESCRIPTION

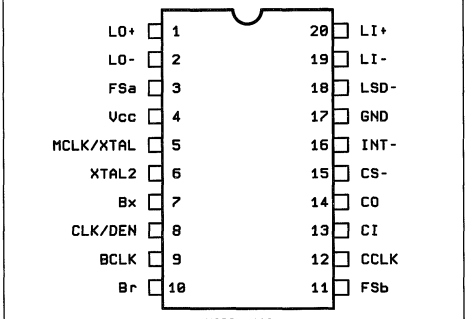
The ST5420 (SID-μW) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on SGS-THOMSON Microelectronics double metal advanced HCMOS3A process, and requires only a single + 5V supply. All functions specified in CCITT recommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, the ST5420 provides the 800b/s S & Q multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by ST5420, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters. Adaptive receive signal processing enables the device to operate with low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations.

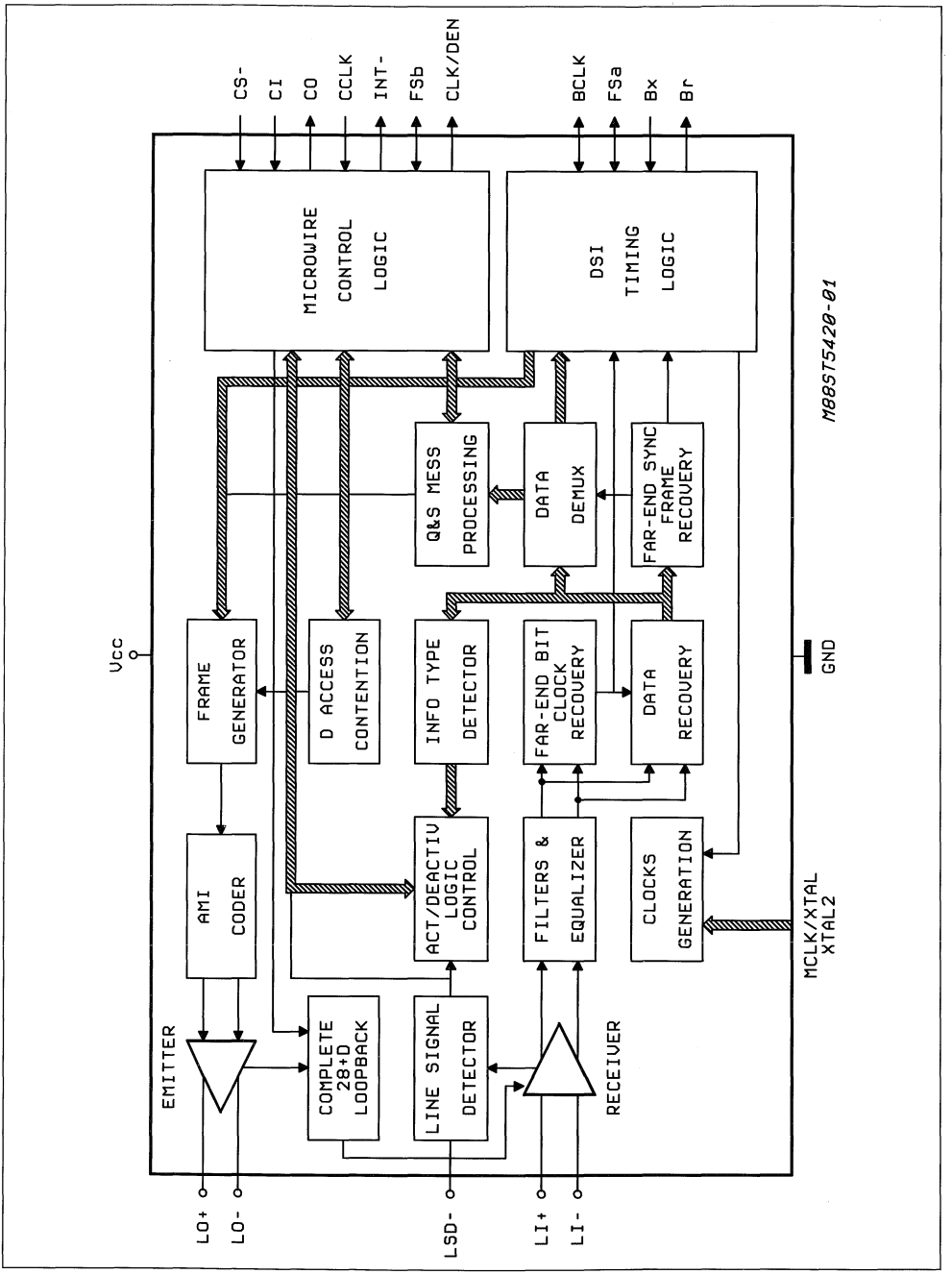
Far-end Clock Resynchronizer and data buffer allow design of NT2 equipment connected to several T interfaces with a minimum external circuitry. Several different Digital Interface formats provide maximum flexibility for 2 B + D basic access data transfer with a minimum pin count. The SID μW programmable functions can be set and controlled via a serial control channel MICROWIRE compatible. The Digital System Interface (DSI) is used for the transfer of "B1", "B2" and "D" channels data.

PIN CONNECTION



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



PIN DESCRIPTION

Name		Description
LO+, LO-	1, 2	ransmit AMI signal differential outputs to the S line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
FSa	3	In NT modes and TE mode DSI Slave, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into Bx. In TE mode DSI Master only, this pin is a digital output pulse which indicates the start of the 'B' channel data transfer at both Rx and Br.
V_{CC}	4	Positive power supply: must be +5V ±5%
MCLK/XTAL	5	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with $R_S < 100\Omega$) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	Crystal Oscillator Output: should be connected to one of the crystal, if used.
Bx	7	Digital input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
CLK/DEN-	8	**CLK** TE mode DSI slave selected: This pin is a clock signal output phased-locked to the received line signal and can be considred as the far-end clock reference. CLK is a clock signal compatible with the bit clock timing of the DSI format selected: 2.048MHz, 256KHz, 1536KHz or 2.56MHz. **DEN** TE mode DSI master selected: This pin is a normally low output which pulses high to indicate the active bit times for D channel data transmitted at the Bx input. It is intended to be gated with BCLK bit clock to control the shifting of D channel data from a Layer 2 device to the ST5420 transmit buffer. By use of the ST5451 HDLC controller, no external circuitry is needed.
BCLK	9	Bit Clock: set the data shift rate for 'B' and 'D' channel on the digital interface side. When NT mode or TE mode Digital System Intrface (DSI) Slave is selected, BCLK is an input which may be anymultiple of 8KHz from 256KHz to 4.096MHz. It need not be synchronous with MCLK. In TE mode DSI Master this pin an output clock with the frequency depending on the interface format selected. It is synchronous with the data on Bx and Br pins and is phase-locked to the received line signals. Depending on the DSI format choosen BCLK can assume 4 different values: DSI format 1: 2048KHz DSI format 2: 256KHz DSI format 3: 512KHz DSI format 4: 2560KHz
Br	10	Digital output: data is shifted out from the Tri-state Br during the assigned time slots. Elsewhere, Br is high impedance, 2B + D data is shifted out at the BCLK frequency on the transmit rising edges of BCLK except in format 3 wich has a timing GCI compatible. In format 3, data is shifted out at half the BCLK frequency on the transmit rising edges of BCLK.
FSb	11	In NT modes and TE mode DSI Slave, this pin is the Receive Frame Sync. pulse input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data out from Br. In TE mode DSI Master only this pin is an 8 bit wide pulse which indicates the active slot for the B2 channel on the digital interface.
CCLK	12	Clock input for the MICROWIRE control channel.
CI	13	MICROWIRE control channel serial data input.
CO	14	MICROWIRE channel serial data output for status information. When not enabled by CS-, this output is Tri-state.
CS-	15	Chip Select Input: When pulled low enables the control channel data to be shifted in and out. When high, this pin inhibits the control interface.
INT-	16	Interrupt output: A latched output signal, normally Tri-state, that goes low to indicate a change of status of the loop transmission system.

PIN DESCRIPTION (continued)

Name		Description
GND	17	Negative power supply: normally 0V (ground). All analog and digital signals are referred to this pin.
LSD-	18	The line signal detect output, normally Tri-state pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is disabled when the device is powered up.
LI-, LI+	19, 20	Receive AMI signal inputs from the S line transformer: A 1:2 step-up transformer should be used identical to the transmit side. The LI- pin is connected to the intrnal voltage reference at 2.5V and must be decoupled to GND with a 10µF capacitor in parallel with a 0.1µF ceramic capacitor. To ensure the receive input impedance I.430 spec even if power is lost, it is necessary to add 3 external resistors between the transformer and the LI+, LI- pins.

FUNCTIONAL DESCRIPTION

POWER-ON INITIALIZATION

Following the initial application of power, ST5420 enters the power down de-activated state, where all the internal I.430 circuits, including the master oscillator, are inactive and in a low power state except for the line signal detect (LSD-) circuit.

When the SID is powered down and a line signal is detected LSD- pin pulls low.

Configuration mode programming of the SID has to be completed before a power up (PUP) instruction.

POWER UP

An instruction PUP on the MICROWIRE control interface is required to power up the SID.

Power up transition enables all analog and I.430 circuitry, starts the crystal oscillator and reset the state machine to the de-activated state inhibiting the LDS- output as well.

In TE mode DSI master selected, BCLK and FSa clocks are provided according to the format selected.

POWER DOWN

An instruction PDN on the MICROWIRE control interface is required to power down the SID.

PDN forces the device to the low power state without sequencing through any of the de-activation states. It should therefore only be used after the SID has been put in a known state, eg in the line de-activated state.

The power down transition disables analog and "I.430" circuitry, stops the crystal oscillator and all the clocks internally generated.

During power down, Configuration Registers remain in their current state and can be changed by the MICROWIRE control interface.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.
This coding rule requires that a binary ONE is represented by a 0V high impedance output, whereas a binary ZERO is represented by a positive or negative 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The line frame format used in the SID follows the CCITT recommendation specified in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity.

In Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B + D 144kbit/s basic access data, an echo channel, the E bit, which is used to retransmit back the D bits received from the TE (s), and three extra bits : FA, M and S.

In the TE to NT direction, the frame contains in addition to the 2B + D data, of an extra bit : FA.

FA, M and S bits are used to set up a Q multiframe channel in the TE to NT direction, and a S multiframe channel from NT to TE. These 800 bit/s message oriented channels are structured on the base of the United State ANSI standard specification for layer 1 maintenance.

Figure 1 : Inverted AMI Line-coding Rule.

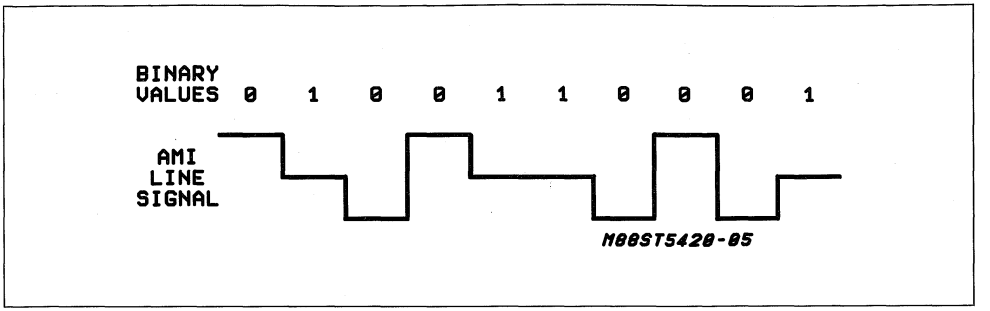
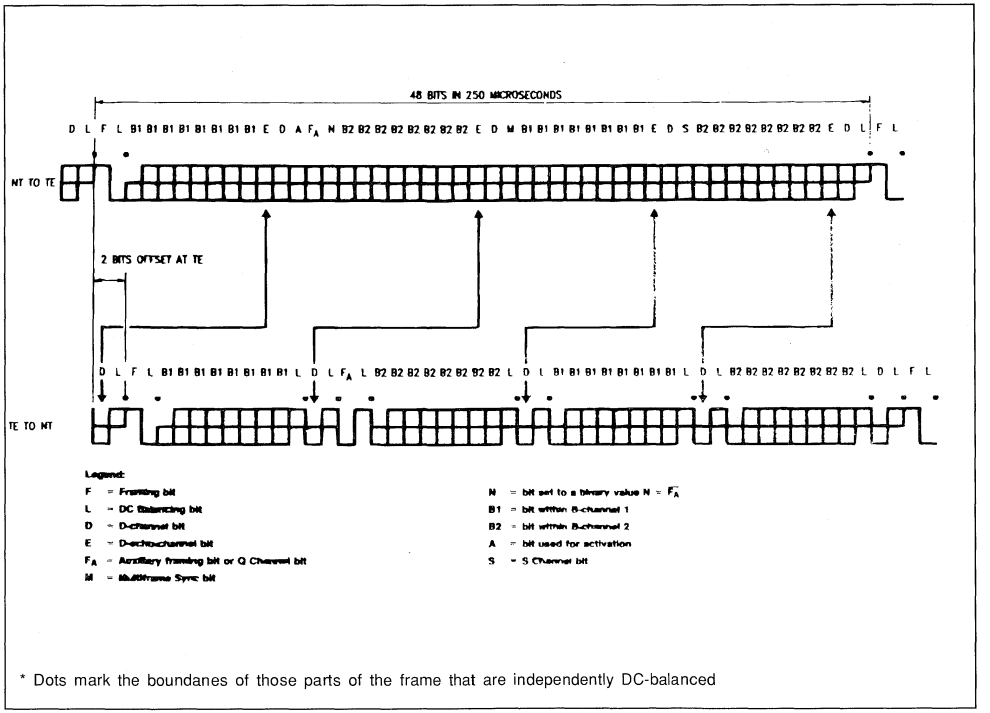


Figure 2 : Frame Format.



* Dots mark the boundanes of those parts of the frame that are independently DC-balanced

LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO– are designed to drive a transformer with an external termination resistor. A 2: 1 transformer, terminated in a 50Ω load, results in a signal amplitude of 750mV pK on the line and meets the I.430 pulse shape specification.

When driving 400Ω or 5.6Ω load, I.430 requirements are also respected.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430.
When driving a O+ or O– symbol, a voltage limited current source is turned on. Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+/ LO– by means of clocks respectively locked on the far-end received

bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from the FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1 : 2 transformer which may be of the same type used for the transmit direction.

At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance spec even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI– pins. Alternatively, a 1 : 1 transformer and 2 external resistors may be used. To correct pulse attenuation and distorsion caused by the transmission line in point to point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE mode or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes the Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, which can discriminate a valid line signal from noise, is enabled to detect the presence of incoming data if the far-end starts activation of the loop. LSD– output pulls low to wake up the equipment.

DIGITAL INTERFACES

The SID provides two digital interface for both control and basic access data transfer named MICROWIRE and DSI.

Digital System Interface (DSI): The Digital System Interface (DSI) combines B and D channel data onto common pins Bx and Br. Several multiplexed formats are available as shown figure 3. Selection is made via MICROWIRE. Direct connection among different ISDN devices can be provided.

At this interface, phase skew between Transmit and Receive directions may be accomodated at the Line Card or NT2 end since separate Frame Sync inputs FSa and FSb are provided. Each of these synchronizes a counter which gates the transfer of B1, B2 and D channels in the allocated Time-slots.

In NT2 or PBX equipments, the serial shift rate is determined by the BCLK input and may be any value from 256kHz to 4096kHz. Thus, the B and D channel slots can be interfaced to a TDM bus and assigned to the first 4 bytes wide Time Slots of the frame. Unused channels are high impedance.

In TE mode DSI master selected, FSa is an output indicating the start of both Transmit and Receive B and D channel data transfers. BCLK is also an output at the frequency of which is dependent on the Format selected :

in Format 1, BCLK = 2048KHz
in Format 2, BCLK = 256kHz
in Format 3, BCLK = 512kHz
in Format 4, BCLK = 2560KHz

Format 3 is GCI compatible excluding C/I and M channel transfer.

Except for Format 3, data is transmitted in both direction at the BCLK frequency. Data is shifted out from Br on the rising edges of BCLK and is shifted in on Bx on the falling edges of BCLK.

Control Interface (MICROWIRE) **:** A serial interface, which can be clocked independently from DSI, is provided for microprocessor control of various functions in the SID. All data transfers consist of a single byte shifted into the Control Register via the CI pin simultaneous with a single byte shifted out from the Status Register via the CO pin. Data shifts into CI on rising edges of CCLK and out from CO on falling edges when CS– is pulled low for 8 cycles of CCLK.

An interrupt output, INT– goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising CCLK edge after CS– goes low.

Tables 1 and 2 list the control functions and status indicators.

Status read. Whenever a change occurs in one or more of the conditions indicated in the SID Status Register, the INT– pin is pulled low. The "controller" device must service the interrupt before attempting to send a new command to the SID device. On the first rising edge of the CCLK after CS– goes low, the INT– pin from SID is cleared to the high impedance state.

The status bits are output on the CO pin. If the in-

terrupts for EOM status and MER status have been disabled then, these status are assumed not necessary and cannot be accessed.

Command write. If the "controller" needs to send a command to SID, it pulls CS– pin of SID low and transmits 8 bits of command on the 8 rising edges of CCLK. While the command bits are being transmitted, a SID status change could occur, but the resulting interrupt (if selected) will be inhibited until the CS– is cleared to the high state. The INT– will then go low, forcing an interrupt. The controller then forces a low level on the CS– input to access the status as described above.

When a command is being received on the CI pin, the CO pin outputs a "00000000" byte indicating a NOC "no change" status. It is possible to write in the SID on the CI pin while shifting out the status register onto CO.

Table 1 : Microwire Control Register Functions.

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Activatiotion/deactivation									
*Power Down	PDN	0	0	0	0	0	0	0	0
Power Up	PUP	0	0	1	0	0	0	0	0
Deactivation Request	DR	0	0	0	0	0	0	0	1
Info2 Transmit Request	FI2	0	0	0	0	0	0	0	1
Activation Request	AR	0	0	0	0	0	0	1	1
Device Mode:									
*NT Mode Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Mode DSI slave	TES	0	0	0	0	0	1	1	0
TE Mode DSI Master	TEM	0	0	0	0	0	1	1	1
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
Digital Interface Format:									
* DSI Format 1	DIF1	0	0	0	0	1	0	0	0
DSI Format 2	DIF2	0	0	0	0	1	0	0	1
DSI Format 3	DIF3	0	0	0	0	1	0	1	0
DSI Format 4	DIF4	0	0	0	0	1	0	1	1
B channel Configuration:									
*B Channel Mapped Direct	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
D Channel Access:									
D Channel Request Class 1	DREQ1	0	0	0	0	1	1	1	0
D Channel Request Class 2	DREQ2	0	0	0	0	1	1	1	1

(*) indicates initial state following power on initialization.

Table 1 : Microwire Control Register Functions (continued).

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
End of Message Indication:									
*EOM Indication Enabled	EIE	0	0	0	1	0	0	0	0
EOM Indication Disabled	EID	0	0	0	1	0	0	0	1
Multiframe Processing:									
*Multiframe Disabled	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
*Enable 3X Checking	EN3X	0	0	1	0	1	0	0	0
Disable 3X Checking	DIS3X	0	0	1	0	1	0	0	1
Loopback Test Mode:									
*Clear All Loopbacks	CAI	0	0	0	1	1	0	1	1
Loopback B1 on DSI Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on DSI Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2 B + D Enabled	LSB	0	0	0	1	1	0	1	0
Loopback B1 on Line Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on Line Enabled	LBB2E	0	0	0	1	1	1	0	1

(*) indicates initial state following power on initialization.

Table 2 : Microwire Status Register Functions.

Functions	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
No Change	NOC	0	0	0	0	0	0	0	0
Line Signal Detected	LSD	0	0	0	0	0	0	1	0
Activation Pending	AP	0	0	0	0	0	0	1	1
End of Message on D Channel	EOM	0	0	0	0	0	1	1	0
Lost Contention	CON	0	0	0	0	0	1	1	1
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4
Activation Indication	AI	0	0	0	0	1	1	0	0
Line Error Indication	EI	0	0	0	0	1	1	1	0
Deactivation Indication	DI	0	0	0	0	1	1	1	1

Figure 3a : DSI Formats Master.

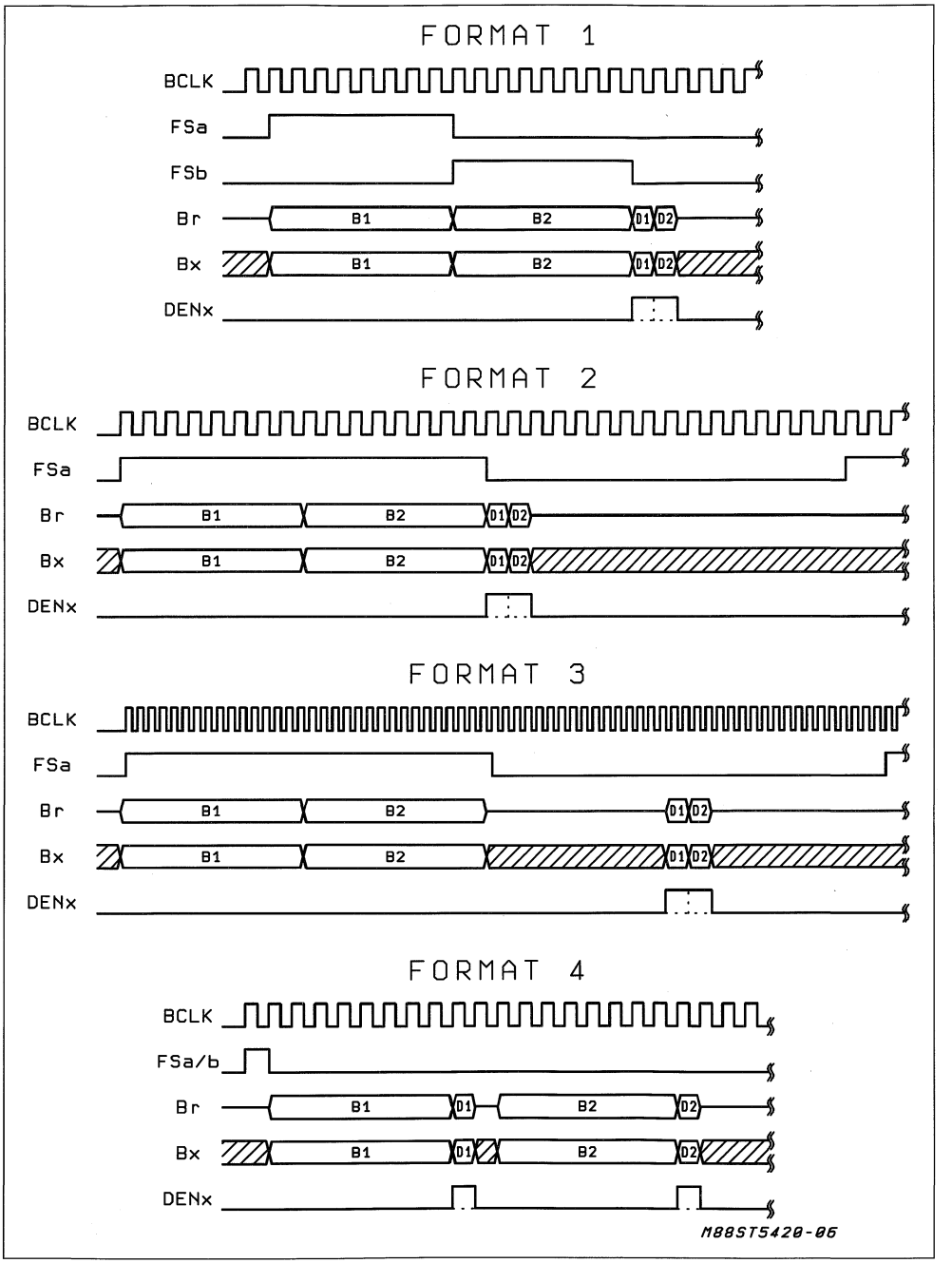
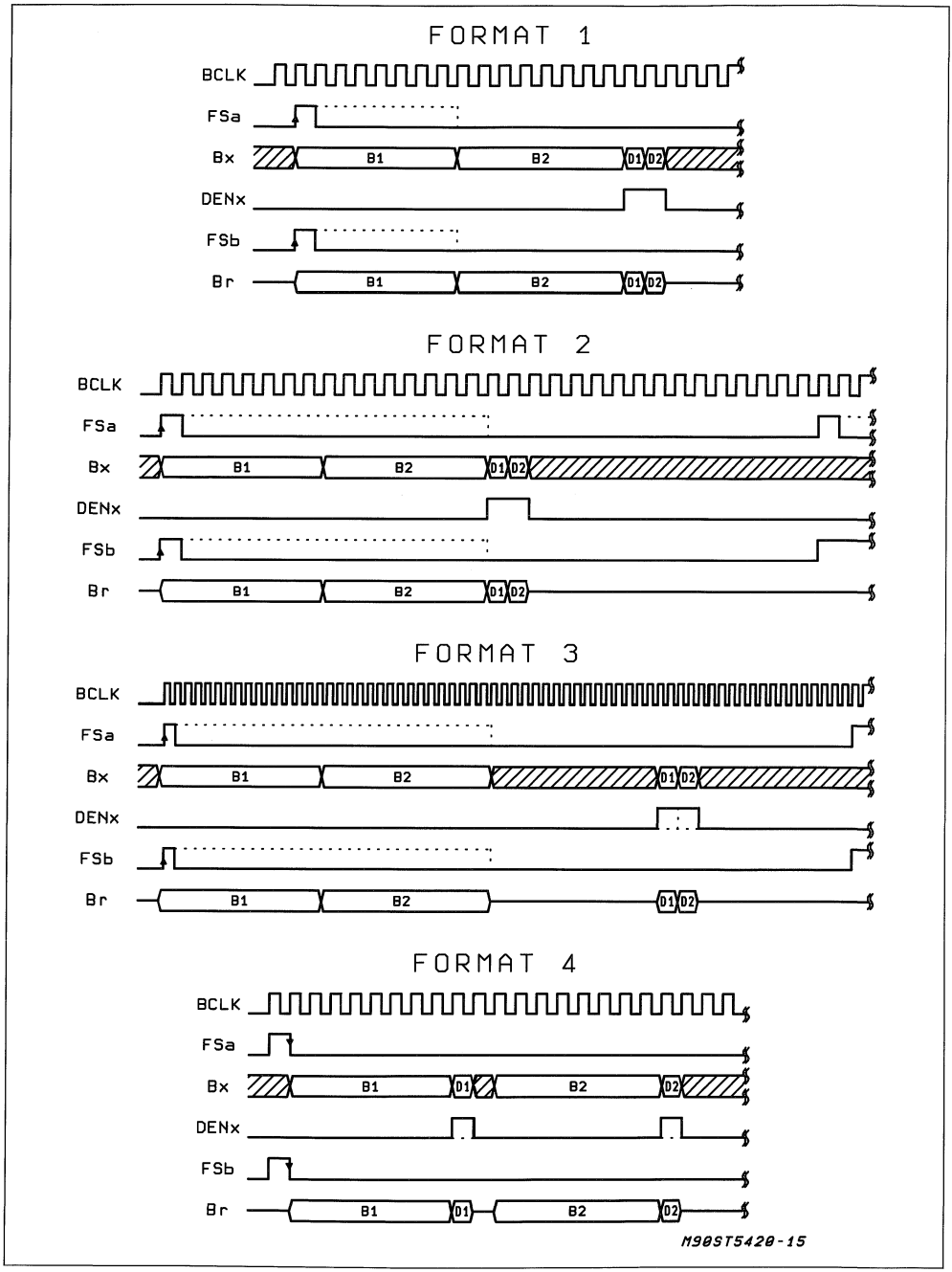


Figure 3b : DSI Formats Slave.



CONTROL FUNCTIONS DESCRIPTION

ACTIVATION/DEACTIVATION

PUP : Power Up. The Power Up command enables all analog circuitry, starts the XTAL and resets the state machine to the deactivated state enabling INFO0 transmission. It also inhibits the LSD–output.

PDN : Power Down. The Power Down command immediately forces the device to a low power state, without sequencing through any of the deactivation states. It should therefore only be used after SID has been put in a known state.

DR : Deactivation Request. The Deactivation Request command forces the device through the appropriate deactivation sequence specified in I.430. In TE mode, is equivalent to a Timer Expiry instruction.

AR : Activation Request. The Activation Request initiates the specified Activation sequence. It is recommended that an AR be delayed at least 2ms after the device is powered up.

FI2 : Force Info2. Being in the activated state G3, the RSY instruction forces the SID through the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, RSY instruction has no effect. Should be used in NT mode only in NT1 equipment. On loss of signal received from the line, the SID sends INFO2 on the line.

Command. An activation being in progress, a second AR command allows the SID through the appropriate sequence to send INFO4 on the line. Should be used in NT mode only in NT1 equipment. In that revision only.

DEVICE MODE

NTA : NT Mode Adaptive Sampling. In NT mode, Adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters of each other (depending on cable capacitance as indicated in I.430). Transmit section of the SID is phased locked to the DSI FSa signal.

NTF : NT Mode Fixed Sampling. In NT mode, Fixed sampling should be selected when the device is in an NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section of the SID is phased locked to the DSI FSa signal.

TES : TE Mode DSI slave. This mode should be selected when the device is used on the T side of an NT2 equipment. The I.430 circuitry operates as in the TE mode but the DSI interface is then driven by BCLK and FSa sources in the NT2.
Data buffers and a clock resynchronizer enable the Digital Interface to function with jittering sources for FSa and BCLK.
A clock signal output phased locked to the Receive line signal is delivered on CLK in a mode depending on the reference clock generation configuration selected.
All D channel access control circuitry is disabled.

TEM : TE Mode DSI Master. This mode should be selected when the device is in a Terminal. The SID is then the source of the BCLK and FSa signals. Access to the Transmit D channel, including the priority and contention resolution control, is enabled.

MMA : Monitoring Mode Activation. The SID being selected previously in the TEM mode, the MMA command allows the device to receive and activate on INFO3 frames, while being the master of the Digital System Interface. That mode can be used for applications such as outputs monitoring of TEs on a Passive Bus via a "dummy" NT.
The MMA mode can be disabled by any configuration command : ie TEM.

B CHANNELS CONFIGURATION

BDIR/BEX/B1E/B1D/B2E/B2D. BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels.

When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line in those B channel bit positions regardless of data at the Bx input, meanwhile being Br output in high impedance state. When enabled by means of the B1E and B2E instructions, B channels are transparently transmitted.

D CHANNEL ACCESS

DREQ1/DREQ2. The instructions DREQ1 and DREQ2 are a request from the layer 2 to the SID selected in TE mode to attempt to access the transmit D channel at the S interface. The correct priority class for the pending message must also be selected : 8 or 9 selected with DREQ1 and 10 or 11 selected with DREQ2.

END OF MESSAGE INDICATION

EIE/EID. In TE configuration, the End of Message Status indicator sending can be enabled by means of the instruction EIE and disabled by means of the instruction EID.

MULTIFRAME PROCESSING

MID/MIE/MFT/MFR. The multiframe channel processing must be enabled by an MIE instruction and an MID instruction must be used to disable. In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S1, S2, S3 and S4 respectively.

In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR status message is autonomously sent from the SID in which M1, M2, M3 and M4 bits represent the Q1, Q2, Q3 and Q4 or S1, S2, S3 and S4 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.XYZ.198Y. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by the SID when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT mode.

DIS3X/EN3X. When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical. When DIS3X is set, Multiframe messages are transferred transparently every superframe.

LOOPBACK TEST MODES

LBS/LB1E/LBB1E/LB2E/LBB2E/CAL. Three classes of loopback mode are available on the SID selected by the appropriate Control Instruction. LBS set a the loopback of the 2B + D channels from the Bx input to the Br output. It may be set when the device is either activated, in which case it is transparent or when it is deactivated in which case it is non-transparent.

LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1E and LBB2E instructions turn each individual B channel from the Digital Interface received input back to the Digital Interface transmit output. They may be set separately or together.

CAL instruction clears all the loopbacks simultaneously.

STATUS INDICATORS DESCRIPTION

NOC : No Change. The status indicator NOC is transmitted from CO output during a Control Access on MICROWIRE interface when no change has occured.

LSD : Line Signal Detection. If set, indicates that the far-end of the line is attempting to activated the interface. May be used as an alternative to the LSD– pin to wake up a microprocessor.

AP : Activation Pending. If set in NT mode, indicates that INFO1 frames have been identified on the line. The SID is waiting for an Activation Request instruction to send INFO2.

If set in TEM or TES mode, indicates that INFO2 (or INFO4) frames have been identified on the line when the following events occur :

- being in the TE deactivated state, detection of INFO2 or INFO4
- being in the TE loss framing state F8, detection of INFO2

EOM : End Of Message. In TE configuration, set when the closing flag of a D channel message has been transmitted by a TE on the S interface indicating successful completion of a packet. The Interrupt associated with this indicator can be disabled via the Control Instruction EID if desired.

CON : Lost Contention. Set when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit indicating a lost contention. D channel access attempt is deactivated at the S interface. A new DREQ1 or DREQ2 instruction is needed to restart the procedure.

AI : Activate Indication. If set, indicates that the S interface has received INFO3 or INFO4.

EI : Error Indication. If set in the TE mode, indicates

If set in the NT mode, indicates that a loss of frame synchronization is detected on the line.

DI : Deactivate Indication. If set, indicates that the S interface has been deactivated.

ACTIVATION/DEACTIVATION

NT Mode. After power on initialization, the SID can be configured in NT power down mode, depending on register configuration setting. The SID is powered up by means of the PUP instruction.

Activation may be initiated from either end of the loop. To operate an activation from the Network, the device must be first powered up by the appropriate instruction followed at least 2ms later by an AR instruction. Network timing : FSa, BCLK and MCLK if provided must be present at this time.

When the activation is initiated by the far-end, the SID being in the Power Down state, a Line Signal Detector pulls low the LSD– and INT– pins, either of which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie INFO1. The appropriate procedure is then followed according to I.430. The detailed description is given in figure 4.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request to the SID should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force de-activation. Timer 2 which is specified to prevent unintentional re-activation, is not required since the SID can uniquely recognize INFO1 frames.

TEM or TES Mode. After Power on initialization, the SID can be configurated in TEM or TES side power down mode, depending on register configuration setting. The SID is powered up by means of the PUP instruction.
Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate instruction followed at least 2 ms later by an AR instruction. When the activation is initiated by the far-end, the SID being in the Power Down state, a Line Signal Detector pulls low the LSD– and INT– pins, either of which can be used to wake up the system. A Power Up instruction must then be issued allowing identification of received signal ; INFO2. The appropriate procedure is then followed according to I.430. The detailed description is given in figure 5.

I.430 recommends that a Timer should be available in an TE. An Activation Request to the SID should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation.

Figure 4 : Activation Procedure NT Selected.

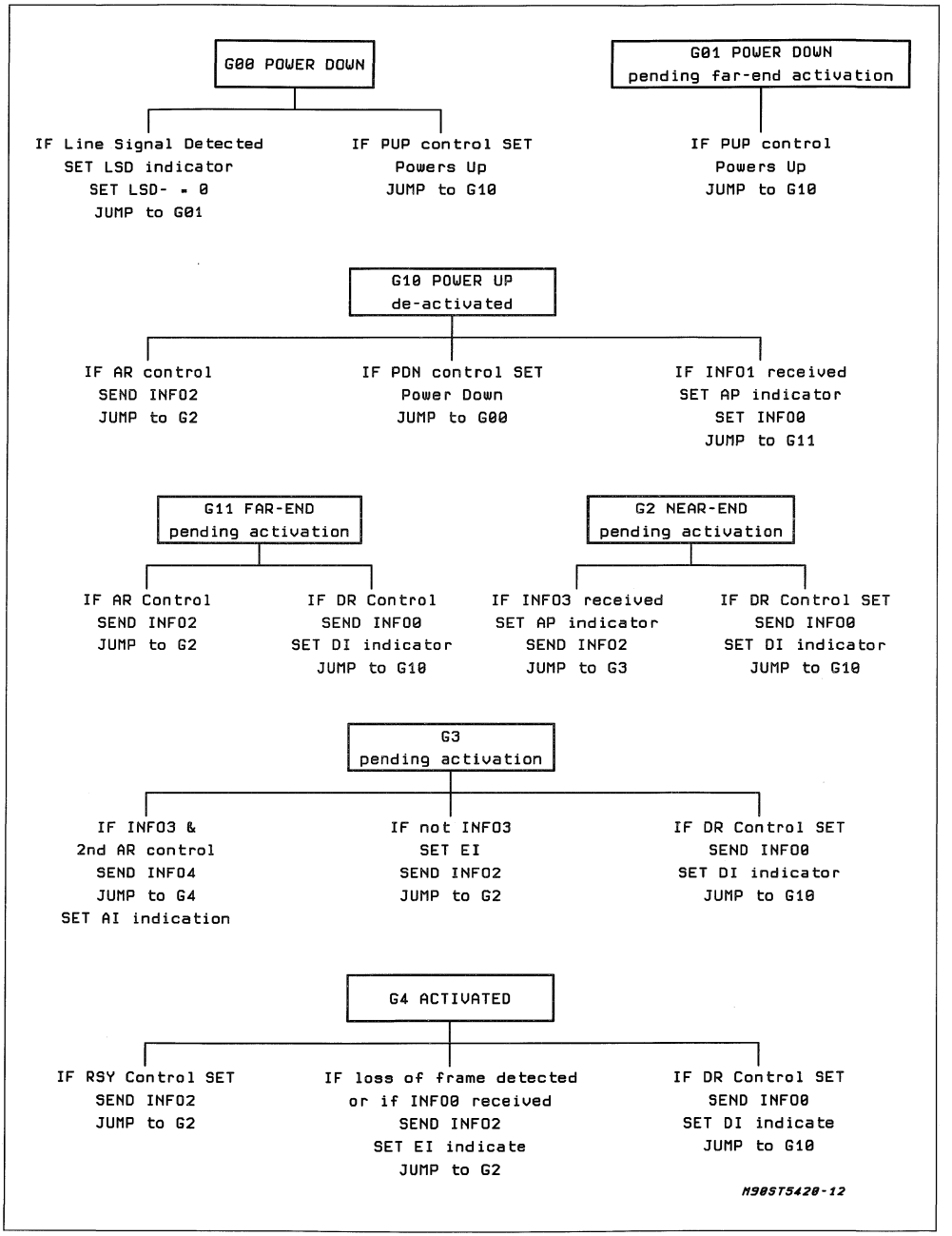


Figure 5 : Activation Procedure TE Selected.

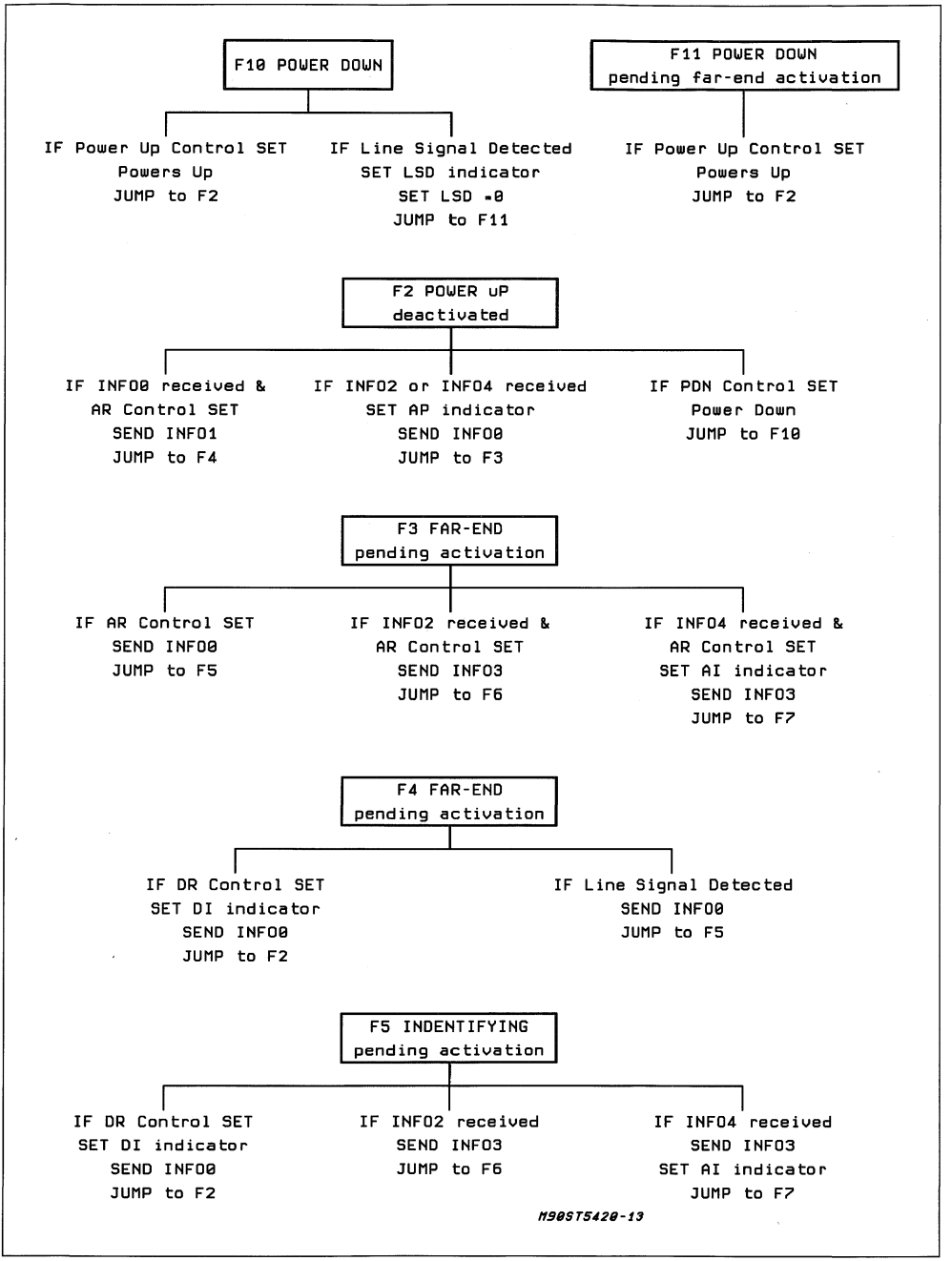
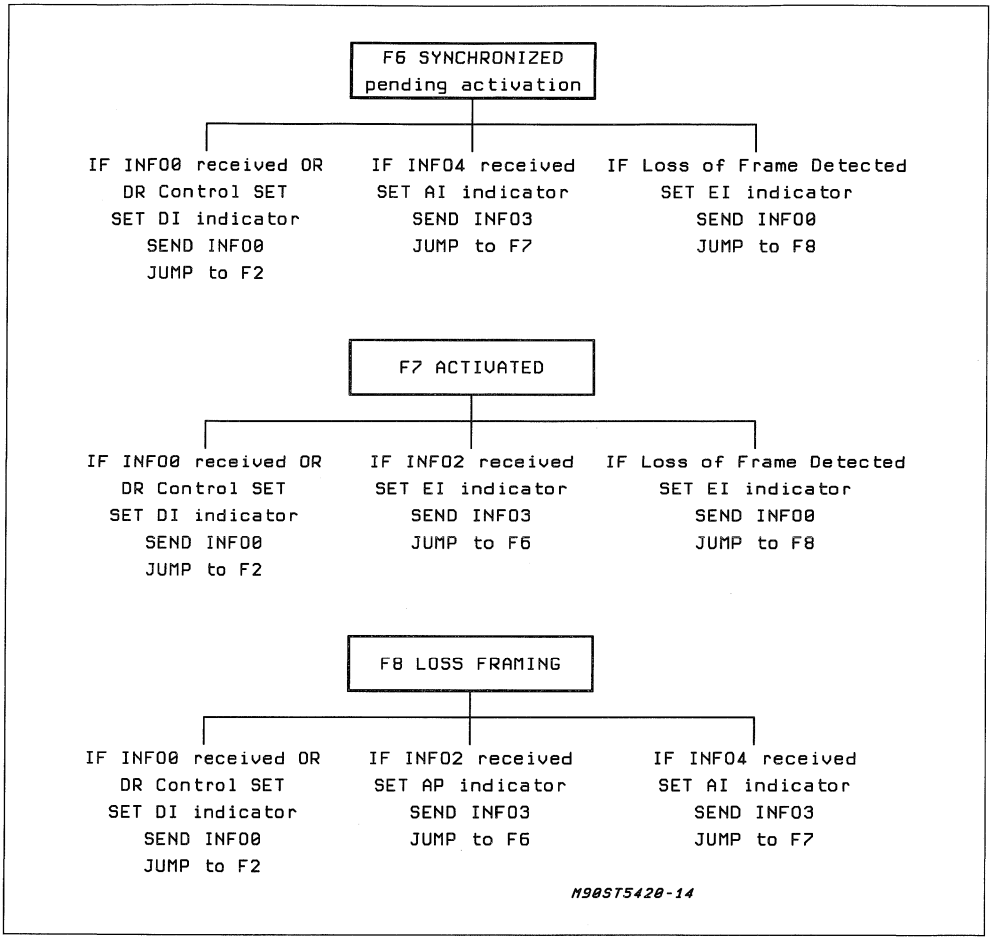


Figure 5 : Cont'd Activation Procedure TE Selected.



D Channel Access in TEM Mode. In TEM mode, the SID arbitrates access for Layer 2 HDLC frames to the D channel bit positions on the line in accordance with the I.430 Priority Mechanism for Signalling and Packet Priority Classes. The shifting of D channel Transmit data from the Controller into the SID buffer is controlled by DEN output which can be gated with the Digital Interface Bit Clock BCLK.

After Power initialization, DEN output pulses are inhibited and no D channel data is shifted into the Bx input.

A Controller device requiring to start transmission of a packet on the line should first activate the line by the appropriate procedure. Then it should prime its Transmit Buffer such that the opening Flag is ready to be shifted accross the Digital interface. Then a Control Instruction DREQ1 or DREQ2 will initiate the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

In response to the DREQ instruction, the DEN output is immediately enabled to prefetch the opening Flag from the Controller device into the SID D channel Buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assumed by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the

value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit Buffer, to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1" has been counted, the leading 0 of the opening flag is transmitted in the next D bit position towards the NT. Then, DEN pulses are also re-enabled in order to shift D channel bits from the Controller into the SID Transmitter buffer. No interrupts are necessary for local flow control between the Controller and the SID.

During transmission in the D channel, the SID continues to compare each E bit received from the NT with the D channel bit previously transmitted before proceeding to send the next D bit. In the event of a mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore stops and "1"s are transmitted in all following D bit positions. Status indication type CON is set and the INT– output is pulled low to interrupt the Controller. DEN output pulses are again inhibited.

In order to retransmit the lost frame, the Controller must begin as before by priming again its Transmit Buffer with the packet header and writing a new DREQ instruction into the Control Register.

Successful completion of a Transmit frame is detected by the SID when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions, with the DEN output held low to prevent further transfer of Data from the Controller. If enabled by the Control Instruction EIE, the INT output is pulled low with status indicator EOM set to indicate the End of message.

In order to transmit a new frame, the Controller must begin as before.

POWER SUPPLIES

While the pins of the ST5420 SID device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1µF should be connected from this common point to V_{CC} as close as possible to the device pins.

Figure 6 : Voice Terminal Application Diagram.

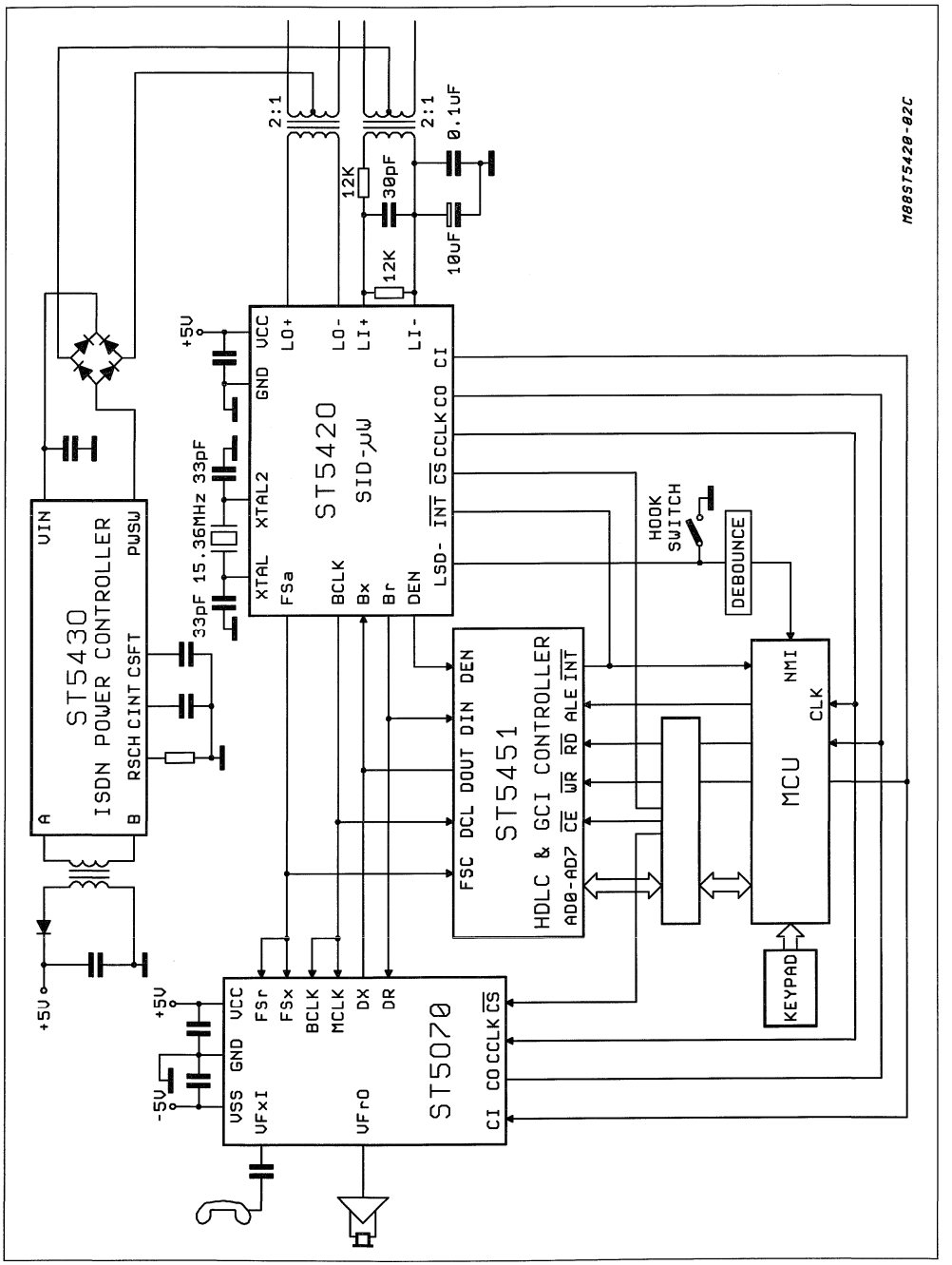
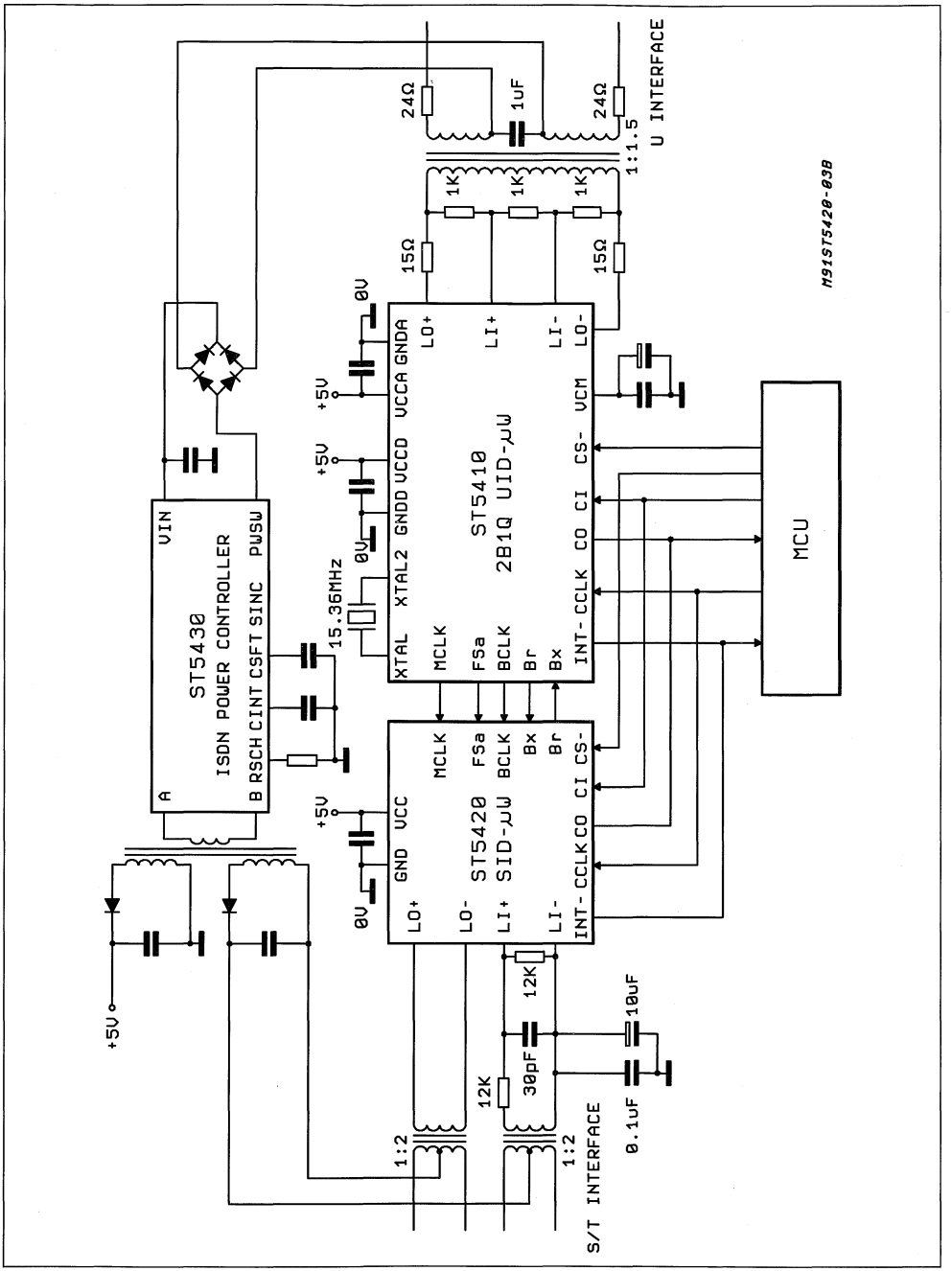


Figure 7 : Network Terminal Application Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
	V_{CC} to GND	7	V
	Voltage at LO, LI	V_{CC} + 1V to GND - 1V	
	Current at LO	±100	mA
	Voltage at any Digital input	V_{CC} + 1V to GND - 1VmA	
	Current at any Digital output	±50	mA
	Storage Temperature Range	-65 to +150	°C
	Lead temperature (soldering, 10 second)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise : V_{CC} = 5V ± 5%, T_A = 0°C to 70°C ; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND).

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2			V
V_{OL}	Output Low Voltage	Br IL =-3.2mA All Other Digital Outputs, IL = 1mA			0.4	V
V_{OH}	Output High Voltage	Br IL = -3.2mA All Other Digital Outputs, IL = +1mA	2.4			V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	-10		10	µA
I_{IH}	Input High Current	Any Digital Input, V_{IH} < V_{IN} < V_{CC}	-10		10	µA
I_{OZ}	Output Current in High Impedance (tri-state)	All Digital Tri-state I/Os	-10		10	µA
LINE INTERFACE						
I_{LI}	Input Leakage	0V > LI+, LI- > 5V	-1		1	µA
R_{LI}	Input Resistance	0V > LI+, LI- > 5V	20			KΩ
V_{LI}	Input Voltage Range		-0.5		V_{CC} +0.5	V
R_{LLO}	Load Resistance	from LO+ to LO-		200		Ω
C_{LLO}	Load Capacitance	from LO+ to LO-			200	pF
V_{OS}	Differential Offset Voltage at LO+, LO-		-20		20	mV
POWER DISSIPATION						
I_{CC0}	Power Down Current	All Outputs Open-Circuit			600	µA
I_{CC1}	Power Up Current	(Note 1)			15	mA

Note 1: when the device is activated and driving a correct terminated line, ICC1 increases by several mA. A worst case data pattarn, consisting of all binary O'S increases ICC1 by approximately 8mA.

ELECTRICAL CHARACTERISTICS (continued)

TRANSMISSION PERFORMANCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Transmit Pulse Amplitude	Conform to all CCITT I430 Requirements Using the Specified Transformer	±1.55		±1.75	
	Input Pulse Amplitude	Differential Between LI+ & LI–	±175			mVpk

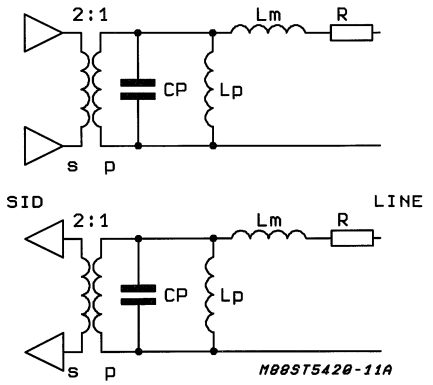
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Input Clock Jitter				50	ns
	Timing Recovery Jitter	BCLK Output Relative to MCLK at NT	– 130		+ 130	ns
t_{MH}, t_{ML}		Clock Pulse Width High and Low of MCLK	20			ns
t_{MR}, t_{MF}		Rise Time and Fall Time of MCLK Used as an Input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10khz)

Symbol	Parameter	Min.	Typ.	Max.	Unit
1 : N	Primary to secondary turn ratio	– 1	2	1	%
R	Primary Total DC Resistance			10	Ohm
Lp	Primary Inductance	20			mH
Lm	Primary Inductance with Secondary Shorted			20	µH
Cp	Primary Capacitance with Secondary Open			25	pF

Figure 8 : Transmit & Receive Transformer Model.



TIMING SPECIFICATIONS (unless specified otherwise : V_{CC} = 5V ± 5%, T_A = 0°C to 70°C ; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND ; see note 5 for timing definition).

SERIAL CONTROL PORT TIMING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{CH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	100			ns
t_{CL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	100			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCSL}	Hold Time, CCLK High to CS Transition		10			ns
t_{SSC}	Setup Time, CS–Transition to CCLK High		50			ns
t_{SIC}	Setup Time, CI Valid to CCLK High		50			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		20			ns
t_{DCO}	Delay Time, CCLK Low to CO Data Valid	Load = 100pF. Plus 1 LSTTL Load			20	ns
t_{DSO}	Dealy Time, CS–Low to CO Data Valid	Bit C7 only			50	ns
t_{DCZ}	Delay Time, CCLK Low to CO High				50	ns
t_{HCSH}	Hold Time, 8th CCLK Low to CS High		100			ns
t_{DCI}	Delay Time, CCLK High to INT- High					ns

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 4

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK High to FSa High	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to Data Valid		20		80	ns
t_{DZC}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HCD}	Hold Time BCLK Low to Data Invalid		20			ns

Note : 5. A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply :
a) All input signals are defined as : V_{IL} = 0.4V, V_{IH} = 2.7V, t_a < 10ns, t_a < 10ns.
b) Delay times are measured from the Input signal Valid to the output signal Valid.
c) Setup times are measured from the Data input Valid to the clock input Invalid.
d) Hold times are measured from the clock signal Valid to the Data Input Invalid.

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 1, 2

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK Transition to FSa Transition	TE Mode only			30	ns
t_{DCD}	Dealy Time BCLK High to Data Valid		20		80	ns
t_{DFD}	Dealy Time FSa High to Data Valid	Load 100pF. Apply only if FSa Rises Later Than BCLK Rising Edge.			80	ns
t_{DCZ}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns

TIMING SPECIFICATIONS (continued)

DIGITAL INTERFACE TIMING : FORMAT 3

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Transition to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH} t_{WCL}	BCLK Width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		30			ns
t_{DCF}	Delay Time BCLK Transition to FSa Transition	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to Data Valid		20		80	ns
t_{DFD}	Delay Tune FSa High to Data Valid	Load 100pF. Apply only if FSa Rises Later Than BCLK Rising Edge.			80	ns
t_{DCZ}	Delay Time BCLK Low to Data Invalid		20		80	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		20			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and NT2 T Side Modes only	0		30	ns

TIMING DIAGRAMS

Figure 9 : Serial Control Interface Timing.

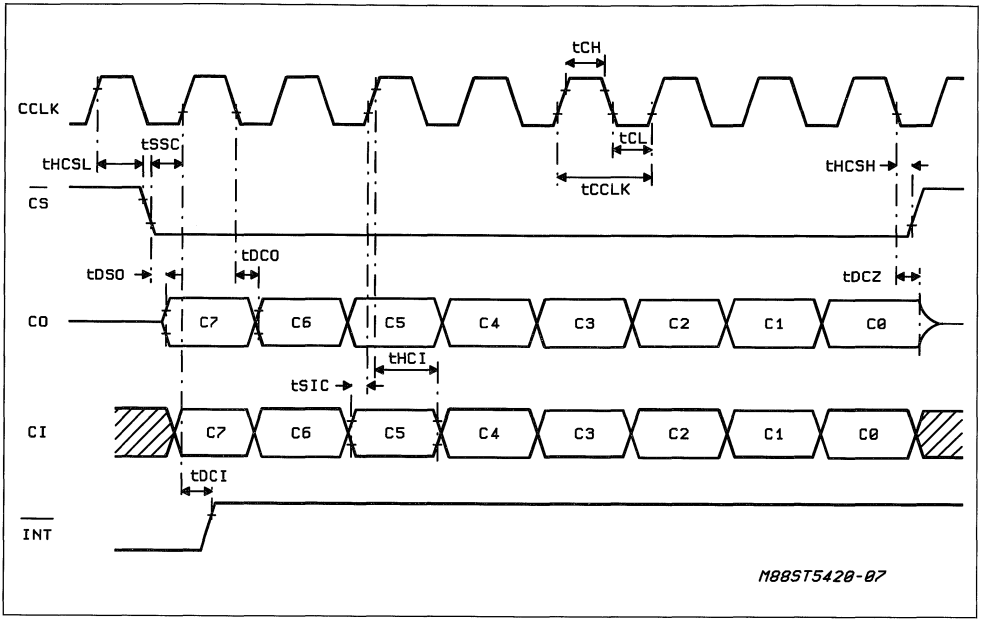


Figure 10 : Digital Interface - Formats 1 & 2 (similar to COMBO I/II non delayed data timing mode).

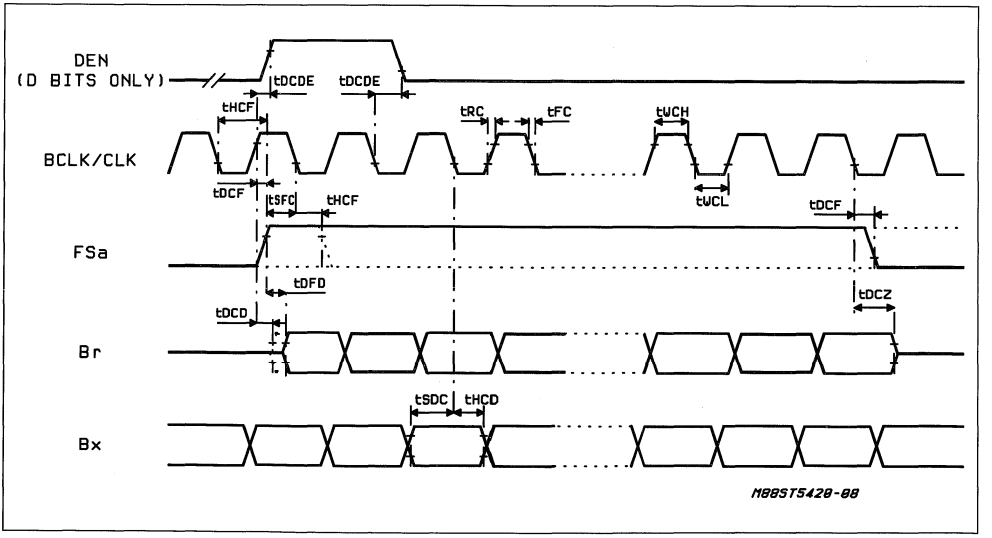


Figure 11 : Digital Interface Timing - Format 3 (GCI compatible).

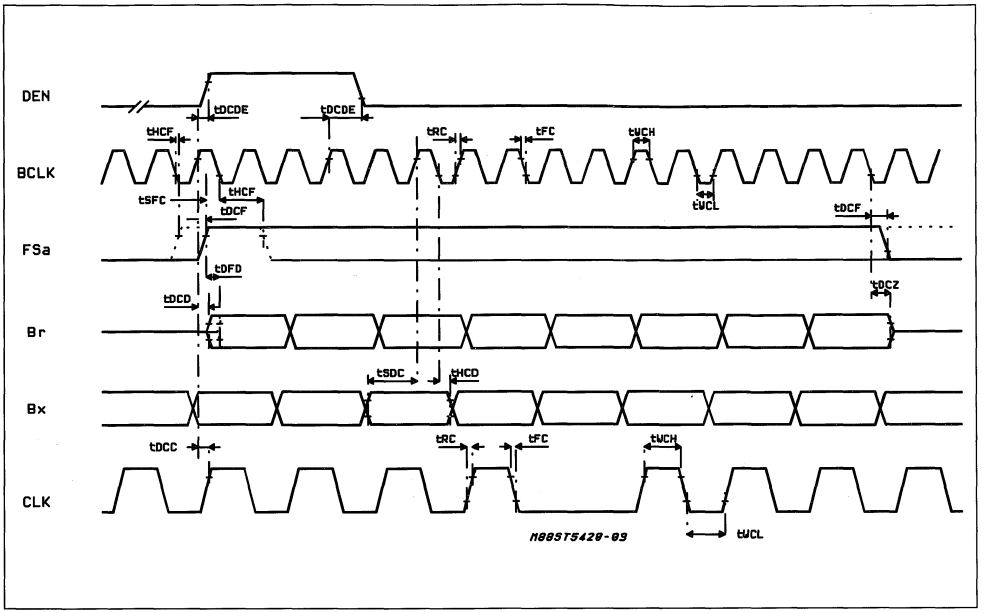
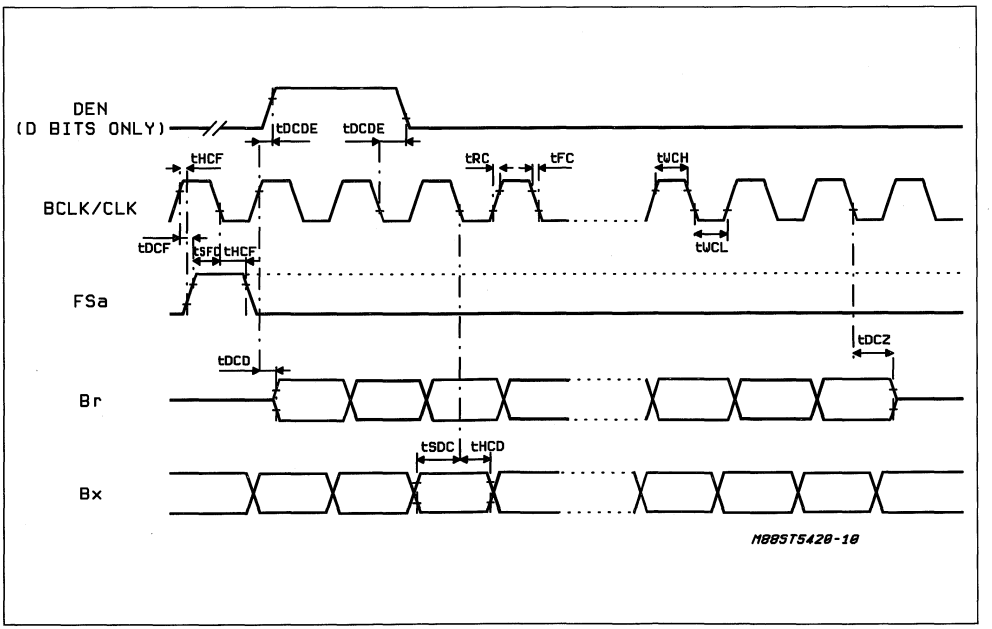


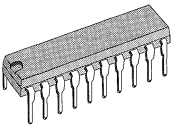
Figure 12 : Digital Interface - Formats 4 (similar to COMBO I/II non delayed data timing mode).



SID-GCI : S/T INTERFACE DEVICE WITH GCI

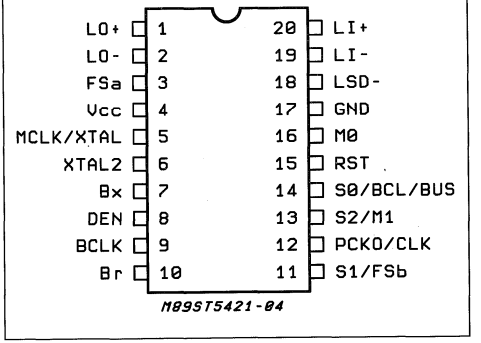
ADVANCE DATA

- SINGLE CHIP 4 WIRES 192kb/s TRANSCEIVER FULLY COMPLYING WITH CCITT I.430
- ISDN BASIC ACCESS HANDLING 144kb/s 2B + D TRANSMISSION
- GCI COMPATIBLE INTERCHIP INTERFACE
- EXCEEDS I.430 RANGE : AT LEAST 1.5KM POINT-TO-POINT AND 200M POINT-TO-MULTIPOINT
- ADAPTIVE AND FIXED TIMING OPTIONS FOR NT
- CLOCK RESYNCHRONIZER AND DATA BUFFERS FOR NT2
- PROGRAMMABLE S1 AND Q CHANNELS HANDLING ACCORDING TO US ANSI STANDARD FOR LAYER 1 MAINTENANCE
- EASILY INTERFACEABLE WITH ST5451 HDLC & GCI CONTROLLER AND ANY OTHER GCI COMPATIBLE DEVICE



DIP20

PIN CONNECTION



DESCRIPTION

The ST5421 (SID-GCI) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on SGS-THOMSON HCMOS 3A double metal advanced process, and requires only a single + 5V supply. All functions specified in CCITT reccommendation I.430 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in TE (Terminal Equipment), in NT1 or NT2 (Network Termination) or in PABX line-card device.

GCI interchip interface highly enhances device connection effiency by multiplexing controls and data on the same bus and requiring only 4 pins. ST5421 implements all the GCI standard functions for Monitor and Control/Indicate channels, supporting up to 8 GCI peripherals in multiplexed mode.

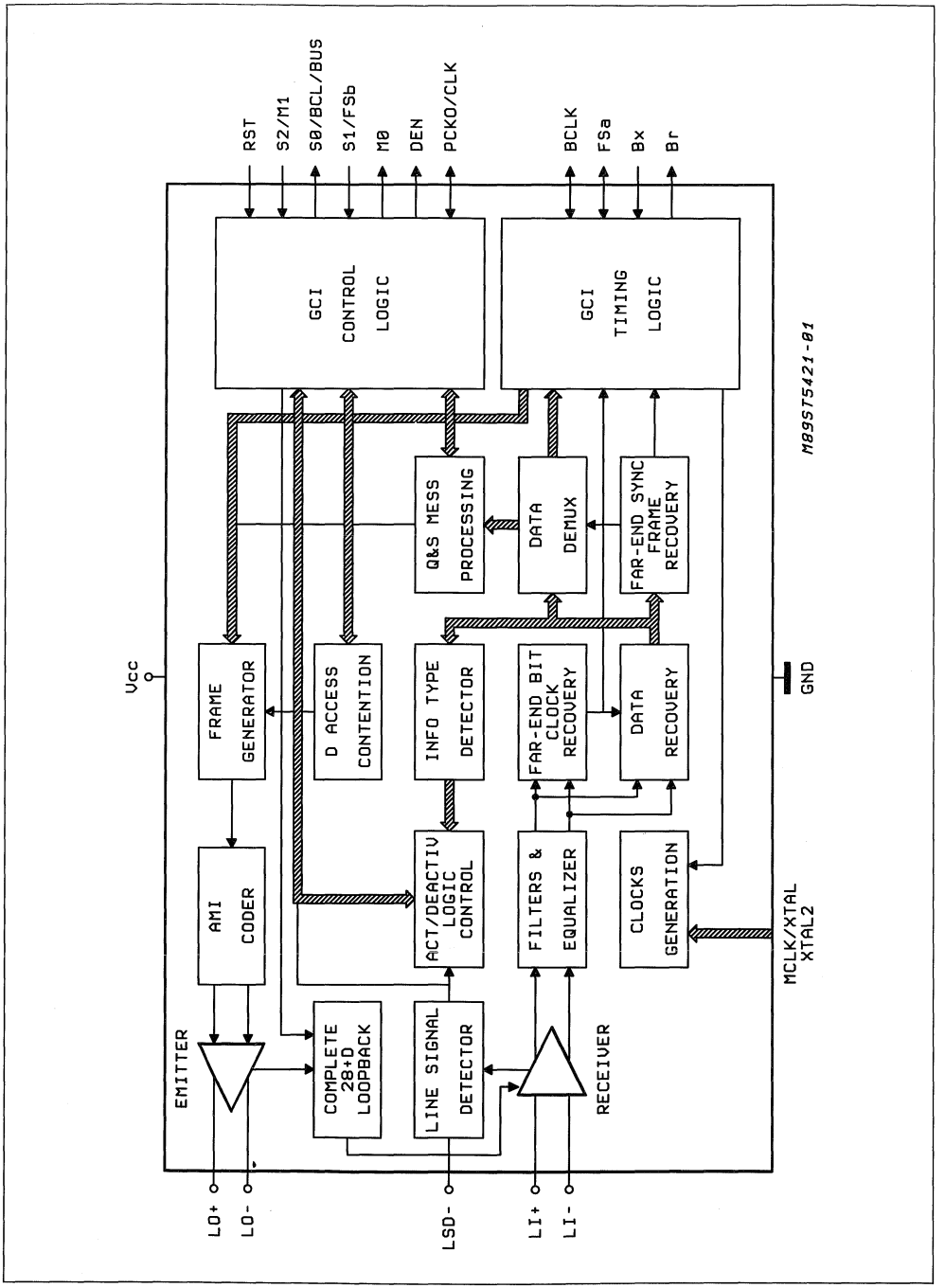
As specified in I.430, full-duplex transmission at 192kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192kb/s aggregate rate, including 2 'B' channels, each of 64kb/s, and 1 'D' channel at 16kb/s. In addition, multiframe transmission is provided in a switchable processing mode based on United State ANSI standard for Layer 1 maintenance. 800 bit/s message oriented data transmission is supported by S1 and Q channels.

All I.430 wiring configurations are supported by ST5421 including passive bus for TE's distributed within 200 meters, and point-to-point and point-to-multipoint extended up to at least 1500 meters (24 AWG cables). Adaptive receive signal processing enables the device to operate with low bit error rate on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

Far-end Clock Resynchronizer automatically selected, data buffer and slave-slave mode allow design of NT2 trunk-card connected to several T interfaces.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



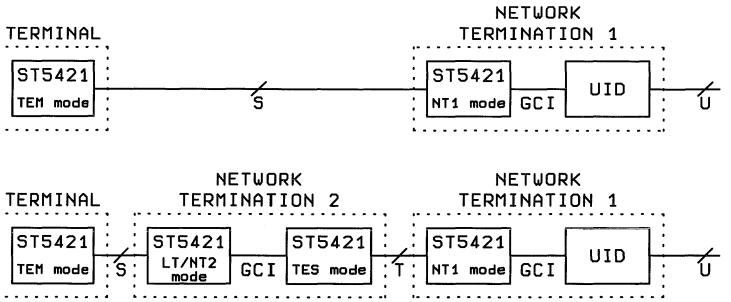
PIN DESCRIPTION

Name	Number	Description
GND	17	Ground Reference Voltage: all analog and digital signals are referenced to this pin.
V_{CC}	4	Positive Power Supply Input 5V (± 5%) relative to GND
MCLK/XTAL	5	Master Clock or Crystal Oscillator Input: this pin requires either a 15.36MHz crystal (parallel resonant with R_S < 100 Ω) to be tied between this pin and XTAL2 or a logic CMOS level 15.36MHz clock from a stable source. When using a crystal, a total of 33pF load capacitance to GND must also be connected. In NT configurations. MCLK clock input doesn't need to be synchronous with the Network Reference Clock (FSa).
XTAL2	6	Crystal Oscillator Output. This pin should be connected to one end of the 15.36MHz crystal, otherwise is not connected.
BCLK	9	Bit Clock: this signal determines the data shift rate at GCI. Data is shifted-in on Bx and shifted-out on Br at half the BCLK frequency. When NT/TES mode is selected. BCLK is an input which does not need to be synchronous with the Master Clock input (MCLK). When TEM is selected, BCLK is an output at frequency of 1536kHz. This clock is phase locked to the receive line signal and synchronous with FSa output.
FSa	3	Frame Synchronization Clock: 8kHz clock which defines the start of the frame on the GCI slave (NT/TES) Fsa is an input used as a network reference clock for S/T line. In GCI master (TEM) is an output applicable as a validation strobe for the first B channel.
S1/FSb	11	S1 if M0 = 1; is GCI channel number selection. FSb if M0 = 0 and M1 = 0 (TEM): is a data strobe indicating the active slot for the second B channel on the GCI.
Bx	7	Digital Input for GCI Channels: data to be transmitted to S line is shifted-in at half the BCLK frequency on the 2nd falling edge.
Br	10	Digital Output for GCI Channel (OPENDRAIN): data is shifted-out at half the BCLK frequency on the transmit rising edges of BCLK. An external pull-up resistor is needed.
DEN	8	DEN in TEM mode: is an output, normally low, that pulses high to indicate the active time slot for D channel data at the Bx input. It is intended to be gated with BCLK to control the D channel shifting from a layer 2 device (i.e. ST5451) to ST5421 transmit buffer. Using ST5451 HDCL/GCI controller, no external circuitry is needed.

PIN DESCRIPTION (continued)

Name	Number	Description
PCK0/CLK	12	PCK0 IN TEM, LT/NT2, NT1 mode: 32 kHz clock output synchronized to GCI clocks. It is intended to synchronize DC/DC converter in TEM mode. CLK in TES mode: is a clock signal open drain output phased-locked to the receive S line signal and applicable as far-end clock reference. Its frequency is 1536kHz compatible with 768kbit/s GCI data rate. An external pull-up resistor is needed.
M0	16	M0 = 0: GCI mode selection; Time slot Assigner is selected on GCI channel 0. M0 = 1: GCI in a multiplex mode; S0, S1, S2 pins define the GCI channel number allocated to ST5421. TES/NT2 selection is done with the configuration registers.
S2/M1	13	S2 if M0 = 1: GCI channel number selection. If M0 = 0; M1 = 0: TEM selected, M1 = 1: NT1 selected.
S0/BCL/BUS	14	S0 if M0 = 1; GCI channel number selection. BCL in TEM; bit clock output at 768kHz compatible with COMBO families ETC5054/57. BUS in NT1; S Bus Configuration Selection: low for fixed timing recovery and high for adaptive timing recovery.
RST	15	Reset Pin: must be low at Power On Reset; after, a high pulse on this pin reset ST5421 in a state depending on the other configuration pins.
LSD-	18	Line Signal Detect: open drain output, normally high impedance, pulling low when SID-GCI is powered down and an S line signal is detected. It is applicable to wake up a microprocessor from a low power idle mode. $\overline{LSD}$ output goes back to high impedance when ST5421 is powered up.
LO+, LO-	1,2	Transmit AMI signal differential outputs to the S/T line transformer; when used with an appropriate 2:1 step down transformer, the line signal conforms to the output pulse masks in CCITT I.430.
$\overline{LI}$,LI$^+$	19,20	Receive AMI signal inputs from the S/T line transformer. They should be connected to an appropriate 1:2 or 1:1 transformer through a line coupling circuit to conform I.430 recommendation. $\overline{LI}$ pin is also the internal voltage reference pin.

Table 1: Pin configurations



	TEM	LT/NT2(1)	TES (1)	NT1
M0	i=0	i=1	i=1	i=0
DEN	o=DEN			
S2/M1	i=M1=0	i=S2	i=S2	i=M1=1
S1/FSb	o=FSb	i=S1	i=S1	Not used
S0/BCL/BUS	o=BCL	i=S0	i=S0	i=BUS
PCK0/CLK	o=PCK0	o=PCK0	o=CLK	o=PCK0

MB9ST5421-06

(1) differentiation between TES and LT/NT2 is done by register programming.
Default value after reset is LT/NT2 in adaptive timing recovery configuration.

FUNCTIONAL DESCRIPTION

POWER OF INITIALIZATION

Following initial application of power, SID-GCI enters the power down de-activated state.
RST input must be tied low during power-on.

After Power on reset, all the internal I.430 circuits including the master oscillator are inactive and in a low power state except for the line signal detection circuit.

After any period of activity a high pulse on RST reset completely SID-GCI.

Configuration mode programming of SID-GCI is done by means of pins polarization and register programming.

NT1 and TEM modes are defined only by means of 2 configuration pins M0, M1 at Power On Reset.

For NT2 and TES modes (M0=1), configuration has to be completed by means of a Control Instruction on Monitor channel prior a Power Up instruction.

POWER UP/DOWN CONTROL

When TEM configuration is selected, ST5421 provides GCI Clocks needed for control channel transfer. Power Up instruction is directly provided by pulling low the Bx data input. SID-GCI then reacts sending GCI clocks. LSD- output pin can be directly connected to Bx data input for providing an automatic Power up when far-end attempts to activate.
After a period of activity, Power down state is normally re-entered by C/I control code DC (1111) while ST5421 is sending C/I indication code DP (0000); then ST5421 send twice C/I indication code DI(1111) before to power down.
It is possible to force immediately power down state by using PDN (0001) C/I control code.

When NT1 configuration is selected, ST5421 is powered up directly by receiving GCI clocks on BCLK and FSa input from the "U" device. The only way to power down ST5421 is to stop BCLK or FSa clock signal inputs.
For example PDN (0001) C/I control code has no effect.

When NT2 or TES configuration is selected, SID-GCI is powered up by the PUP code (0000) on C/I Control Channel. After a period of activity, Power down state is normally reentred by C/I control code DC (1111) while ST5421 is sending C/I indication DI(1111).
It is possible to force immediately Power down state by using PDN (0001) C/I control code. In NT1, NT2 or TES mode, loss of GCI clocks automatically forces the power down state.

POWER UP/DOWN STATE

Following a period of activity in the power up state, power down state may be re-entered as described above. Configuration Registers remain in their current state. They can be changed by the GCI Monitor channel.

The power down transition disables analog and I.430 circuitry, stops the Crystal Oscillator and all the clocks internally generated. Line Signal Detector Circuit remains active allowing LSD-pin to pull low if a receive signal is detected.

Power up transition enables all analog and I.430 circuitry, starts the Crystal oscillator and reset the state machine to the de-activated state. It also inhibits LSD-output.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate Mark Inversion (AMI) coding with inverted binary is used, as illustrated in figure 1.

This coding rule requires that a binary ONE is represented by a 0 current high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c. balanced line signal.

The frame format used in SID-GCI follows CCITT reccommendation in I.430 and illustrated in figure 2. Each complete frame consists of 48 bits, with a line bit rate of 192kbit/s, giving a frame repetition rate of 4kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a 0+ bit followed by a 0- balance bit to indicate the start of a frame, and by forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to Terminal Equipment (TE) transmission direction, the frame contains in addition to the 2B+D basic access data, an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE (s), and three extra channels: FA, M and S bit.

In the TE to NT direction, the frame contains in addition to the 2B + D data, an extra channel, the FA bit.

FA, M and S bits are used to set up a Q multiframe channel in the TE or NT direction, and a S1 multiframe channel from NT to TE. These 800bit/s message oriented channels are structured on the base of the United States ANSI standard specification for layer 1 maintenance.

Figure 1: Inverted AMI Line-coding Rule.

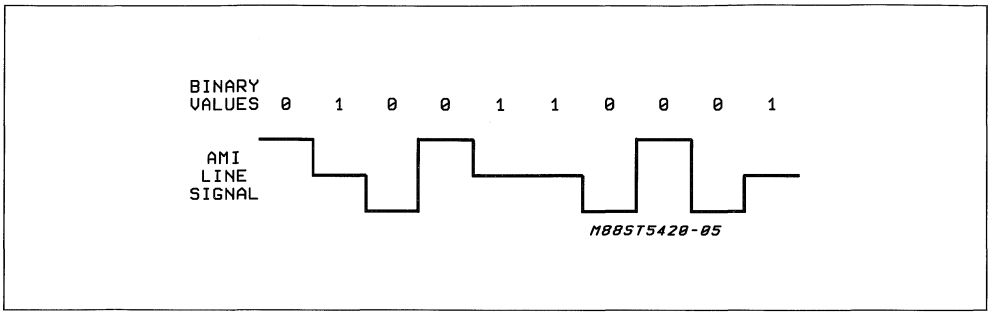
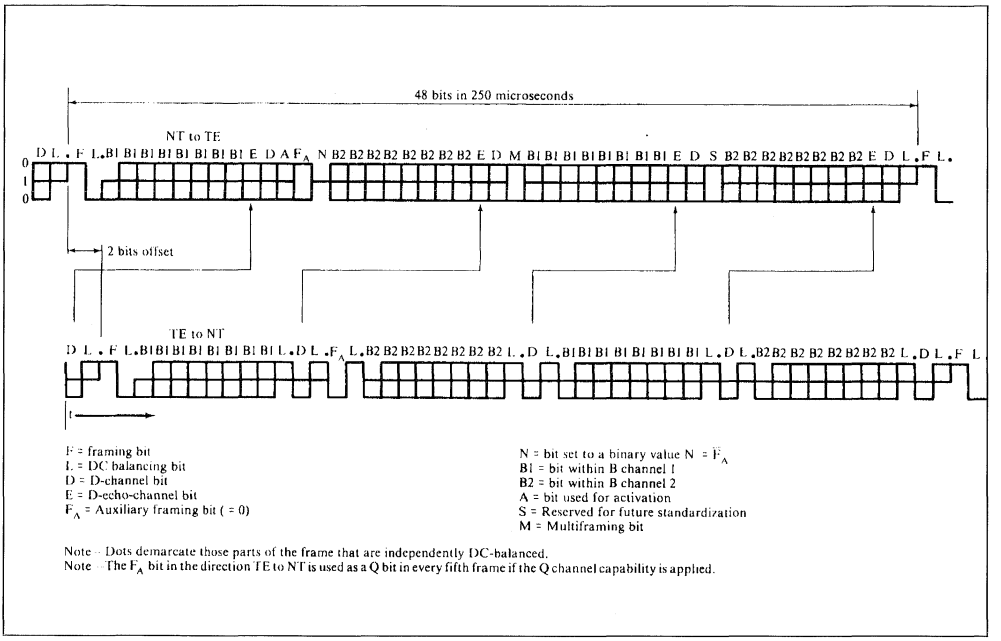


Figure 2: Frame Format



LINE TRANSMIT SECTION

The differential line driver outputs LO+ and LO- are designed to drive a suitable transformer with an external termination resistor. A 2:1 transformer, results in a signal amplitude of 750mV on the line which meets the I.430 pulse shape for all the loads specified.

When driving a binary 1 symbol, the output presents a high impedance in accordance with I.430. When driving a 0+ or 0- symbol, the voltage limited current source is turned on.

Short protection is included in the output stage.

Overvoltage protection is required externally.

Depending on TE or NT selected configuration, 192kbit/s data is transmitted on LO+,LO- by means of clocks respectively locked on the far-end received bit and frame clocks recovered from the line with two bit delay between transmit and receive frame, or locked with a fixed delay on the Frame Sync signal received from FSa input.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 a or 1:2 transformer of the same type used for

the transmit direction.At the front end of the receive section is a continuous filter which limits the noise bandwith. To improve the protection of the line interface and to comply with the receive input impedance spec even if power is lost, it is necessary to add 3 external resistors between the receive transformer and the LI+/LI- pins.

To correct pulse attenuation and distorsion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics.

This equalizer is always enabled when either TE or NT mode adaptive sampling is selected, but is disabled for NT short passive bus applications, when NT mode fixed sampling is selected.

An adaptive threshold circuit maximizes Signal to Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.

The MCLK input provides the reference clock for the DPLL at 15.36MHz.

When the device is powered down, a Line Signal Detect circuit, able to discriminate a valid line signal from noise, is enabled to detect the presence of incoming data. LSD-output pulls low to wake up the equipment.

GCI INTERFACE

General Description

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...

In Terminal Equipments, this interface allows connection between SID-GCI and an associated ST5451 HDLC&GCI Controller used for 16kbit/s D channel processing and SID-GCI control. 64kbit/s B1 and B2 channels are transferred on GCI interface providing direct connection for B channel processing peripherals like Programmable ISDN COMBO ST5080 or extra ST5451 controllers.

In NT2 or PBX line card, GCI interface permits connection of up to 8 SID-GCI onto a common serial multiplexed bus. Each SID-GCI is assigned to one GCI channel selected by hardware configuration.

Figure 3 shows the Frame structure of a GCI channel. One GCI channel is structured in four subchannels:

- B1 channel 8 bits
- B2 channel 8 bits
- Monitor (M) channel 8 bits
- SC channel which is structured as follows:
  - D channel 2 bits
  - C/I channel 4 bits
  - A bit associated with M channel
  - E bit associated with M channel

B1,B2 and D channels are used to transfer 2B + D basic access data.

M channel is used to read and write multiframe S1 and Q channel messagès and to configurate SID-GCI. Protocol for byte exchange on the M channel uses the E and A bits.

C/I (Control/Indicate) channel is used to exchange "real time" primitives between the SID-GCI and the Controller as Activation/Deactivation codes.

Physical Description

The interface consists of 4 wires:

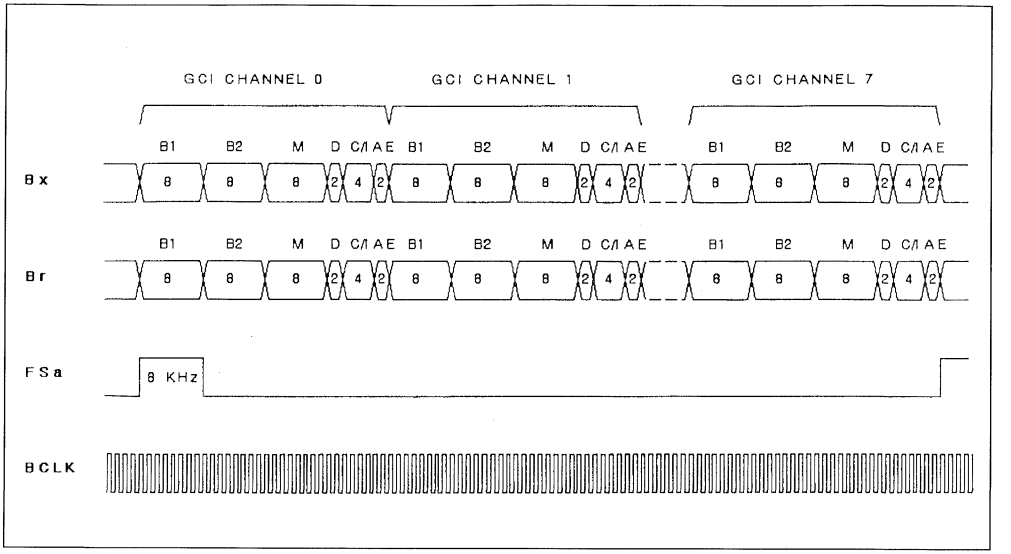
- Input Data: Bx
- Output Data: Br
- Bit Clock: BCLK
- Frame Synchronization: FSa

Data is synchronized by BCLK and FSa signals. The latter insures reinitialization of a time slot counter at each frame beginning. Its rising edge is the reference for the first bit of the first GCI channel. Data is transmitted in both directions at half the BCLK frequency, on the rising edge of BCLK and is sampled 1.5 period after the transmit rising edge. Unused channels are high impedance.

In NT2 or PABX equipments, up to 8 GCI channels (32 bits each) may be multiplexed on Bx and Br links used as a serial bus for several devices. The channel number selection is made by programming pins S0,S1 and S2 according to the following rules:

S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0 -3
0	0	1	1	4 - 7
0	1	0	2	8 - 11
0	1	1	3	12 - 15
1	0	0	4	16 - 19
1	0	1	5	20 - 23
1	1	0	6	24 - 27
1	1	1	7	28 - 31

Figure 3: GCI Interface Structure



BCLK frequency may be any value between 512 and 6176kHz.

In TEM and NT1 configurations, the first GCI channels is automatically selected.

In TEM configuration, due to SID-GCI recovery circuitry, a low jitter should be provided on FSa and BCLK clocks. FSa and BCLK are always in phase. The maximum value of jitter amplitude is a step of 65ns at each GCI frame (125µs). The maximum high frequency jitter amplitude is 130ns pk-pk.

For applications such as the network side of an NT2, eg, a PABX trunk card, TES mode allows the transmission side of SID-GCI to be a slave to the received frame timing while GCI is also in slave mode Elastic buffers which allow any phase relationship between FSa and I.430 frames and a clock resynchroniser circuit absorb jitter and low frequency wander up to at least 18µs pk-pk at frequencies below 10Hz.

Exchange Protocol on the C/I channel

Exchange of information in the C/I channel runs as follows:

Two devices connected on a GCI channel send each other a permanent four bit command code in the C/I field. The same code is sent at a 8kHz frequency as long as the content of the internal C/I register remains unchanged.

When a change of C/I the command is initiated that is recognized by SID-GCI if detected in two consecutive frames.

ST5421 will interpret the new code and send the corresponding control instructions on the S line or switch a local function as long as the corresponding action is required.

An information change received from the S line or a local status change of SID-GCI set a new indication code on the C/I channel. The code is sent at least in 2 consecutive frames.

Table 2 gives the C/I codes meaning. C1 bit is first transmitted.

Here after for each mode a list of recognized Control and Indicate codes is given.

TEM mode: Control

0000 (DR) : Deactivation Request
In the Power Up state, DR instruction can be used as a Deactivation Request instruction to force transmission of INFO0 on the S line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state after that DI (1111) has been sent in two consecutive frames.

1000 (AR8) : Activate Request Class 8.
AR8 instruction combines an Activation Request, which initiates the Activation Sequence on the line, and a request to attempt to access the transmit D channel in the high priority class at the S interface after its complete activation. After activation of the S interface, AI8 indication is sent by ST5421. D channel access attempt is

Table 2: C/I Channel Coding

Code	TEM		LT/NT2		TES		NT1	
C1 C2 C3 C4	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DP	DR	TIM	PUP/DR	DP	PUP/DR	TIM	DR
0001	X	PDN	X	PDN	X	PDN	X	X
0010	X	X	X	X	X	X	X	X
0011	EOM	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	X	EI	FI2
0101	X	X	X	X	X	X	X	X
0110	X	X	X	X	X	X	X	X
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	FI4	AI	X	AI	FI4
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DC	DI	DC	DI	DC	DI	DC

(x) codes reserved

automatically processed for each HDLC frame to be transmitted without need for new Control Instruction.
Except for code EOM, any further indication change on C/I as CON or EI deactivates D channel access attempt at the S interface. A new AR8 instruction is needed to restart the procedure.
Note : A new AR8 instruction means that if the controller was already sending AR8, it has to change first the code sent to ie DC (1111) and after change again to AR8.

1001 (AR10) : Activate Request Class 10.
Same meaning as AR8 command but requesting access to transmit D channel with low priority class.
After activation of the S interface has been completed, AI10 indication is sent by SID-GCI.

1010 (ARL) : Activate Request Loopback.
ARL instruction operates a loopback of 2B + D channels from Bx input to Br output. It may be set when the device is either activated, in which case it is transparent (the composite signal is also transmitted to the line), or when it is deactivated in which case it is non transparent.
Any change from ARL to another C/I command clears the loopback.
When the complete loopback is activated, (AIL) code is sent by SID-GCI.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DP sent by SID-GCI). When S line is not deactivated, DC has no effect.

TEM mode : Indication

0000 (DP) : Deactivation Pending Indication.
DP code indicates ST5421 is powered up and that no identified signal has been detected on the S line. DP indication is sent when one of the following events occur :
- Power Up has been completed and no signal is identified on the line,
- after a period of activity, INFO0 is detected on the S line,
- the device being in status F4, F5, F6, F7 or, F8, a DR instruction is issued.

0011 (EOM) : End of Message.
EOM indicates that the closing flag of a D channel message has been transmitted on S line indicating successfull completion of a packet sending. EOM is sent continuously until receiving of a new AR8 or AR10 command or line status change.
EOM code sending can be disabled via a Monitor channel instruction EID : (see table 3).

0100 (EI) : Error Indication.
EI indicates that a frame loss of has been detected on S line ; is sent when one of the following events occur :
- being in the F6 or F7 states, detection of a loss of frame, (jump to F8).

- being in the F7 state, receiving of INFO2, (jump to F6).

1000 (AP) : Activation Pending.
AP indicates that INFO2 (or INFO4) frames have been identified on the line.
AP indication is sent when one of the following events occur:
- being in F2 deactivated state, detection of INFO2 or INFO4.
- being in the loss framing state F8, detection of INFO2

1001 (CON) : Contention Indication
CON is sent when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.
D channel access attempt is deactivated at the S interface. A new AR8 or AR10 instruction is needed to restart the procedure.

1100 (AI8) : Activation Indication Class 8.
AI8 is sent when, following an AR8 instruction, the S line is completely activated (state F7). The D channel access procedure is set in the high priority class 8 (or 9).

1101 (AI10) : Activation Indication Class 10.
AI10 is sent when, following an AR10 instruction, the S line is completely activated. The D channel access procedure is set in the low priority class 10 (or 11).

1110 (AIL) : Activation Indication Loopback.
AIL indicates that the complete loopback requested by the instruction ARL is completed.

1111 (DI) : Deactivation Indication.
DI is sent at least in two consecutive frames when, being in the S line deactivated state (DP indication sent by SID-GCI) DC control instruction is received on C/I control channel.
After that, SID-GCI is automatically powered down.

TES mode : Control.

0000 (PUP/DR) : Power Up Request/Deactivation Request.
When in Power Down, Power Up instruction powers up the device in the configuration previously set. When in Power Up, PUP/DR can be used as a Deactivation Request instruction to force the transmission of INFO0 on the line.

0001 (PDN) : Power Down Request.
PDN instruction forces the device to the Power Down state.

1000 (AR) : Activate Request.
AR instruction initiates the Activation Sequence on the line. It is recommended that an AR be delayed at least 2ms after the PUP instruction.

1010 (ARL) : Activate Request Loopback.
Identical to TEM mode.

1111 (DC) : Deactivation Control.
DC instruction allows ST5421 to enter automatically the Power Down state if the S line is deactivated (DI sent by SID-GCI). When S line is not deactivated, DC has no effect.

TES mode : Indication.

0000 (DP) : Deactivation Pending.
DP code indicates ST5421 has been just powered up and no signal has been identified on the line.

0100 (EI) : Error Indication.
Identical to TEM mode.

1000 (AP) : Activation Pending.
Identical to TEM mode.

1100 (AI) : Activation Indication.
AI is sent when, following an AR instruction, the S line is completely activated in state F7.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation indication.
DI indication is sent when one of the following events occur:
- After a period of activity, INFO0 is detected on the S line,
- the device beeing in status F4, F5, F6, F7 or F8, DR instructions is issued.

NT1 mode : Control.

0000 (DR) : Deactivation Request.
DR command forces ST5421 through the appropriate deactivation sequence where INFO0 is sent on the line. The device remains in the Power Up state. DI indication is sent.

0100 (FI2) : Force Info 2
Being in the activated state G3, FI2 instruction forces the appropriate sequence to send INFO2 on the line. If the S line is not completely activated, FI2 instruction has no effect.

1000 (AR) : Activation Request.
Being in the inactive Power Up state, sending INFO0, AR instruction forces SID-GCI through the appropriate sequence to send INFO2 on the line. It is recommended that an AR instruction be delayed at least 2ms after setting the GCI clocks.

1010 (ARL): Activate Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An activation Request being in progress, FI4 instruction allows SID-GCI through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
DC instruction has no effect on SID-GCI.

NT1 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, the LSD- output is pulled low to indicate that the far-end is attempting to activate the S interface. The device requests GCI clock signals. Receiving of GCI clocks powers up the SID-GCI, LSD- is freed, and TIM code is sent on the C/I channel.

0100 (EI) : Error Indication.
EI code indicates that a loss of frame has been detected on the S line, ST5421 being previously activated.

1000 (AP) : Activation Pending.
AP code indicates that INFO1 frames have been identified of the line. The device is waiting for an activate request to send INFO2.

1100 (AI) : Activation Indication.
AI code indicates that the S line is activated. That means it is receiving INFO3.

1111 (DI) : Deactivation Indication.
DI code indicates S line is completely deactivated: the device can be powered down switching off GCI clocks.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

NT2 mode : Control.

0000 (PUP/DR) Power Up Request/Deactivation Request.
When in Power Down state, PUP code powers up the device in the NT2 configuration previously selected. When in Power Up state DR code forces the appropriate deactivation sequence where INFO0 is sent on the line. SID-GCI remains in Power Up state.

0001 (PDN) : Power Down Request.
Identical to TES mode.

1000 (AR) : Activation Request.
After a PUP instruction, AR forces the appropriate sequence to send INFO2 on the line. It is recommended that AR instruction is sent after receiving TIM indication..

1010 (ARL) : Activation Request Loopback.
Identical to TEM mode.

1100 (FI4) : Force Info 4.
An Activation Request being in progress, FI4 instruction puts ST5421 through the appropriate sequence to send INFO4 on the line.

1111 (DC) : Deactivation Control.
The DC instruction allows to enter the power down state if the S line is deactivated.
DC control has no effect if SID-GCI not sending DI indication.

NT2 mode : Indication.

0000 (TIM) : Timing Requested.
Being in Power down state, LSD- output is pulled low to indicate that far-end is attempting to activate the interface. SID-GCI requests GCI clocks followed by a PUP instruction. After receiving, LSD- is freed and TIM is sent on C/I channel.

0100 (EI) : Error Indication.
Identical to NT1 mode.

1000 (AP) : Activation Pending.
Identical to NT1 mode.

1101 (AI) : Activation Indication.
Identical to NT1 mode.

1110 (AIL) : Activation Indication Loopback.
Identical to TEM mode.

1111 (DI) : Deactivation Indication.
The DI code indicates that the S line is completely deactivated.

EXCHANGE PROTOCOL ON M CHANNEL

Protocol allows a bidirectional transfer of bytes between SID-GCI and a Controller (for example ST5451) with an acknowledgement at each received byte.

Write cycle.
The Controller sends to ST5421 control instruction(s) coded on a single byte. It is possible but optional to write several control instructions in a single message. Control instruction bytes are structured as defined in Table 3.

Read cycle.
When a new validated S1 or Q message is received from the line, the device send a single byte message as defined in table 4. If a new message is received from the S line before the previous is acknowledged by the controller end, this new message is lost.

Exchange protocol.

The exchange protocol is identical for both directions.

The sender uses E bit to indicate that it is sending a M byte while the receiver uses A bit to acknowledge the received byte.

When no message is transferred, E bit and A bit are forced to inactive state (i.e. high impedance).

A transmission is initialized by the sender setting E bit in active state and sending the first byte on M channel in the same frame. Transmission of a message is allowed only if A bit received has been detected inactive in the last two frames.

When the receiver is ready, it validates the received byte internally when it has been detected identical in two consecutive frames. Then, the receiver set first A bit from inactive to active state; it is the pre-acknowledgement, and maintain A bit active at least in the following frame, it is the acknowledgement.
If validation is not possible, the two last bytes received not identical, the receiver abort the message by setting A bit active for one frame only.

A second M byte may be transmitted by the sender turning E bit from active to inactive state and sending the byte in the same frame. The E bit is set inactive for one frame only. If it remains inactive more than one frame, it is an end of message. The second byte may be transmitted only after receiving the pre-acknowledgement of the previous byte (see timing diagram).

The receiver validates the current received byte as for the first one and then set A bit in the next two frames first from active to inactive state (pre-acknowledgement) and from inactive to active (acknowledgement). If the receiver cannot validate (the two bytes received are not identical) it pre-acknowledges normally but let A bit in the inactive state in the next frame which indicates an abort request.

If a message is aborted, ST5421 sends again the complete message until receiving acknowledgement.
A received message is acknowledged or aborted without flow Control.
Figure 4 gives the timing of a write cycle. The most significant bit of a Monitor byte is sent first of the M channel. E & A bits are active low and inactive state on Br is high impedance.

Figure 4: Monitor messaging

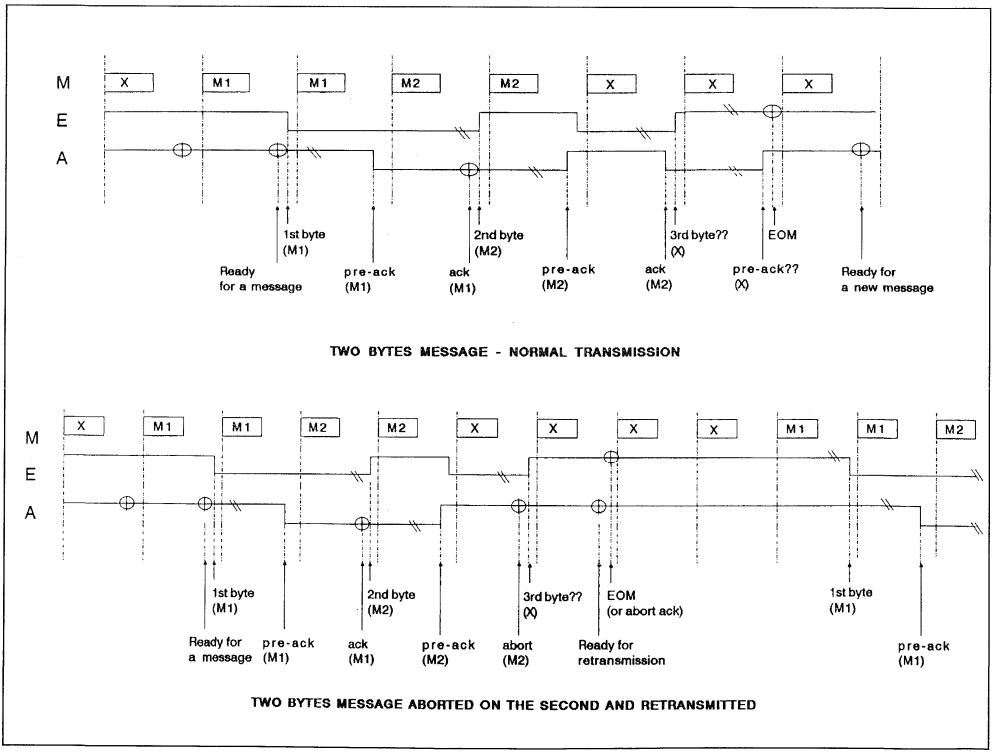


Table 3: Monitor Channel Instruction

Functions	Mnemonic	Bit Number 7	6	5	4	3	2	1	0
Device Mode:									
NT Mode Adaptive Sampling (*)	NTA	0	0	0	0	0	1	0	0
NT Mode Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode (slave-slave)	TES	0	0	0	0	0	1	1	0
Monitoring Mode Activation	MMA	0	0	0	1	1	1	1	1
TE Master Mode	TEM	0	0	0	0	0	1	1	1
B Channel Configuration:									
B Channel Mapped Direct (*)	BDIR	0	0	0	0	1	1	0	0
B Channel Exchanged	BEX	0	0	0	0	1	1	0	1
B1 Channel Enabled (*)	B1E	0	0	0	1	0	1	0	0
B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enabled (*)	B2E	0	0	0	1	0	1	1	0
B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
End of Messages Indication:									
EOM Indication Enabled (*)	EIE	0	0	0	1	0	0	0	1
EOM Indication Disabled	EID	0	0	0	1	0	0	0	0
Multiframe Processing:									
Multiframe Disabled (*)	MID	0	0	0	1	0	0	1	1
Multiframe Enabled	MIE	0	0	0	1	0	0	1	0
Disable Three Time Checking	DIS3X	0	0	1	0	1	0	0	1
Enable Three Time Checking (*)	EN3X	0	0	1	0	1	0	0	0
Write Multiframe Message	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Mode:									
Clear All loopbacks (*)	CAL	0	0	0	1	1	0	1	1
Loopback B1 on Line Enabled	LB1E	0	0	0	1	1	0	0	0
Loopback B2 on Line Enabled	LB2E	0	0	0	1	1	0	0	1
Loopback 2B+D Enabled (1)	LBS	0	0	0	1	1	0	1	0
Loopback B1 on GCI Enabled	LBB1E	0	0	0	1	1	1	0	0
Loopback B2 on GCI Enabled	LBB2E	0	0	0	1	1	1	0	1

(1) alternate command instruction to ARL (C/I code); but without any status indication pending.
(*) initial state following Power on initialization

Table 4: Monitor Status Messages

Functions	Mnemonic	Bit Number 7	6	5	4	3	2	1	0
Multiframe Receive Register	MFR	0	0	1	1	M1	M2	M3	M4

Monitor channel code description:
Monitor channel code list is given in table 3 and 4.

Device mode.

NTA : NT mode Adaptive sampling.
In NT mode, adaptive sampling should be selected when the device is an NT equipment connected on any wiring configuration up to the maximum specified length for operation. Multiple Terminals, if required, must be grouped within approximately 50 meters one from each other (depending on cable capacitance as indicated in I.430). Transmit section of SID-GCI is phased locked to GCI FSa source.

NTF : NT mode fixed sampling.
In NT mode, fixed sampling should be selected when the device is in a NT equipment connected on a passive bus wiring configuration up to approximately 200 meters in length depending on cable type. In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed to enable multiple Terminals (nominally up to 8) to be connected anywhere along the passive bus. Transmit and Receive section is phased locked to GCI FSa source.

TES : TE mode connected on the T interface.
This mode should be selected when the device is used on the T interface side of an NT2 equipment. I.430 circuitry operates as in TE mode but GCI interface is driven by BCLK and FSa sources providing a slave-slave configuration.

Data buffers and a clock resynchronizer enable

the GCI to function with FSa and BCLK jittering sources. No phase relationship is needed between the line recovered clocks and GCI.

A 1536kHz clock signal output phased locked to the Recevied line signal is delivered on CLK.

CLK output signal is generated only when ST5421 if fully activated (state F7) and no clock signal is detected on that pin by the device during his own selected GCI channel.
Otherwise CLK output remains high impedance.

Note: CLK output is activated immediately on the first bit of the B2 channel (GCI side) and is deactivated immediately if SID-GCI leaves F7 state.

D channel access Control circuitry is disabled. i.e. D channel data at Bx input is continuously transmitted to the line; there is no monitoring of the D echo channel from the network direction.

MMA : Monitoring mode activation.
When ST5421 is configured in TE mode by means of pins M0, M1, the MMA instruction allows to receive and activate on INFO3 frames, while remaining the master of GCI. That configuration can be used for applications such as monitoring the outputs of TEs on a passive bus.
The received 2B+D can then be passively monitored (the line transmit LO+,LO- would not be connected).

TEM : TE Master Mode.
When ST5421 is in TE configuration by means of pins M0, M1, and in the Monitoring Mode Activation by means of the instruction MMA, the TEM instruction set back SID-GCI in the normal TE Master mode.

B channels configuration.

BDIR/BEX B1E/B1D B2E/B2D
BDIR and BEX instructions provide for the exchange of data between the B1 and B2 channels. (Note: when enabling a B channel in conjuction with the BEX command, channels is referenced at the CGI).
When either or both B channels are disabled by means of the B1D or B2D instruction, binary 1 are transmitted on the line regardless of Bx input while Br output is in high impedance state. When enabled by means of B1E and B2E instructions, B channel are transparently transmitted.

End of message indication.

EID/EIE
C/I channel End Of Message code sending can be enabled with instruction EIE and disabled by means of EID.

Multiframe processing.

MFT/MFR/MIE/MID
In the Transmit direction, with the device in TEM or TES mode, data entered in bit positions M1, M2, M3 and M4 of instruction MFT is transmitted to the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT mode, data entered in the M bit positions is transmitted to the TE in multiframe bit positions S11, S12, S13 and S14 respectively. In the Receive direction, when the Multiframe receive data buffer requires servicing, the MFR (see table 4) status message is autonomously sent with M1, M2, M3 and M4 bits representing Q1, Q2, Q3 and Q4 or S11, S12, S13 and S14 bits received from the multiframe respectively.

Multiframe Structure and transmission protocol on the line comply with the ANSI US Standard T1.605.1989. "Basic Access Interface for S and T Reference points - Layer 1 specification".

Multiframe message exchange can be supported by SID-GCI when the line is synchronized : states F6 & F7 in TEM or TES modes and state G3 in NT modes.

The multiframe channel processing must be enabled by an MIE instruction to use these channels.

DIS3X/EN3X

When EN3X is set, a new Multiframe message received from the line is checked and transferred on the M channel when received three times identical.
When DIS3X is set, Multiframe messages are transferred tranparently every superframe.

Loopback test modes

CAL/LBS/LB1E/LB2E/LBB1E/LBB2E
LB1E and LB2E instructions turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.
LBB1E and LBB2E instructions turn each individual B channel from GCI input to the GCI output. They may be set separately or together.
CAL instruction clears both loopbacks.
It is not allowed to set or clear a LB1, LB2, LBB1 or LBB2 loopback while a complete loopback is set by means of the C/I instruction ARL. LBS can be used as an alternate command to ARL.

Activation/Deactivation

In NT configuration :

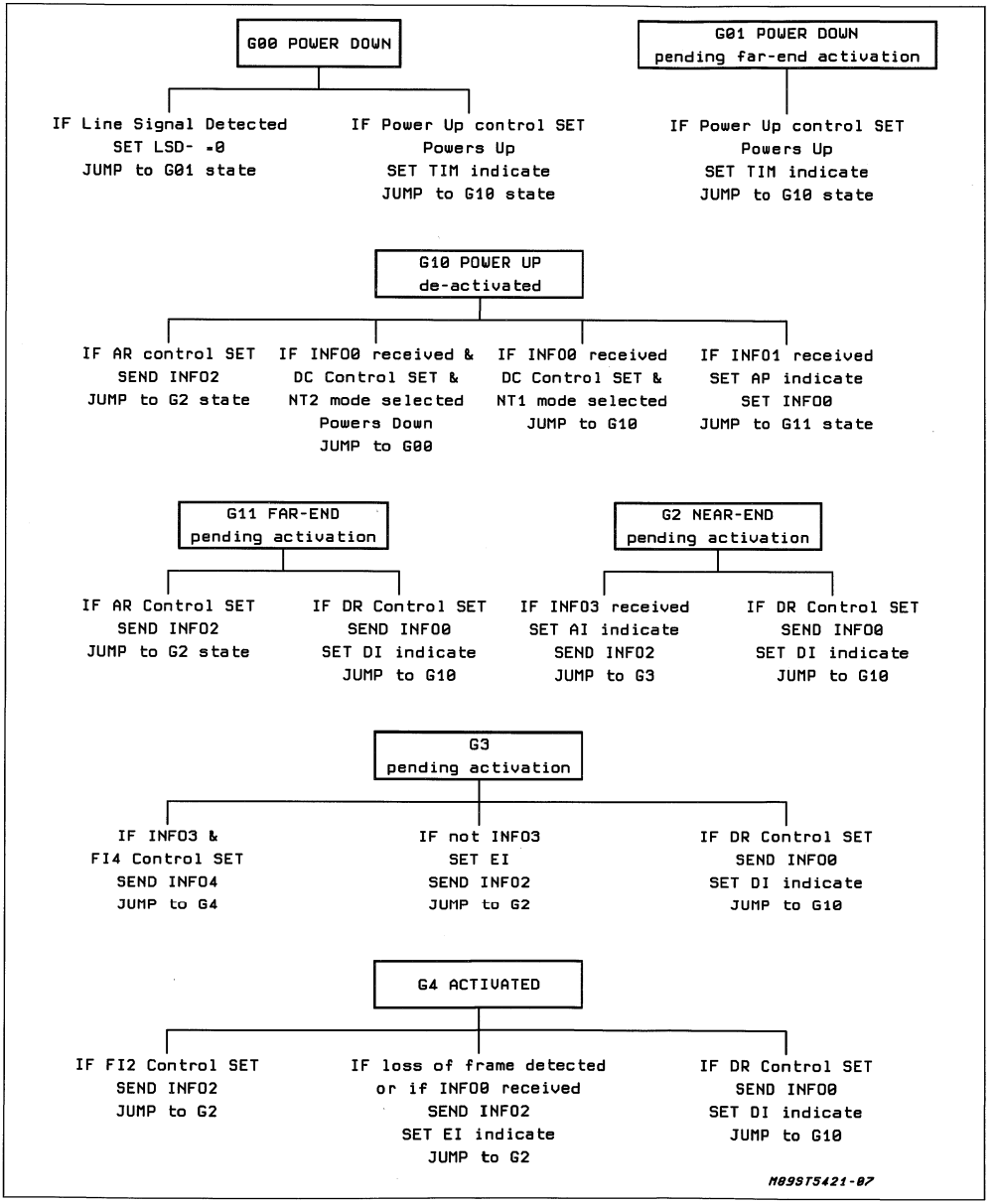
After Power on initialization, ST5421 can be con-

figured in NT1 or NT2 mode, by means of pins and register programming. In NT1, SID-GCI is powered up directly by receiving the GCI clocks on BCLK and FSa inputs. In NT2 mode, the device is powered up by means of PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop.

To operate an activation from the Network, ST5421 must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. Network timing,

Figure 5: Activation Procedure in GCI mode, NT Selected.



FSa, BCLK and MCLK must be present at this time. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector circuit pulls low LSD- pin, which can be used to wake up the system. A power Up procedure must be then be issued allowing identification of received signal ie, INFO1 or INFO2. The appropriate procedure is then followed according to I.430.

I.430 recommends that 2 Timers should be available in an NT. An Activation Request should be associated with the start of an external Timer 1 if required. Timer 1 should be stopped when the AI indication is generated following successful activation. If Timer 1 expires before AI is generated, however, Control instruction DR should be written to the device to force deactivation. Timer 2 which is specified to prevent unintentional re-activation, is not required since ST5421 can uniquely recognize INFO1 frames.
Two extra codes are needed for NT1 application: FI4 indicates to the SID-GCI that the U line is activated and allows completion of activation by sending INFO4. FI2 indicates to SID-GCI that the U line has lost synchronization and requests sending of INFO2.

In TEM or TES configuration :
After Power on initialization, ST5421 can be configured in TE or TES power down mode, depending on pins and register configuration setting. In TEM mode, SID-GCI is powered up by pulling low the Bx input. SID-GCI reacts by sending GCI free-running clocks. In TES mode, the SID-GCI is powered up by means of the PUP code on the C/I Control channel.

Activation may be initiated from either end of the loop. To operate an activation from the Terminal, the device must be first powered up by the appropriate procedure followed at least 2ms later by an AR instruction on the C/I channel. When activation is initiated by the far-end, SID-GCI being in the Power Down state, a Line Signal Detector Circuit pulls low the LSD- pin, which can be used to wake up the system. A Power Up procedure must then be issued allowing identification of received signal ie, INFO2. The appropriate procedure is then followed according to I.430.

Figure 6: Activation Procedure in GCI mode, TE Selected

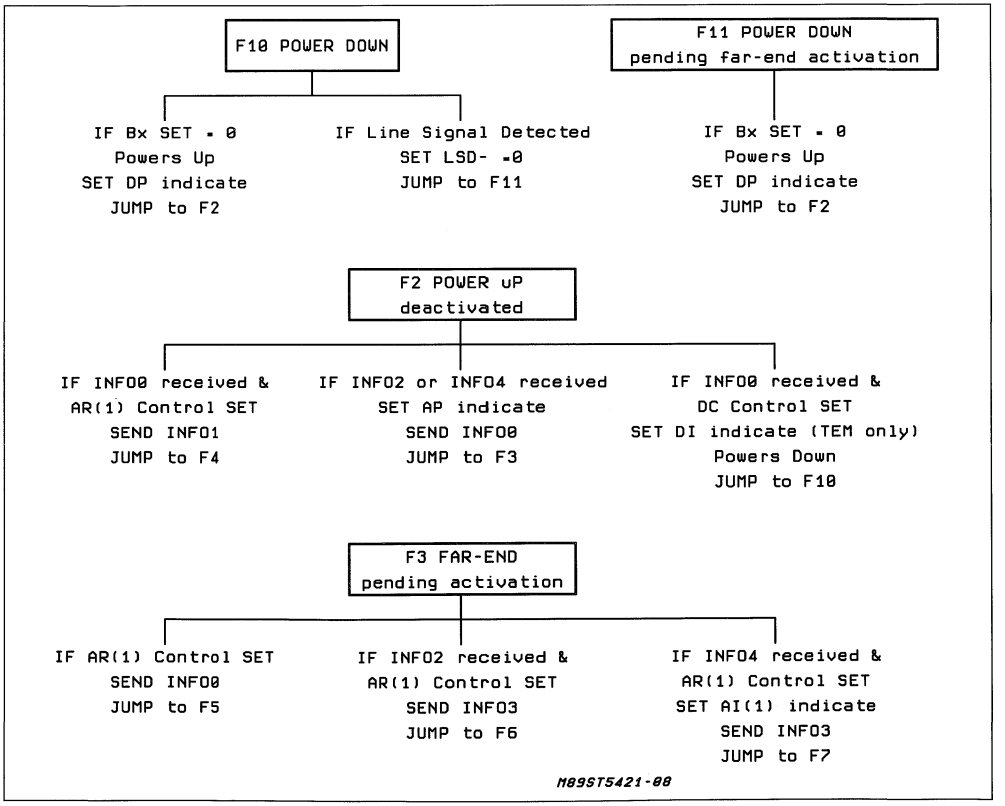
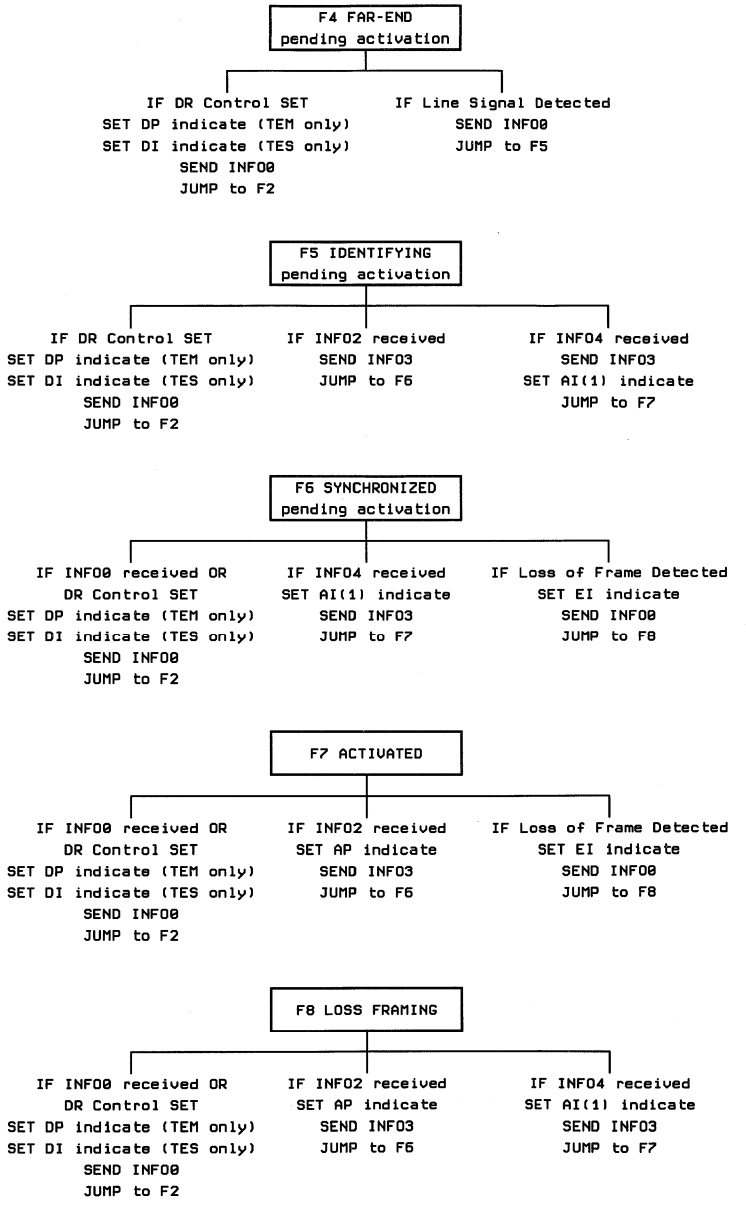


Figure 6: Continued



I.430 recommends that a Timer should be available in a TE. An Activation Request to the SID-GCI should be associated with the start of an external Timer 3 if required.Timer 3 should be stopped when the AI indication is generated following successful activation. Timer 3 expires before AI, AI8 or AI10 is generated, however, Control instruction DR should be written to the device to force de-activation.

D CHANNEL ACCESS IN TEM MODE

A controller device requiring to start transmission of a packet on the line should first prepare the complete message such that the opening Flag is ready to be shifted accross GCI. A Control Instruction AR8 or AR10 will initiate first the Activation Sequence on the line until activation has been completed and then the D channel access sequence according to Priority Class 1 (signalling) or Priority Class 2 (Data packet) respectively.

After line activation, AI8 (or AI10) indication is sent from SID-GCI. Then, DEN output immediately enables to prefetch the opening flag from the controller device into the SID-GCI D channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface is transmitting in the D channel. This is assured by counting consecutive "1"s in the E bit position of frames received from the NT and comparing the value with the current priority level as specified by I.430. If another TE is active in the D channel, DEN pulses are inhibited once the Opening Flag is in the Transmit buffer to prevent further fetching of Transmit data from the Controller until D channel access is achieved.

As soon as the required number of consecutive E bit "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D bit position to the NT. Then, DEN pulses are re-enabled in order to get new D channel bits. No other instructions are necessary for local flow control between controller and ST5421.

During transmission in the D channel, SID-GCI continues to compare each E bit with the D bit previously transmitted before proceeding to send the next. In case of mis-match, a contention for the previous D bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D bit positions. Status indication CON is sent to the controller on C/I channel. DEN output pulses are again inhibited, and D channel access sequence is disabled.

In order to retransmit the lost frame, the controller must begin as before sending a new AR8 (or AR10) ; it has to change first the code sent (ie DI) and after change again to AR8. Successful sending of a transmit frame is detected when the closing Flag is transmitted in the D channel. "1"s are then transmitted in the following D bit positions.

If enabled by the Control Instruction EIE, indication EOM is sent to indicate the End of message.

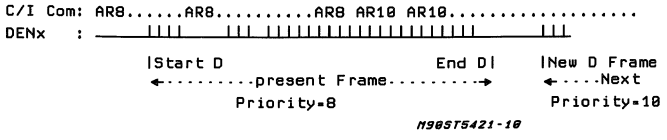
After sending of a transmit frame successfull, SID GCI will automatically perform a new D access sequence if it's still receiving AR8 or AR10 command on C/I channel, otherwise no D access sequence will be done until reception of AR8 or AR10 command.

Any indication change on the C/I channel except EOM indicates deactivation of the D channel access sequence and a new AR8 (or AR10) is needed to restart the procedure.

Note: Users willing to control the D channel access, can use this procedure:
Send AR8 or AR10 until receiving DENx, then remove ARx command code and replace it by an another command (ie DI that is equivalent to a NOP operation if the device is full_activated). At the end of a D frame EOM Indication is received (if EIE is set); when a new D message is prepared an ask for a new D channel access by AR8 or AR10 can be sent.

Users that want to discriminate consecutive D channel access with EOM Indication, are suggested to remove EOM Indication, between 2 D frames, to be able to separate the 2 messages EOM: With the following method: send AR8 (AR10) continuously, until receiving EOM Indication, then send ONCE AR8~ [0111] (AR10~ [0110]) on C/I channel and continue to send the previous code AR8 (AR10); this AR8~ (AR10~) is a kind of EOM aknowledge: the device detect a 'new' primitive AR8 (AR10), stop EOM Indication and replace it by AI8 or AI10 if ST5421 is still full activated.

For application with automatic D channel access and wanting to change the priority class (8 or 10) for D channel, they can use the following procedure:
Assuming that the present D frame is priority class 8 and that the next D frame will be priority class 10, users can change AR8 code to AR10 as soon as they are sure that the present D frame is started, by controlling DENx, anticipating the next D messages before the closing flag of the present D frame. When the automatic D channel access will be performed for next D message, the D channel request will be done with the desired priority class. (see figure below).



MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S interface includes a low-speed (800 b/s) channel for loop maintenance accessed via the monitor channel of ST5421. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table 5. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and enables the MFR message. The algorithm is present during INFO2 and INFO4 frames. In TE modes this command only enables the MFR message since the device will always search for and synchronize to the multiframing identification bits if NT is sending them. In all modes, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before a MFR message is generated. Table 5 lists the codes which are 3-times checked. Note, however, that no other action is taken by the ST5421 in response to received codes (e.g. loop-backs are not automotically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constrains from the device, and to utilise the unassigned codes for other functions.
It is possible to disable the checking algorithm by setting DIS3X instruction on M channel. There, Multiframe words are transferred transparently on M channel.

The MID command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR message in both NT and TE modes. Both the MIE and MID commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "idle" messages, by means of an MFT instruction, prior to activation.

Table 5: Codes for Q and S1 channel messages

Message (1)	NT to TE					TE to NT				
	Received at TE				Number of Repetitions Before MFR message (EN3X set)	Received at NT				Number of Repetitions Before MFR message (EN3X set)
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (Normal)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	—	—	—	—	—
STF Fail	0	0	0	1	3	—	—	—	—	—
ST Request (3)	—	—	—	—	—	0	0	0	1	3
STI Indication	0	1	1	1	3	—	—	—	—	—
DTSE-IN	1	0	0	0	1	—	—	—	—	—
DTSE-OUT	0	1	0	0	1	—	—	—	—	—
DTSE-IN & OUT	1	1	0	0	1	—	—	—	—	—
LB1 Request	—	—	—	—	—	0	1	1	1	3
LB1/Indication	1	1	0	1	3	—	—	—	—	—
LB2 Request	—	—	—	—	—	1	0	1	1	3
LB2/Indication	1	0	1	1	3	—	—	—	—	—
LB1/2Request (2)	—	—	—	—	—	0	0	1	1	3
LB1/2Indication	1	0	0	1	3	—	—	—	—	—
Loss-of-Received Signal Indication	1	0	1	0	3	—	—	—	—	—
Unassigned	All other codes				1	All other codes				1

Notes:
(1) No autonomous action is taken by ST5421 in response to received messages. Where appropriate, the external controller must respond with a command or other action.
(2) The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.
(3) The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Figure 7: ISDN Telephone Set Application (non isolated)

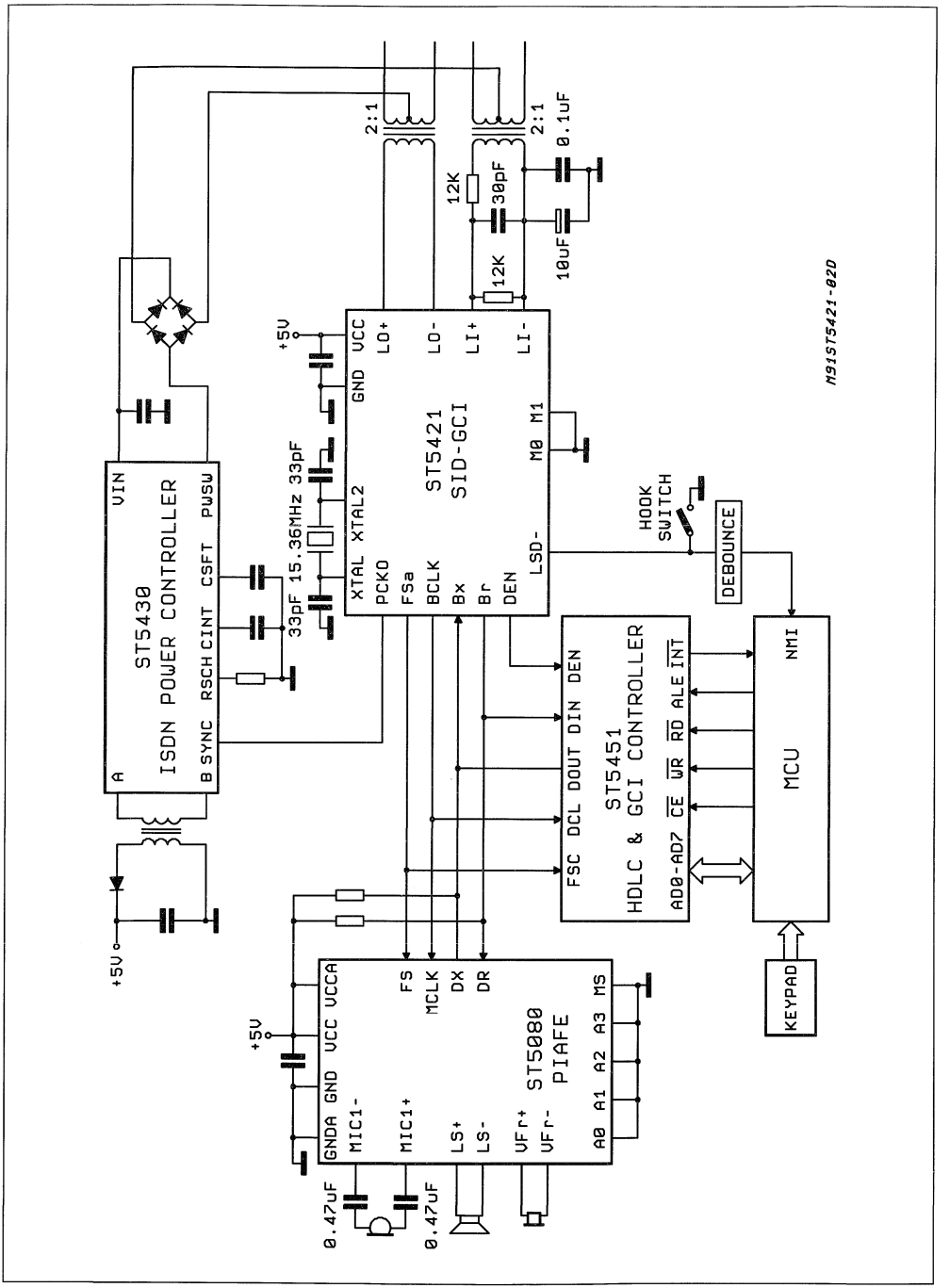
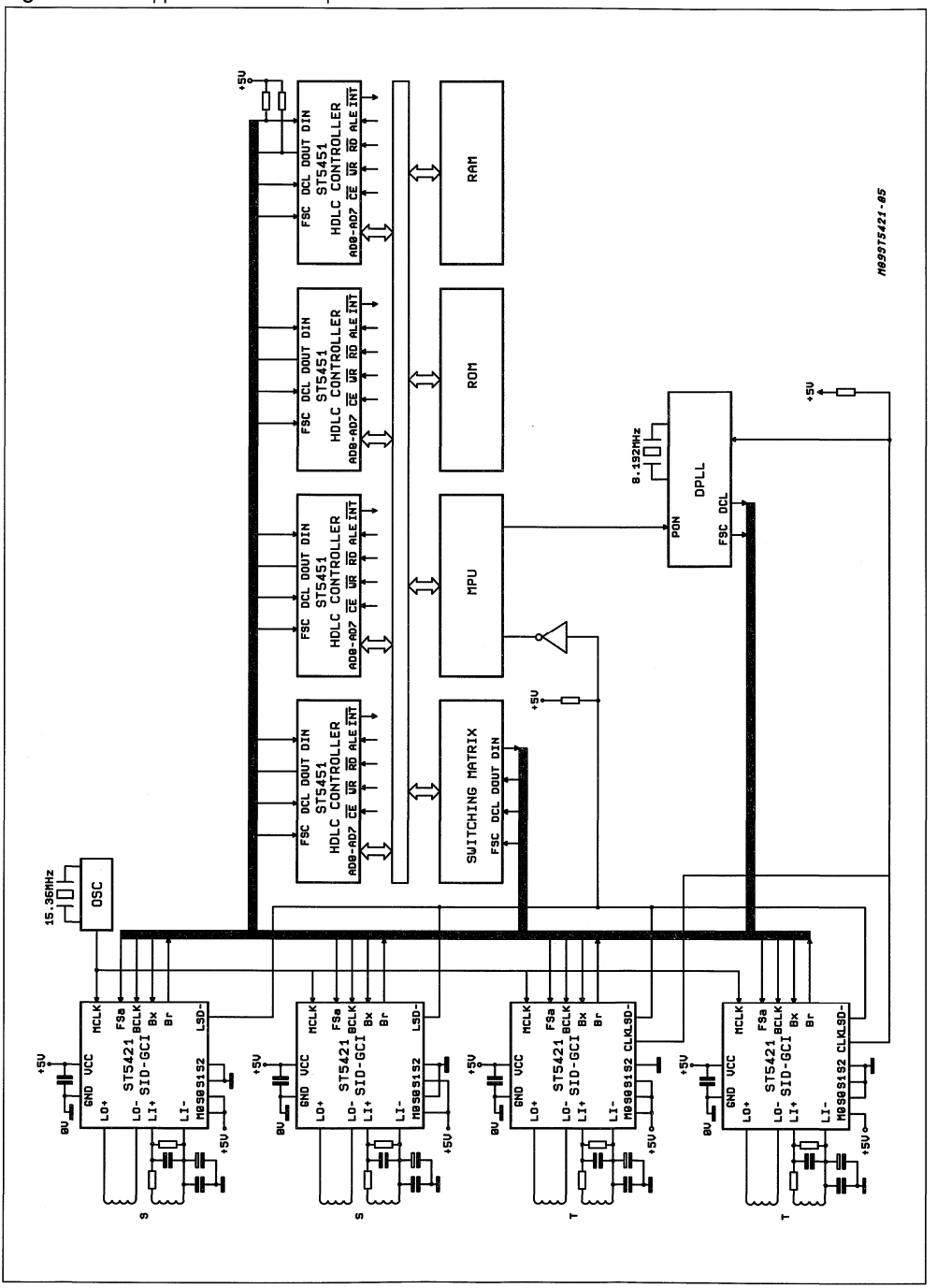


Figure 8: NT2 Application GCI Compatible



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Voltage at Bx, Br	V_{CC} + 1 to GND - 1	V
Voltage at any Digital Input (except Bx)	V_{CC} + 1 to GND - 1	V
Current at any Digital Input (except Br)	± 50	mA
Current at Lo	± 100	mA
Storage Temperature Range	-65 to +150	°C
Lead Temperature (soldering 10s)	300	°C

ELECTRICAL CHARACTERISTICS (unless specified otherwise: V_{CC} = 5V ±5%, T_A = 0 °C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND).

DIGITAL INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL input	V_{CC}-0.5			V
V_{OL}	Output Low Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA			0.4	V
V_{OH}	Output High Voltage	Br: I_L = 3.2 mA All other Digital Outputs: I_L = ±1mA All outputs, I_L = 100µA	2.4 2.4 V_{CC}-0.5			V V V
I_{IL}	Input Low Current	Any Digital Input, GND < VIN < V_{IL}	-10		+10	µA
I_{IH}	Input High Current	Any Digital Input, VIH < V_{IN} < V_{CC}	-10		+10	µA
I_{OZ}	Output Current in HIGH Impedance (tri-state)	All Digital Tri-state I/Os	-10		+10	µA

LINE INTERFACE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
R_{LI}	Differential Input Resistance	GND < LI_+, LI- < V_{CC}	200			kΩ
C_{LLO}	Load Capacitance	From LO+ to LO-			200	pF
V_{OS}	Differential Offset Voltage at L_{O+}, L_{O-}	Driving Binary 1s, 220Ω between LO+ and LO-	-20		20	mV

POWER DISSIPATION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CC}0$	Power Down Current	All Outputs Open-circuit			850	µA
$I_{CC}1$	Power Up Current	Device Deactivated (Note1)			16	mA

Note1: when the device is activated and driving a correct terminated line, ICC1 increases by several mA. A worst case data pattarn, consisting of all binary O'S increases ICC1 by apprximately 8mA.

ELECTRICAL CHARACTERISTICS (continued)

TRANSMISSION PERFORMANCE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	Transmit Pulse Amplitude	Conform to all CCITT I430 requirenents using the specified transformer. (see transformer model)				
		R_L 220Ω between L_{O+} and L_{O-}	±1.4		±1.6	Vpk
	Transmit Pulse unbalance	0^+ reletive to 0^-			±5	%
	Input Pulse Amplitude	Differential between L_{I+} &L_{I-}	±175			mVpk

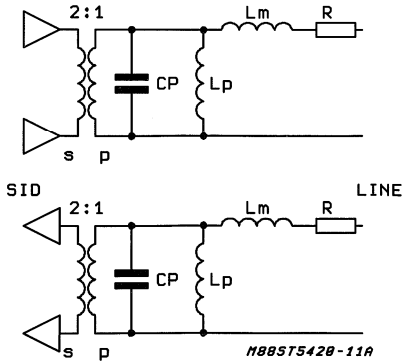
MASTERCLOCK

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
	MCLK Frequency			15.36		MHz
	MCLK Frequency Tolerance		-100		100	ppm
	MCLK Input Clock Jitter				50	ns pk-pk
	Timing Recovery Jitter	BCLK Output Relative to MCLK at TE	-130		130	ns
t_{MH}, t_{ML}	Clock Pulse width High and Low of MCLK	$V_{IH} = V_{CC}$ -0.5V, V_{IL} = 0.5V	20			ns
t_{MR}, t_{MF}	Rise Time and Fall Time of MCLK	Used as a logical input			10	ns

TRANSFORMER MODEL (all values are to be measured at 10kHz)

		Min.	Typ.	Max.	Unit
1:N	Primary to Secondary Turn Ratio	-1%	2	1%	
R	Primary Total DC Resistance		12		Ohm
Lp	Primary Inductance	22	30	37.5	mH
Lm	Primary Inductance with Secondary Shorted		16	20	mH
Cp	Primary Capacitance with Secondary Open			25	pF

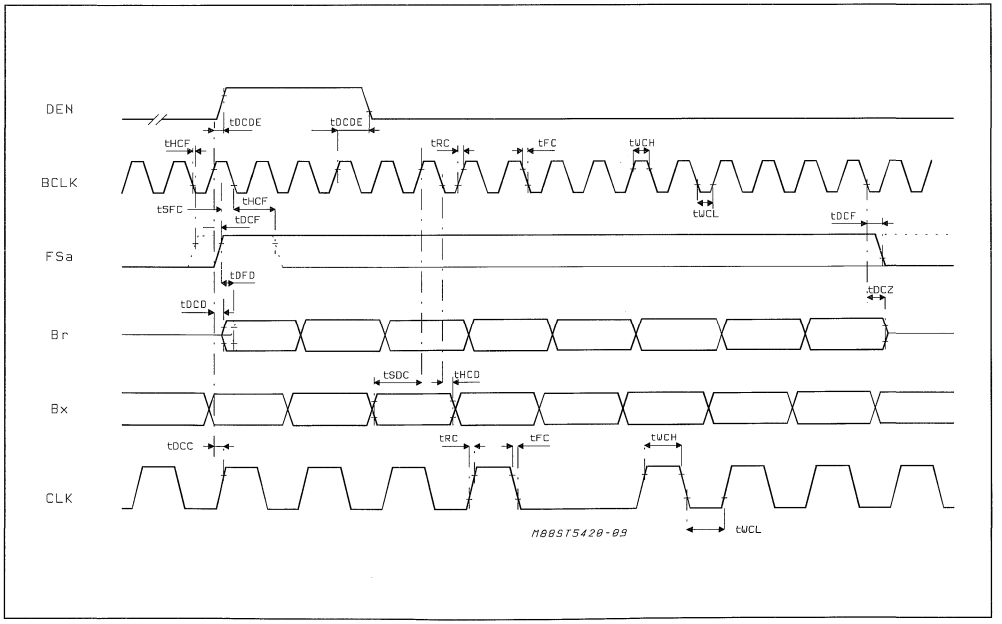
Figure 9: Transmit & Receive Transformer Model



TIMING SPECIFICATIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{DCDE}	Delay Time BCLK High to DEN Transition	TE Mode only			30	ns
t_{HCF}	Hold Time BCLK Trans. to FSa Transition		0			ns
t_{RC}, t_{FC}	Rise & Fall Time BCLK				15	ns
t_{WCH}, t_{WCL}	BCLK width High & Low		60			ns
t_{SFC}	Setup Time FSa High to BCLK Low		70		BCLK -50	ns
t_{DCF}	Delay Time BCLK High to FSa HIGH	TE Mode only			30	ns
t_{DCD}	Delay Time BCLK High to DATA Valid		20		80	ns
t_{DFD}	Delay Time FSa High to Data Valid	Load 100pF. Apply only if FSa rises later than BCLK rising edge			80	ns
t_{DCZ}	Delay Time BCLK Low Data Invalid		50		120	ns
t_{SDC}	Setup Time Data Valid to BCLK Low		30			ns
t_{HDC}	Hold Time BCLK Low to Data Invalid		20			ns
t_{DCC}	Delay Time BCLK High to CLK High	TE and TES side modes only	0		30	ns

Figure 10: GCI Mode



APPLICATIONS INFORMATION

While the pins of ST5421 SID-GCI device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND to the device before any other connections, should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.15F should be connected from this common point to V_{CC} as close as possible to the device pins.

CRYSTAL OSCILLATOR

The clock source for ST5421 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

CRYSTAL SPECIFICATION

ST5421 SID-GCI clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of 1 100ppm total to comply with the CCITT I.430 specification for TE applications.The frequency tolerance limits span the conditions of full operating temeprature range (commercial or industrial) and effects due to aging and part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33pF total capacitance from each pin to ground. The external capacitors must be mica or high-Q ceramic type. The use of NPO (Negative Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33pF capacitance includes the external capacitor plus any trace and lead capacitance on the board. Nominal frequency of 15.360MHz, frequency tolerance (accuracy, temperature and aging) less than 1.60ppm, with Rs = 150, CL= 20pF, parallel mode, C0 (shunt capacitance) 7pF.An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50K shunted by a total of 33pF of capacitance. Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

EXTERNAL OSCILLATOR CONFIGURATION

An external 5V drive clock sourcxed may be connected to the MCLK (pin 5) input pin of ST5421. The nominal frequency should be 15.36MHz with a tolerance of 1 80ppm. The ST5421 SID provides a load of about 7pF at the MCLK input pin.

LINE TRANSFORMER REQUIREMENTS

The electrical characteristics of the pulse transformer for the ISDN "S" interface are defined to meet the output and input signal and the line isolation and characteristics as defined in CCITT reccommednation I.430. The transformer provides isolation for the line card or terminal from the line it lasi provides a means to transfer power to the terminalb over the S-loop via the "phantom" circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with ST5421 to meet the CCITT recommendation on output pulse mask and impedance requirements.

LINE TRANSFORMER RATIO

The transmit and th receive transformers can be the same (with a winding ratio of 1:2) or optionally, the receive transformer could have a transformer ratio of 1:1. The primary of the transformer is connected to the S loop while the secondary is connected to the device.

EXTERNAL PROTECTION CIRCUITRY

Precautions are to be taken to ensure that ST5421 SID-GCI is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightening discharge that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer.

DC BIAS CAPACITORS FOR ANALOG REFERENCE

Two decoupling capacitors (0.1µF mica) and 10µF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

ST5421 EXCEEDING I.430 TRANSMISSION RE-

QUIREMENTS

This ST5421 is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the ST5421 SID design by employing superior analog front end designs. For example, in the receive path, an analog prefiter removes <200kHz noise signals, which is then followed by an adaptive line equalizer to accomodate varying line conditions with superior performance. A continuously tracking adaptive threshold circuit provides the slicing levels for the detection circuits for correct interpretation of transmission bits even on long lossy loops. This implementation results in longer ranges of S interface cables compared to I.430 requirements.

ISDN POWER SUPPLY

ADVANCE DATA

APPLICATIONS

- SWITCH MODE POWER SUPPLIES FOR ISDN APPLICATIONS
- SUITABLE AS A DC/DC CONVERTER IN TE, NT AND LT APPLICATIONS
- EXTRACTOR/FEEDER IN NT's
- EMERGENCY POWER EXTRACTOR IN TE
- ISOLATED AND NON-ISOLATED APPLICATIONS SUPPORTED
- COMPLIES WITH CCITT I.430 S BUS RECOMMENDATIONS

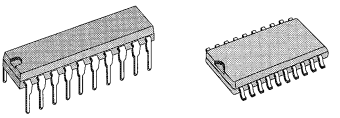
FEATURES

- LARGE INPUT VOLTAGE RANGE 24V-90V
- DEVICE SUPPLY VOLTAGE RANGE 5V-8V
- HIGH EFFICIENCY:
  >50% at P = 25mW
  >80% at P = 1.0W
- BURST MODE REGULATION AT LOW POWER, FOR EFFICIENCY IMPROVEMENT
- EXTERNAL MOS DRIVER FOR HIGH CURRENT/POWER APPLICATIONS
- FREE FREQUENCY OSCILLATOR (10KHz to 100kHz) WITH SYNCHRONIZATION POSSIBILITY
- OVERCURRENT DETECTION WITH FOLDBACK LIMITATION
- INTEGRATED SOFT START
- UNDERVOLTAGE DETECTION
- POLARITY REVERSAL DETECTION AND SIGNALING
- PRIMARY "START UP" CURRENT LIMITATION

DESCRIPTION

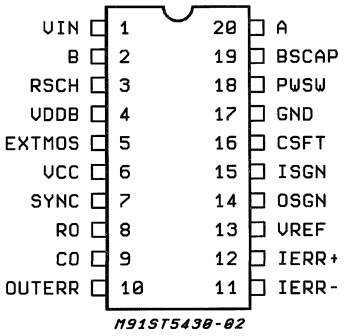
The ST5430 is a ISDN Switch Mode Power Supply specifically designed to be used in all the ISDN configurations:
-LT: U line powering from CO battery
-NT:
a) Power extractor from U line
b) NT, U and S device powering at +5V
c) S bus emergency powering at 40V

MULTIPOWER BCD TECHNOLOGY



DIP20 SO20

PIN CONNECTION (Top view)



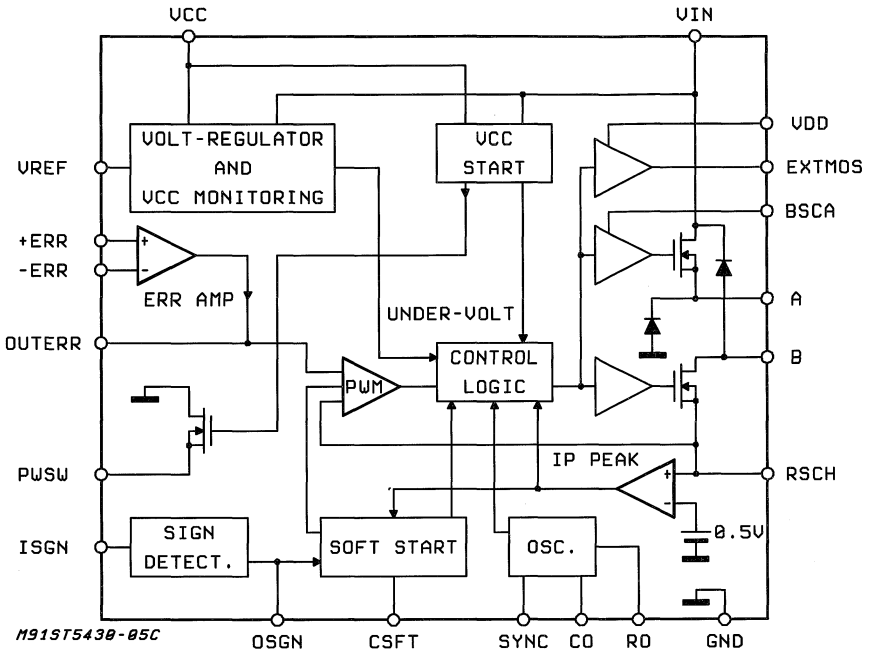
-TE:
a) Emergency power extractor from S bus
b) TE devices powering at +5V
It performs the functions of Switch Mode Power Supply for flyback converter with current mode feedback.
The ST5430 is relaized with BCD technology featuring, 5V CMOS, 40V Bipolar and 100V DMOS, for high efficiency design both in size and in power consumption.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

PIN FUNCTIONS

No.	Name	Description
1	Vin	Input Voltage (24V to 90V)
2	B	Negative Side of Primary Transformer Winding
3	RSCH	Primary Current Sense Resistor
4	VDD	External Mos Buffer Supply Voltage
5	EXTMOS	External Mos Gate Drive
6	Vcc	Supply Voltage
7	SYNC	Input Synchronization
8	Ro	Oscillator Resistor
9	Co	Oscillator Capacitor
10	OUTERR	Output of Error Amplifier
11	IERR–	Negative Input of Error Amplifier
12	IERR+	Positive Input of Error Amplifier
13	Vref	Voltage Reference Output
14	OSGN	Output Sign of V_{IN}
15	ISGN	Input for Sign Detection of V_{IN}
16	CSFT	Soft Start Capacitor
17	GND	Ground
18	PWSW	Power on Switch
19	BSCA	Bootstrap Capacitor
20	A	Positive Side at Primary Transformer Winding

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC},V_{DD}	Supply Voltage	8	V
V_{IN}	Input Voltage	90	V
$I_{O\,rms}$	Output Current (Pins A & B)	0.5	A
T_{STG}	Storage Temperature	-65 to +125	°C
T_{OP}	Operating Temperature	-40 to +85	°C
T_J	Junction Temperature	125	°C

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V, V_{IN} = 24V, T_{amb} = 25°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{REF1}	Voltage Reference			1.2		V
Z_{REF}	Output Impedance			13		Ω
V_{CRJ}	V_{CC} Rejection	V_{CCAC} = 0.1V_{rms} f = 1KHz	45			dB
I_{OREF}	Max Out Current	V_{CC} = 5V	–10		+10	µA
V_{no}	Noise Voltage			100		nV/√Hz
$V_{CC\ min}$	Supply Voltage	@ V_{REF} = 0.9 · V_{REF1}	3			V

OSCILLATOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
F_{max}	Maximum Frequency				100	kHz
A_{CCF}	Accuracy	Δf / f f=20kHz V_{CC}=5V	–5		+5	%
V_{CCREJ}	Freq. Stability vs V_{CC}	4.5V < V_{CC} < 5.5V		0.4		% / V
V_{RO}	Out RO Voltage			1.2		V
I_{SYNC}	INPUT SYNCHRO CURRENT	V_{SYNC} = 0V			1	µA
I_{CO+}	Capacitor charge current with R_O = 62kΩ	V_{CC} = 5V		18		µA
I_{CO-}		V_{CC} = 5V		–18		µA

ERROR AMPLIFIER

Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit
I_{BIAS}	IN Bias Current	V_{CC} = 5V		15	30	nA
V_{IO}	IN Offset Voltage			5		mV
I_{IO}	IN Offset Current			2	20	nA
G_{wr}	Gain Band Product	C_{LOAD}=12pF R_{LOAD}=10MΩ		300		kHz
O_{VG}	Open Loop Voltage Gain			100		dB
I_{OERR+}	Output Positive Current	V_{CC} = 5V V_{OUT}=1V	0.5			mA
I_{OERR-}	Output Negative Current 1	V_{CC} = 5V V_{OUT}=0.5V	–5			µA
I_{OERR-}	Output Negative Current 2	V_{CC} = 5V V_{OUT}=1.5V			–0.5	mA
C_{CMR}	Commun Mode Rejection	V_{INCM}=0.1Vrms	–65			dB
SVR	Supply Voltage Ratio Rejection	V_{CCAC}=0.1Vrms f=1kHz	–65			dB
SB	Slew Rate			0.14		V / µs
I_{CMV}	Input Common Mode Voltage		0		3	V
O_{SV}	Output Swing Voltage		0.1		3	V
V_n	Input Equiv. Noise Voltage	f=1kHz , Rs=10Ω		40		nV/√Hz

SUPPLY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{VCC}	V_{CC} Current	f = 20kHz		0.8	2	mA
I_{VCCF}	V_{CC} Dynamic Current	f = 100kHz			4	mA
I_{VIN}	Input V_{IN} DC Current	V_{IN} = 100V; V_{CC} = 5.0V f = 20kHz		0.35		mA

OUTPUT DMOS CIRCUIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
R_{onA}	A Output on Resistance	V_{CC} = 5V		2.2	4	Ω
I_{AMax}	A Output Current	V_{CC} = 5V	250			mA
t_{DHL}	Delay Out A / Osc			550		ns
t_{DLH}				400		ns
R_{onB}	B Output on Resistance	V_{CC} = 5V		2.2	4	Ω
I_{Bmax}	B Output Current	V_{CC} = 5V			–250	mA
t_{DHL}	Delay Out B / Osc			450		ns
t_{DLH}				400		ns
I_{outB+}	External Mos Output Buffer current	V_{CC} = 5V V_{DD} = 5V	10	20		mA
I_{outB-}				–40	–20	mA

POWER ON CIRCUIT

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{INmin}	Min. Input Voltage	V_{CC} = 5V		22	24	V
R_{ONpw}	Power Switch R_{ON}			2.2		Ω
V_{CCDET}	V_{CC} Detection		4.5		7	V
I_{VCCST}	Start V_{CC} Current		2.5	3.5		mA
I_{BST}	Bootstrap Current	f = 15KHz f = 20KHz		0.25		mA

SIGN OF V_{IN} DETECTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{OH}	Output	V_{14} = 1V, V_{15} = 0.5V		–12	–5	µA
V_{OL}		V_{CC} = 5V, I_{14} = 0.5mA		0.4	0.5	V
V_{TH}	Input	Threshold Voltage	1	1.4	2	V
INLO		V_{CC} = 5V	1	2.2	5	µA

SOFT START CAPACITOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{STC}	Charge Current		7	9	11	µA

PEAK PRIMARY CURRENT DETECTOR

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{THIP}	Threshold Voltage			0.55		V

Figure 1: Application with internal DMOS

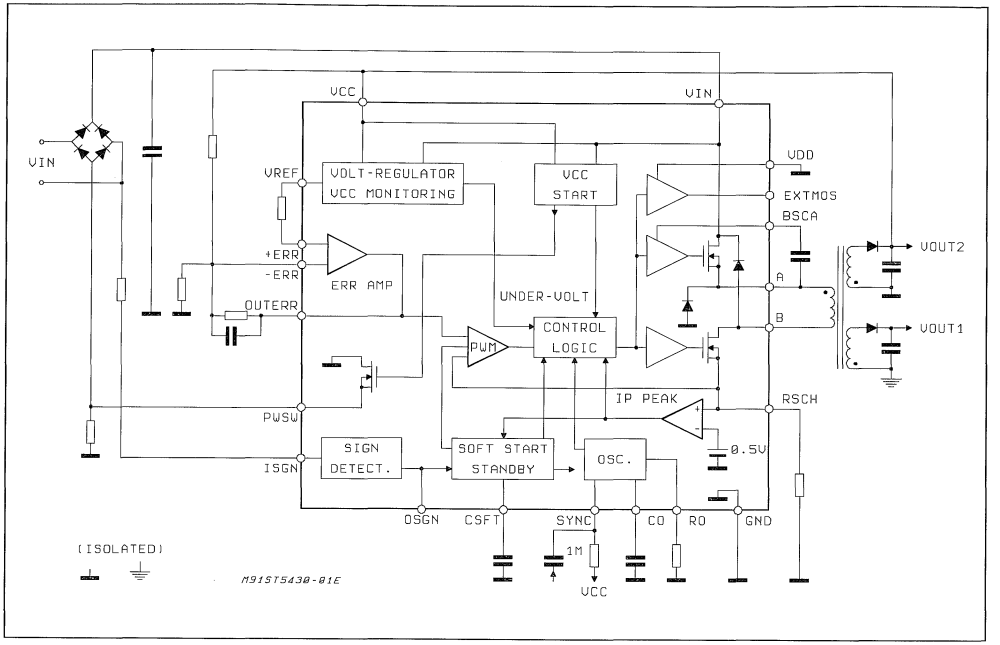
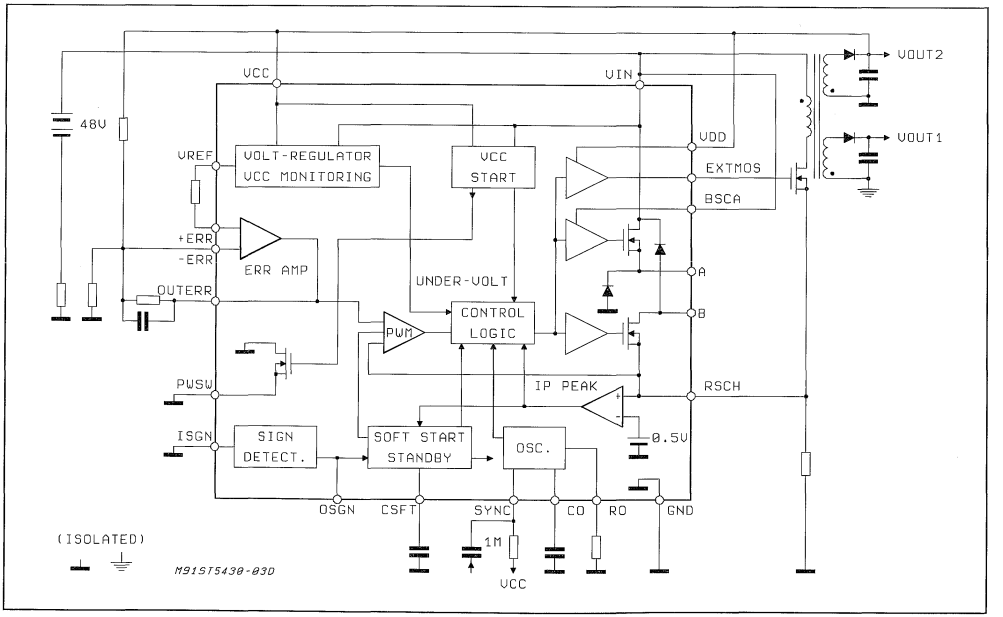


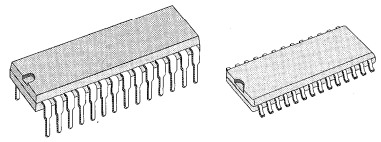
Figure 2: Application with external MOS



ISDN HDLC AND GCI CONTROLLER

ADVANCE DATA

- MONOLITHIC ISDN ORIENTED HDLC AND GCI CONTROLLER.
- GCI AND µW/DSI COMPATIBLE.
- FULLY CONTROLLING GCI AND GCI-SCIT M & C/I CHANNELS MANAGEMENT.
- FULLY SUPPORTING LAPB AND LAPD PROTOCOL ON B OR D CHANNEL.
- EASILY INTERFACEABLE WITH ANY KIND OF STANDARD NON MULTIPLEXED OR MULTIPLEXED BUS MICROPROCESSOR.
- DMA ACCESS WITH MULTIPLEXED BUS µP
- CAN HANDLE AND STORE AT THE SAME TIME TWO FRAMES IN TRANSMISSION (64bytes FIFO Tx) AND EIGHT FRAMES IN RECEPTION (64bytes FIFO Rx)
- COMPATIBLE WITH ALL THE SGS-THOMSON ISDN PRODUCT FAMILY.

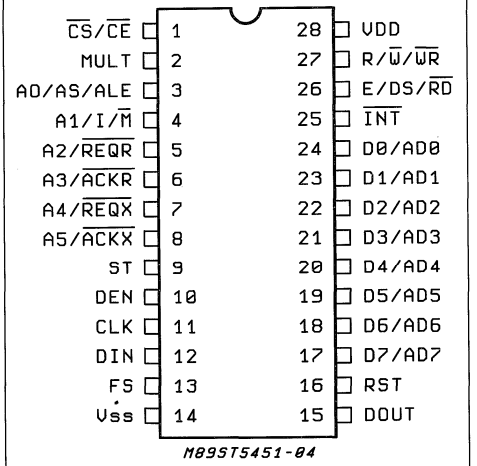


DIP28 SO28

ORDERING NUMBERS:

ST5451N ST5451D

PIN CONNECTION (Top view)

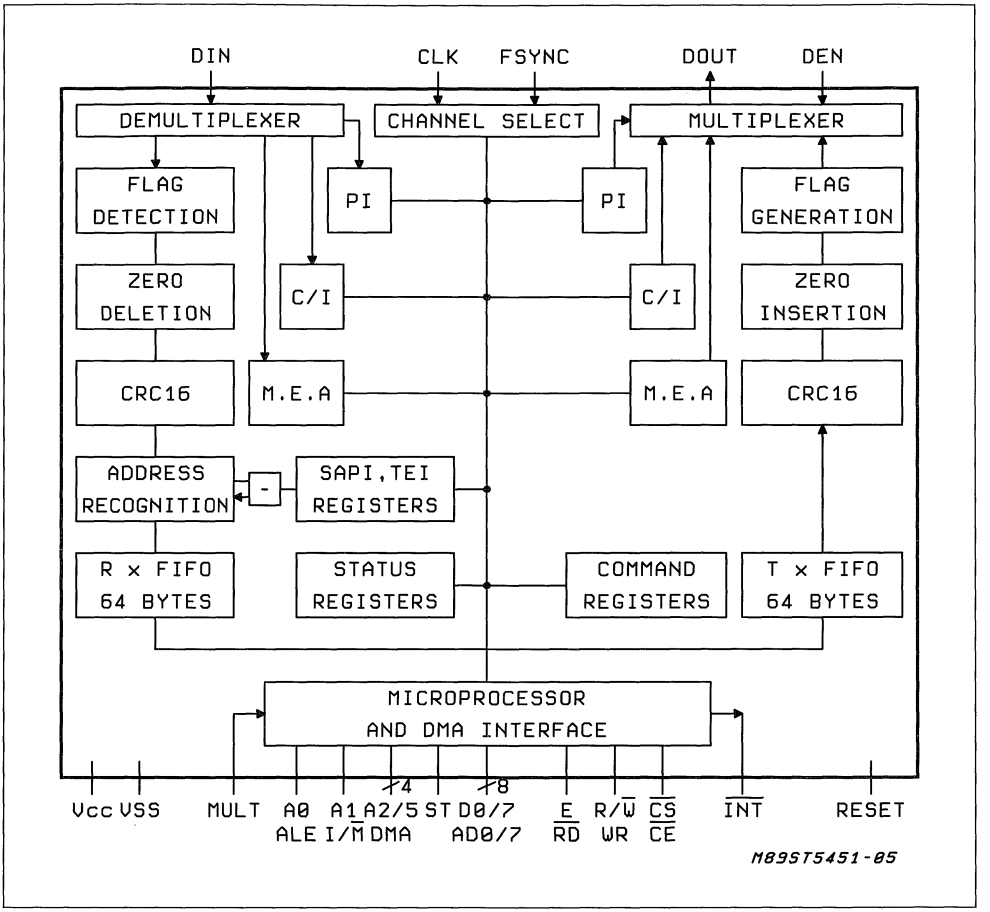


GENERAL DESCRIPTION

ST5451 HDLC and GCI controller is a CMOS circuit fully developed by SGS-THOMSON and diffused in advanced 1.2 µm HCMOS3 technology.
The device is intended to be used mainly in ISDN applications, in Terminal (TE) and in Line Terminations (LT).
ST5451 can handle HDLC packets either on 16Kbit/s D channel or 64 Kbit/s B channel; it can work with a wide range of PCM signals going from GCI (General Circuit Interface) to DSI (Digital System Interface) to any PCM-like stream.
ST5451 is a complete GCI controller designed to comply with the GCI and GCI-SCIT (Special Circuit Interface for Terminal) completely handling Monitor (M) and Command/Indicate (C/I) channels.
ST5451 can be easily controlled by many different kind of microprocessors or microcontrollers having either non-multiplexed or multiplexed bus structure.
ST5451 can be used in connection with ST5420/1 S Interface Devices (SID-µW and SID-GCI) and ST5080 Programmable ISDN Combo (PIC) in Terminals and with ST5410 U Interface Device (UID) in Line Terminations.

This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

BLOCK DIAGRAM



PIN DESCRIPTION

NAME	PIN	TYPE	FUNCTION
$\overline{CS}$	1	I	Chip Select. A low level enables ST5451 for read/write operations.
$\overline{INT}$	25	O	Interrupt request is asserted by ST5451 when it request a service. Open drain output.
MULT	2	I	Multiplexed Bus. Indicates the µP bus interface selected. MULT = 1: multiplexed bus and DMA available. MULT = 0: address and data bus separated.
I/$\overline{M}$	4	I	Intel/Motorola. When MULT = 1 this pin selects either Intel or Motorola 6805 bus.

DEMULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 0)

NAME	PIN	TYPE	FUNCTION
A0/A5	3-8	I	Address Bus. To transfer addresses from µP to ST5451.
D0/D7	17-24	I/O	Data Bus. To transfer data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
E	26	I	Enable. Read/write operations are synchronized with this signal; its falling edge marks the end of an operation.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1 I/$\overline{M}$ = 1)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
$\overline{WR}$	27	I	Write. This signal indicates a write operation.
$\overline{RD}$	26	I	Read. This signal indicates a read operation.
ALE	3	I	Falling edge latches the address from the external A/D Bus.

MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 0)

NAME	PIN	TYPE	FUNCTION
AD0/AD7	17-24	I/O	Address Data Bus. To transfer addresses and data between µP and ST5451.
R/$\overline{W}$	27	I	Read/Write. "1" Indicates a write operation; "0" a write operation.
DS	26	I	Data Strobe. Read/Write operations are synchronized with this signal: its falling edge marks the end of an operation.
AS	3	I	Address Strobe. Falling edge latches the address from the external A/D Bus.

DMA (direct memory access): only when MULT = 1

NAME	PIN	TYPE	FUNCTION
$\overline{DMA\ REQ\ X}$ DMA REQ R	7 5	O O	Direct Memory Access Requests: these outputs are asserted by the device to request an exchange of byte from the memory.
$\overline{DMA\ ACK\ X}$ DMA ACK R	8 6	I I	Direct Memory Access Acknowledge: these inputs are asserted by the DMA controller to signal to the HDLC controller that a byte is being transferred in response to a previous transfer request.

GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	I/O	Data output for B and D channels. In GCI mode it outputs B1, B2, M and C/I channels. In TE mode (GCI-SCIT) it can invert to input data for M' and C/I' channels (See Table 2).
D_{IN}	12	I/O	Data input for B and D channels. In GCI mode it inputs B1, B2, M and C/I channels. In TE mode (GCI-SCIT) it can invert to output data for M' and C/I' channels (See Table 2).
C_{LK}	11	I	Data Clock. It determines the data shift rate for GCI channels on the module interface.
FS	13	I	Frame synchronization. This signal is a 8 kHz signal for frame synchronization. The front edge gives the time reference of the first bit in the frame.
DEN	10	I	Data Enable. In TE mode, this pin is a normally low input pulsing high to indicate the active bit times for D channel transmit at DOUT pin. It is intended to be gated with CLK to control the shifting of data from HDLC controller to S interface device.

NON GCI INTERFACE

NAME	PIN	TYPE	FUNCTION
D_{OUT}	15	O	Data output. Digital output for serial data. Three modes: - HDLC Protocol multiplexed link - HDLC Protocol non multiplexed link - Non HDLC protocol (transparent Mode).
D_{IN}	12	I	Data input. Digital input for serial data. Three modes (See D_{OUT}).
C_{LK}	11	I	Data Clock. It determines the data shift rate. Two modes: Single or double bit rate.
FS	13	I	Frame synchronization. Used in mode HDCL protocol multiplexed link. Don't care in other modes. The rising edge gives the time reference of the first bit of the frame.
DEN	10	I	Data Enable. When high, enable the data transfer. on D_{OUT}

OTHERS

NAME	PIN	TYPE	FUNCTION
V_{DD}	28	I	Positive power supply = 5V ±5%
V_{SS}	14	I	Signal ground
R_{ST}	16	I	Reset
ST	9	I	Special Test. (Reserved) must be tied to V_{SS}

2 - FUNCTIONS

2 - 1 - Basic HDLC Functions

2 - 1 - 1 - In Receive Direction:

- Channel selection
  In GCI channel B1 or B2 or D may be selected. B1 or B2 may be selected without M and C/I channels
- Flag detection
  A zero followed by six consecutive ones and another zero is recognized as a flag
- Zero delete
  A zero, after five consecutive ones within an HDLC frame, is deleted
- CRC checking
  The CRC field is checked according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Check for abort
  Seven or more consecutive ones are interpreted as an abort flag
- Check for idle
  Fifteen or more consecutive ones are interpreted as "idle"
- Minimum lenght checking
  HDLC frames with less than n bytes between start and end flag are ignored: allowed values are $3 \leq n \leq 6$.

This value is set by a programmable register

- Address Field recognition
  4 SAPI and/or 3 TEI may be recognized. Several programmable registers indicate the recognized address types.

2 - 1 - 2 - In Transmit Direction:

- Shift control in TE mode
  D channel data are signalled by DEN pin.
- Flag generation
  A flag is generated at the beginning and at the end of every frame.
- Zero insert
  A zero is inserted after five consecutive ones within an HDLC frame
- CRC generation
  The CRC field of the transmitted frame is generated according to the generator polynomial

$$X^{16} + X^{12} + X^5 + 1$$

- Abort sequence generation
  An HDLC frame may be terminated with an abort sequence under microprocessor control
- Interframe time fill
  Flags or idle (consecutive ones) may be transmitted during the interframe time. A programmable bit selects the mode.

2 - 2 - FIFO Structure

2 - 2 - 1 - Receive FIFO Structure

In receive direction, a 64 byte FIFO memory is used. It is divided in 8 blocks of 8 bytes automatically chained.

In case of a frame length of 64 bytes or less, the whole frame can be stored in the FIFO. After the first 32 bytes have been received µP is interrupted and may read the available data.

In case of frames longer than 64 bytes, the µP is interrupted to read out the FIFO by 32 byte block.

In case of several short frames, up to eight may be stored inside the FIFO. After an interrupt, one frame is available for the µP. The eventual other seven frames are queued and transferred one by one.

2 - 2 - 2 - Transmit FIFO Structure

In transmit direction, a 64 byte FIFO memory is used, structured in 2 blocks of 32 bytes. ST5451 is requested to transmit after 32 bytes have been written into the FIFO.

If a transmission request does not include a message end, the HDLC controller will request the next data block by an interrupt.

2 - 3 - Microprocessor Interface

Three types of microprocessor interfaces are available (MULT and I/$\overline{M}$ control pins set the desired interface).

- Motorola non multiplexed families.
- Motorola multiplexed family (6805 type)
- Intel family.

You can connect ST5451 to a Direct Memory Access Controller as MC68440 or MC6450 (dual or quad channels).

A programmable register indicates DMA Interface enabling.

TABLE 1 - ST5451 Internal Registers

Address Hexa	Read	Write
00	Receive FIFO	Transmit FIFO
1F	-	-
20	ISTA0	ISTA0
21	ISTA1	ISTA1
22	ISTA2	ISTA2
23	STAR	CMDR
24	MODE	MODE
25	RFBC	TSR
26	CA	CA
27	CB	CB
28	CC	CC
29	CD	CD
2A	CE	CE
2B	CF	CF
2C	CIR1	CIX1
2D	CIR2	CIX2
2E	MONR1	MONX1/0
2F	-	MONX1/1
30	MONR2	MONX2/0
31	-	MONX2/1
32	-	MASK0
33	-	MASK1
34	-	MASK2
3E	CCR	CCR

TABLE 2 - CHANNEL ASSIGNMENT SELECT

CF REGISTER								C/I		M		8KB/s		16KB/s		56KB/s		64KB/s		C/I'		M'		CI"	
TE	MAS /SSC	CCS	CMS /SC	PI	VZ DOUT	MSD1	MSD0	RX	TX	RX	TX	RX	TX	DR	DX	RX	TX	RX	TX	RX	TX	RX	TX	TX	
X	X	X	X	X	X	X	0	RX ON DIN TX ON DOUT																	CONTINUOUS MODE
X	X	0	0	X	X	0	1							DIN	DOUT										MULTIPLEXED NON GCI MODE
X	0	0	1	X	X	0	1					DIN (1)	DOUT (1)												
X	1	0	1	X	X	0	1					DIN (2)	DOUT (2)												
X	X	1	0	X	X	0	1											DIN	DOUT						
X	0	1	1	X	X	0	1					DIN (3)	DOUT (3)												
X	1	1	1	X	X	0	1									DIN (4)	DOUT (4)								
1	1	0	0	0	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										TERMINAL GCI MODE (D MASTER)
1	1	0	1	0	0/1	1	1	DIN	DOUT (5)	DIN	DOUT			DIN	DOUT (5)									DOUT (6)	
1	1	0	0	1	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)		
1	1	0	1	1	0/1	1	1	DIN	DOUT (5)	DIN	DOUT			DIN	DOUT (5)					DOUT (5)	DIN (5)	DOUT (5)	DIN (5)	DOUT (6)	
1	0	0	0	0	0/1	1	1	DIN	DOUT					DIN	DOUT										TERMINAL GCI MODE (D SLAVE)
1	0	0	1	0	0/1	1	1	DIN	DOUT (5)					DIN	DOUT (5)									DOUT (6)	
1	0	0	0	1	0/1	1	1	DIN	DOUT					DIN	DOUT					DIN	DOUT	DIN	DOUT		
1	0	0	1	1	0/1	1	1	DIN	DOUT (5)					DIN	DOUT (6)					DIN	DOUT	DIN	DOUT	DOUT (6)	
1	X	1	0	0	0/1	1	1	DIN	DOUT									DIN	DOUT						TERMINAL GCI MODE (B1 or B2)
1	0	1	1	0	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)												
1	1	1	1	0	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)								
1	X	1	0	1	0/1	1	1	DIN	DOUT									DIN	DOUT	DIN	DOUT	DIN	DOUT		
1	0	1	1	1	0/1	1	1	DIN	DOUT			DIN (3)	DOUT (3)							DIN	DOUT	DIN	DOUT		
1	1	1	1	1	0/1	1	1	DIN	DOUT							DIN (4)	DOUT (4)			DIN	DOUT	DIN	DOUT		
0	X	0	X	X	0/1	1	1	DIN	DOUT	DIN	DOUT			DIN	DOUT										REGULAR GCI MODE

(1) FIRST BIT OF 16KB/S CHANNEL SELECTED
(2) SECOND BIT OF THE 16KB/S CHANNEL SELECTED
(3) LAST BIT OF THE 64KB/S CHANNEL SELECTED
(4) SEVEN FIRST BITS OF THE 64KB/S CHANNEL SELECTED
(5) TO INSURE THE EXCHANGING OF MESSAGES WITH THE OTHERS ST5451 PERIPHERAL DEVICES THE MASTER DEVICE USES THE C/I' AND M' CHANNELS ON DIN PIN FOR THE OUTPUT SERIAL DATA DOUT PIN FOR THE INPUT SERIAL DATA
(6) ONLY THROUGH THE ACCESS PROCEDURE

THIS TABLE SHOWS THE USED CHANNELS ACCORDING TO THE CONFIGURATION OF THE CF REGISTER AND THE PINS USED (DIN, DOUT) WHERE THE RECEIVERS RX AND THE TRANSMITTERS TX GET OR PUT THE DATA

M98ST5451-31

SGS-THOMSON MICROELECTRONICS

3 - REGISTER DESCRIPTION

For all the register pictures MSB is on the left and LSB on the right
If not otherwise stated bit are considered active at 1.

FIFOS

RFIFO (read), XFIFO (write).

The address range of the two FIFOs are identical. All the 32 addresses give access to the "current" FIFO location.

When the closing Flag of a receive frame is detected, a status byte is available in the RFIFO. This byte has the following format:

RBC	RDO	CRC	RAB	0	0	0	0

RBC Receive Byte Count.
The length of the received frame is n time 8 bits (n=3,4,5,...)

RDO Receive Data Overflow
A part of the frame has not been lost because the receive FIFO was full

CRC CRC Check
The received CRC bytes were not correct

RAB Receive Abort
The received frame was not aborted

A status byte equal to D0H indicates a correctly received frame

ISTA0 Interrupt Status Register 0
After RESET 10H

RME	RPF	RFO	XPR	XDU	EXI2	EXI1	0

RME Receive Message End
One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes is stored in the RFIFO.

RPF Receive Pool Full
32 bytes of a frame are in RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow
A complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready
One data block (32 bytes max) may be entered into the XFIFO.

XDU Transmit Data Underrun
A transmitted frame was terminated with an abort sequence because no data were available for transmission in XFIFO and no XME command was issued. It is not possible to transmit frame when that interrupt remains unacknowledged and XRES has not been set.

EXI2 Extended Interrupt 2
The interrupt reason is indicated in register ISTA2

EXI1 Extented Interrupt1
The interrupt reason is indicated in register ISTA1.

ISTA1 Interrupt Status Register 1
After RESET 01H
(GCI mode only)

0	0	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1

CIC1 Comman/Indicate Change
A change in the value of CIR1 is detected

EOM1 End of Message 1 (monitor channel)
MON1 has received an end of message.

XAB1 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON1 has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register 1 ready
A byte has been received in register MONR1.

RAB1 Receive Abort
MON1 received an ABORT from the remote receiver.

XMR1 Transmit Monitor Register 1 ready
A byte can be stored in register MONX1

ISTA2 Interrupt Status Register 2
After RESET 01H
(GCI and TE mode only)

0	0	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

CIC2 Command/Indicate Change
A change in the value of CIR2 is detected.

EOM2 End of Message 2 (monitor channel)
MON2 has received an end of message.

XAB2 Monitor Transmit ABORT
The received byte has not been detected in two successive frames.
MON2 has sent an ABORT (A bit) to the remote transmitter.

RMR2 Receive Monitor Register 2 ready
A byte has been received in register MONR2.

RAB2 Receive ABORT
MON2 received an ABORT from the remote receiver.

XMR2 Transmit Monitor Register 2 ready
A byte can be stored in register MONX2.

MASK0, MASK1, MASK2
After Reset FF; the three mask registers MASK0, MASK1, MASK2 are associated respectively to the three interrupt registers ISTA0, ISTA1,and ISTA2.
Each interrupt source in ISTA registers can be selectively masked by setting to "1" the corresponding bit in MASK1. Interrupt sources (masked or not) are indicated when ISTA is read by the microprocessor. When an interrupt source is not masked, $\overline{INT}$ goes low.

STAR Status Register
After Reset 48H

XDOV	XFW	IDLE	RLA	DCIO	0	0	0

XDOV Transmit Data Overflow
More than 32 bytes have been written into the XFIFO.

XFW XFIFO Write enable
Data can be entered into the XFIFO.

IDLE IDLE State
15 or more consecutive ones have been detected on the input data line.

RLA Receive Line Active
Frames or interframe flags are being received

DCIO D and C/I Channels are occupied

CMDR Command Register
After Reset 00

XHF	XME	RMC	RMD	RHR	XRES	M2RES	M1RES

XHF HDLC frame transmission can start.

XME Transmit Message End
The last part of the frame was entered in XFIFO and can be sent.

RMC Receive Message Complete
Reaction to RPF or RME interrupt. The received frame (or one pool of data) has been read and the corresponding RFIFO is free.

RMD Receive Message Delete
Reaction to RPF or RME interrupt. The entire frame will be ignored. The part of frame already stored is deleted.

RHR Reset HDLC receiver

XRES Reset HDLC transmitter
XFIFO is cleared and the transmitted frame (if any) is aborted.

M2RES Monitor 2 Reset
Reset MONITOR and C/I channels (TX and RX).

M1RES Monitor 1 Reset
Reset MONITOR and C/I channels (TX and RX).

* For the four first bits (XHF, XME, RMC, RMD), the reset is done by the device; the other bits level sensitive

MODE HDLC Mode Register
After Reset 00

DMA	FL1	FL0	ITF	RAC	CAC	NHF	FLA

DMA DMA Interface activation

FL1/0 Frame Length
Minimum frame length accepted

	FL1	FL0
3 bytes	0	0
4 bytes	0	1
5 bytes	1	0
6 bytes	1	1

ITF InterframeTime Fill
ITF= 1 : Flags are transmitted
ITF= 0 : IDLE is transmitted

RAC RAC= 1 : Activate RX
RAC= 0 : deactivate RX

CAC Channel Activation
CAC = 1 : Activate RX and TX
CAC = 0 : deactivate RX and TX

NHF HDLC Function Select
NHF = 1 : disable HDLC function

FLA Flag
FLA = 1 : transmit shared flags
FLA = 0 : transmit two flags between consecutive frames.

RFBC Receive Frame Byte Counter
After reset 00

RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC 0/7 Receive Data Count

Total number of bytes of received frame without CRC.

RDC 0/4 Indicate the number of bytes in the current block available in RFIFO.

RDC 5/7 Indicate the number of 32 bytes blocks received. If the frame exceeds 223 bytes, RDC 5/7 hold the value "111", only RDC 4/0 continue to count modulo 32.

See Table 3.

The contents of the register are valid after an RME interrupt. The µP must read N+1 bytes to transfer the number of bytes received and the status byte into the memory.

CIX1 Command/Indicate Transmit Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Code to be transmitted permanently in the outgoing GCI C/I channel.

CIR1 Command/Indicate Receive Register 1
After reset FFH
(GCI only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4:

Incoming GCI C/I channel.

MONX1 Monitor Transmit Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value written in MONX1 is transmitted in the outgoing Monitor channel according to GCI transfer protocol. XMR1 interrupt indicates when MONX1 is again available.

MONR1 Monitor Receive Register 1
After reset FFH
(GCI only)

M1	M2	M3	M4	M5	M6	M7	M8

The value read from MONR1 gives the value of the byte received in the monitor channel according to GCI transfer protocol. RMR1 interrupt indicates when a new byte is available in MONR1 register.

CIX2 Command/Indicate Transmit Register 2
After Reset FFH
(GCI and TE mode only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 Code transmitted permanently in the 2nd GCI C/I channel.

CIR2 Command/Indicate Receive Register 2
After reset FFH
(GCI and TE mode selected only)

1	1	P1	P2	P3	P4	P5	P6

P1/P6 The contents of the 2nd C/I channel; they are the different requests received from TE peripheral devices to µP.
Six peripherals can make a simultaneous request.

MONX2 Monitor Transmit Register 2
After reset FFH
(GCI and TE mode only)
The value written in MONX2 is transmitted in the 2nd GCI M channel to a peripheral (if PI= 1; register CF).

TABLE 3

N (number of bytes in the frame received without CRC)	Counter 765	Counter 43210	n (number of 32 bytes blocks received)
N	n	m	n
1 Min	000	00001	0
2	000	00010	0
3	000	00011	0
30	000	11110	0
31	000	11111	0
32	001	00000	1
33	001	00001	1
62	001	11110	1
63	001	11111	1
64	010	00000	2
222	110	11110	6
223	110	11111	6
224	111	11111	7
256	111	00000	7
257	111	00001	7
-	111	-	7

MONR2 Monitor Receive Register 2
After reset FFH
(GCI and TE mode only)
The value read from MONR2 gives the value of the byte received from M channel in 2nd GCI channel.

TSR Time Slot Register
After reset 00

TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

In GCI mode (MDS1= 1 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2 indicates B1 or B2
TSR4/7 indicate position of GCI channel
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR4/7 indicate position of GCI and its D channel

In Multiplexed Mode
(MDS1=0 in CF Register)
a) CCS=1 in CF Reg. (64 Kbit/s)
Then: TSR2/7 indicate channel position in the 64 time slots multiplex
b) CCS=0 in CF Reg. (16 Kbit/s)
Then: TSR0/7 indicate channel position in the 256 time slots multiplex.

CA Configurationn Register A
After reset 00

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA0	SAPI 0 is recognized	CA0 = 1
CA1	SAPI 63	CA1 = 1
CA2	SAPI x	CA2 = 1
CA3	SAPI y	CA3 = 1
CA4	TEI 127	CA4 = 1
CA5	TEI z	CA5 = 1
CA6	TEI t	CA6 = 1
CA7	Address filter active	CA7 = 1

CB Configuration register B
After reset 00
Content of CB indicate SAPI x value
High Order 6 Bits

SAPI	0	0

CC Configuration Register C
After reset 00
Content of CC indicate SAPI y value
High Order 6 Bits

SAPI	0	0

CD Configuration Register D
After reset 00
Content of CD indicate TEI z value.

7 High Order Bits

TEI	0

CE Configuration Register E
After reset 00
Content of CE indicate TEI t value.

7 High Order Bits

TEI	0

CF Configuration Register F
After 00

TE	MAS/SSC	CCS	CMS/SC	PI	VZDOUT	MDS1	MDS0

TE TE mode
TE = 1 : the frame is constitued by three GCI channels (GCI-SCIT)

MAS/SSC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16 Kbit/s)
MAS/SSc is MAS and:
MAS = 0 means "Slave device"
MAS = 1 means "Master device"

If SC = 1 (i.e. a sub-channel is selected) MAS/SSC is SSC; if 16Kb is selected SSC chooses between first on second bit of the stream while, if 64Kb is selected SSC chooses between first or last seven bits of the stream (see TABLE 2 and CMS/SC)

CCS Channel Capacity Selection
CCS = 1: 64 Kb/s
CCS = 0: 16 Kb/s.

CMS/SC If CCS = 0, TE = 1, MDS0 and MDS1 = 1 (i.e. GCI mode, TE mode, 16Kbit/s)
CMS/SC is CMS (Contention mode selection) and:
CMS = 1 means "D and C/I channel access procedure active"
CMS = 0 means "D and C/Z channel access procedure active"

If CCS = 1 and TE = 1 CMS/SC is SC (Subchannel) and:
SC = 0 means "16Kbit/s or 64Kbit/s is used"
SC = 1 means "an 8Kbit/s or 56Kbit/s subchannel inside a 16Kbit/s or 64kbit/s is used" (see MAS/SSC)

PI Peripheral Interface (only if TE=1)
PI = 1: CIX2, CIR2, MONX2, MONR2, active

VZDOUT When level 1 device is inactive (i.e. CIR1 = DI = 1111) and GCI has to be waken up (i.e. TIM = 0000 in CIX1), DOUT is set to zero requiring FS and CLK if VZ DOUT=1.

MDS1 Mode Bit 1
MDS1 = 1:GCI mode
MDS1 = 0: Multiplexed mode

MDS0 Mode Bit 0
MDS0 = 1: Multiplexer and Demultiplexer are active.
MDS=0 No multiplexer.

CCR Configuration Register 00
After reset 00

TLP	ADDR	AD3	AD2	AD1	AD0	CRS	TRI

TLP Test Loop
TLP = 1: The transmitter is internally connected to the receiver; the transmit output is not activated. The digital interface must be activated to provide the bit clock and frame Synchro.

ADDR Address Recognized
If TE = 1 and PI = 1
ADDR = 1: The first byte received in MONR2 is compared with AD0/3. If equal the message is accepted, otherwise is ignored.
ADDR = 0: The message is always accepted.

AD0/3 When PI = 1, is the component address.

AD0/2 Address bit used to access D and C/I channels (TE = CMS =1, CCS = 0).

CRS Clock Rate Selection
CRS = 1: Clock frequency is twice the data rate (GCI).
CRS = 0: Clock frequency and data rate are identical.

TRI Tristate
TRI = 1: DOUT in tristate
TRI = 0: DOUT in open drain.

4 - WORKING PROCEDURES

4 - 1 - RECEIVE FRAME

Recognized frame (by means of SAPI and/or TEI identification), having a minimum length is stored in the RFIFO with all bytes between the opening flag and CRC field.

When the frame is less than or equal to 32 bytes, is transferred in one block, and just after the receiving completion interrupt (RME), a status byte is appended at the end. The frame and its status byte remain stored until µP acknowledgement (RMC).

When the frame is longer than 32 bytes, blocks of 32 bytes plus one remainder block of lenght 1 to 32 are transferred to the microprocessor. The receiving 32 byte block generates a RPF interrupt and the data in RFIFO remains valid until µP acknowledgement (RMC).

The µP can ignore a received frame by meaning RMD (Receive Memory Delete), reaction to RPF or RME. The part of frame already stored is deleted and the remainder frame is ignored by the HDLC Controller.

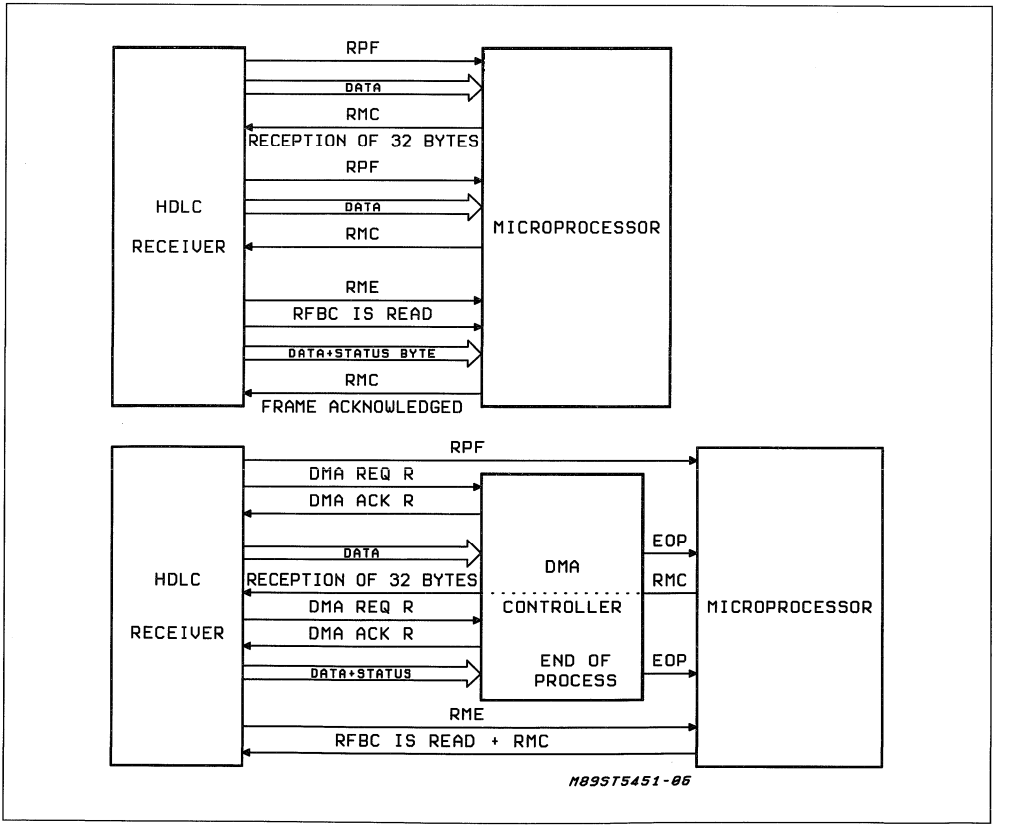
The last block of the frame generates the RME interrupt.

RFBC register bits 0 to 4 indicate the number of bytes currently stored in the RFIFO. Bits 5 to 7 indicate the total number of 32 byte blocks already received. Bits 5 to 7 do not overflow. When the counter status 7 has been reached, it indicates a frame length greater than 223 bytes (see Table 3).

RFBC register is valid only after the RME interrupt and remains valid until RMC acknowledgement by µP.
At each read access by the µP, RFBC 5/7 bits remain unchanged, RFBC 0/4 bits are decreased to reach value 0 when the whole block is read.

Interrupts are queued inside the device. They are sent one by one to the microprocessor after each acknowledgement RMC. If a frame is lost because the RFIFO was full, a RFO interrupt is generated.

Figure 1: Receiving of an HDCL frame



4- 2 - TRANSMIT FRAME

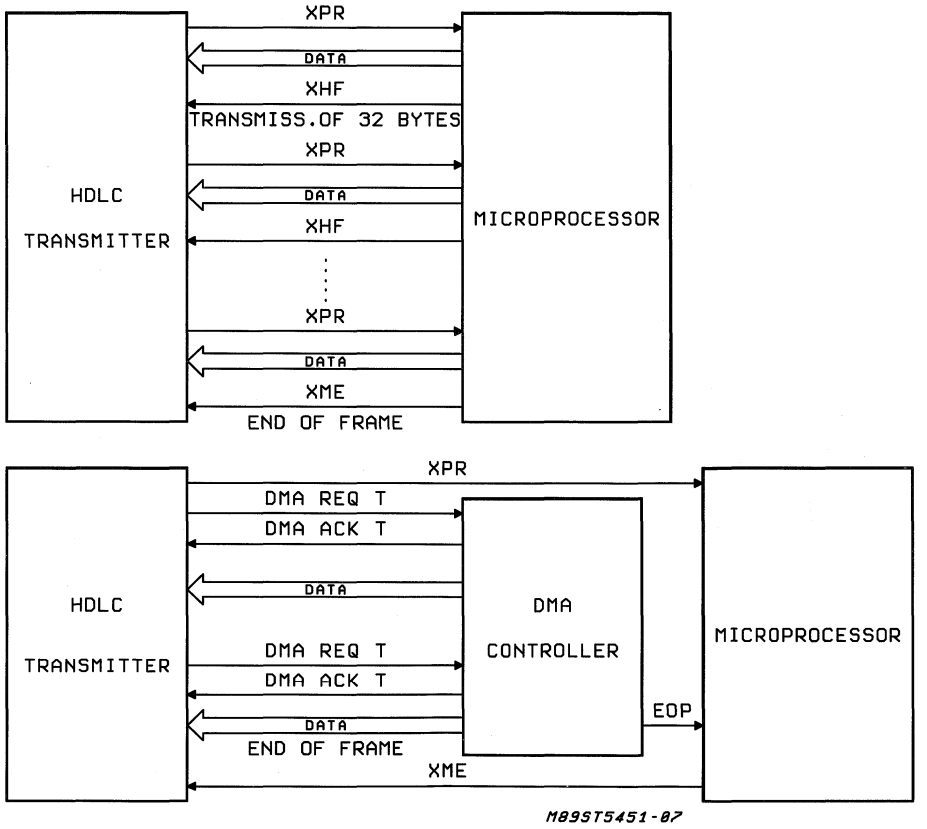
After polling bit XFW or after a XPR interrupt, up to 32 bytes may be stored in XFIFO. Transmission begins after that XHF command is issued by µP. ST5451 will request another data block by an XPR interrupt if the XFIFO contains less than 32 bytes.

When XME is set, all remaining XFIFO bytes are transmitted, the CRC field and the closing flag are added. The HDLC controller then generates a new XPR interrupt.

If the XFIFO becomes empty while XME command has not been set, an abort sequence is generated, followed by interframe time fill and XDU interrupt is generated.

A frame may be aborted by XRES command as well.

Figure 2: Transmission of an HDCL frame



4 - 3 - COMMAND/INDICATE PROCEDURE

The exchange of information in the C/I channel runs as follows:
The two circuits (i.e. ST5421 and ST5451) connected on the GCI interface send one each other a permanent four bit command code in C/I field.

RECEIVE C/I

The ST5451 stores on every frame the four bits of C/I channel coming from level 1 circuit in a first register CIR. This value is compared with the previous one. If a one new appears during two consecutive frames, this new value is loaded in register CIR1 and a CIC1 interrupt is generated.

TRANSMIT C/I

The transmit register CIX1 can be written at any time by the µP. Its content is continuously sent in the C/I channel.

Note: The TIM command (0000) forces a low level on DOUT, if CIR1 = DI (1111) when VZ DOUT = 1 to require FS and CLK.

4 - 4 - MONITOR CHANNEL

The GCI Monitor channel procedure allows full duplex data transmission with acknowledgement using A bit.

MESSAGE RECEIVING

An interrupt (bit RMR1 in ISTA1 register) is generated when a new byte is available in register MONR1.
ST5451 generates an interrupt bit (XAB1 in ISTA1) if it does not read twice the same bytes meanwhile sending an ABORT to the remote transmitter.
It performs an interrupt (EOM in ISTA1) also when it has received an End Of Message. Acknowledgement to remote transmitter is sent if:
- the byte was received twice with the same value
- the microprocessor reads the previous byte stored in register MONR1.
This procedure performs flow control between S interface device and µP.

MESSAGE TRANSMISSION

ST5451generates an interrupt (XMR1 in ISTA1) when register MONX1 is available.
Writing register MONX1/0 generates a message transmission. When the last byte is stored in the register MONX1/1, ST5451 sends the End of Message to remote receiver. If an Abort is received, one interrupt (RAB1) is generated.

4 - 5 - M' and C/I' CHANNELS

The procedure allows a full duplex data transmission between microprocessor and the peripheral devices connected on C/I' local and M' channel through GCI-SCIT channel 1.
Receive Interrupt on C/I' (DOUT is an input).
A new value on C/I' indicates to ST5451 master that one device in the terminal wants to send a message. Up to six peripherals may generate such an interrupt to the microprocessor.
ST5451 writes at every frame the six bits of C/I' channel coming from peripherals in register CIR'.
This value is compared with the previous one and if a new one appears during two consecutive frames, is loaded in register CIR2 and CIC2 interrupt (ISTA2 register) is generated.
µP may send a message on M' channel (DIN becomes an output) to allow the peripheral device to transmit.

MESSAGE TRANSMISSION ON M' CHANNEL

ST5451 sets interrupt XMR2 (ISTA2 register) if register MONX2/0 is available. Writing MONX2/0 generates a message transmission. When the last byte is stored in register MONX2/1, ST5451sends End of Message to remote peripheral.
If an ABORT is received, interrupt RAB2 (ISTA2 register) is issued. Then microprocessor may send its message again.

MESSAGE RECEPTION ON M' CHANNEL

Interrupt bit RMR2 (ISTA2 register) is generated when a new byte is available in MONR2 register.
ST5451 sets interrupt bit XAB2 (ISTA2 register) if it does not read twice the same byte; in this case, it sends an ABORT to remote peripheral.
The controller generates interrupt bit EOM2 (ISTA2 register) when End Of Message is received.

4 - 6 - ACCESS PROCEDURE TO D AND C/I CHANNELS (GCI and TE mode selected only)

Up to eight HDLC controllers may be connected to D channel and C/I channel. A contention resolution mechanism is used if bit CMS (Contention Mode Selection) is set.
The mechanism allows to give an access without losing data.
An access request may be generated, if CIX1 (Command/Indicate Register 1) contains a different code from DI (1111). During the procedure, M channel (with A and E bits) may be used. On input DIN, the GCI controller checks the CMS4 bit (CMS channel - Third GCI channel) (see Fig. 4).
CMS4 indicates the status of C/I and D channels CMS4= 1 "channels free"; CMS4= 0 channels occupied.
If the channels are free, the HDLC controller starts transmitting its individual address AD2 on CMS1, AD1 on CMS2, AD0 on CMS3. If an erroneous address is detected, the procedure is terminated immediately. If the complete address can be read without error, the D and C/I channels are occupied: the ST5451 transmits CMS4 = 0: The HDLC controller which has the lowest address has priority over the others.
The access request is withdrawn if the HDLC controller transmits code DI = 1111. the CMS4 bit (CMS field) is set.

Figure 3: GCI-SCIT Frame Timing

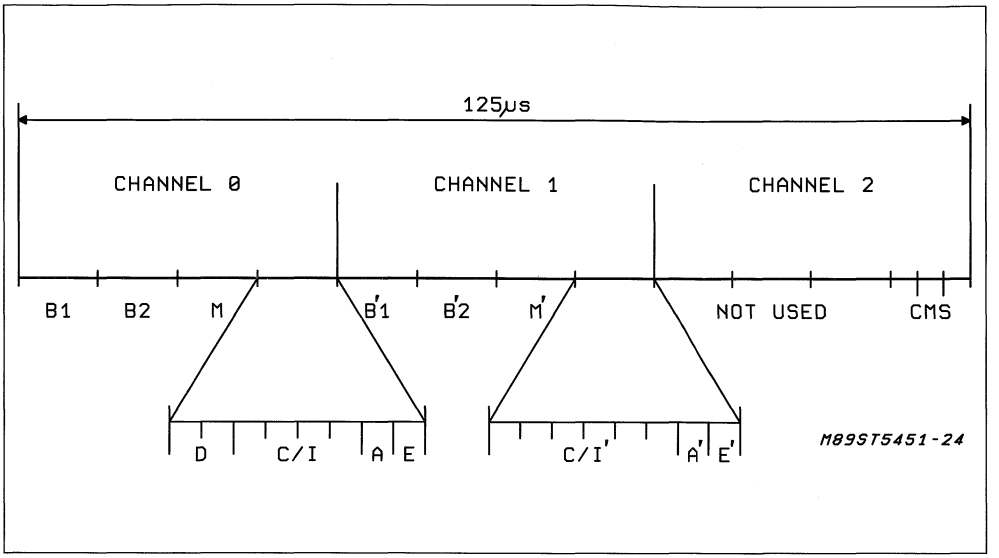
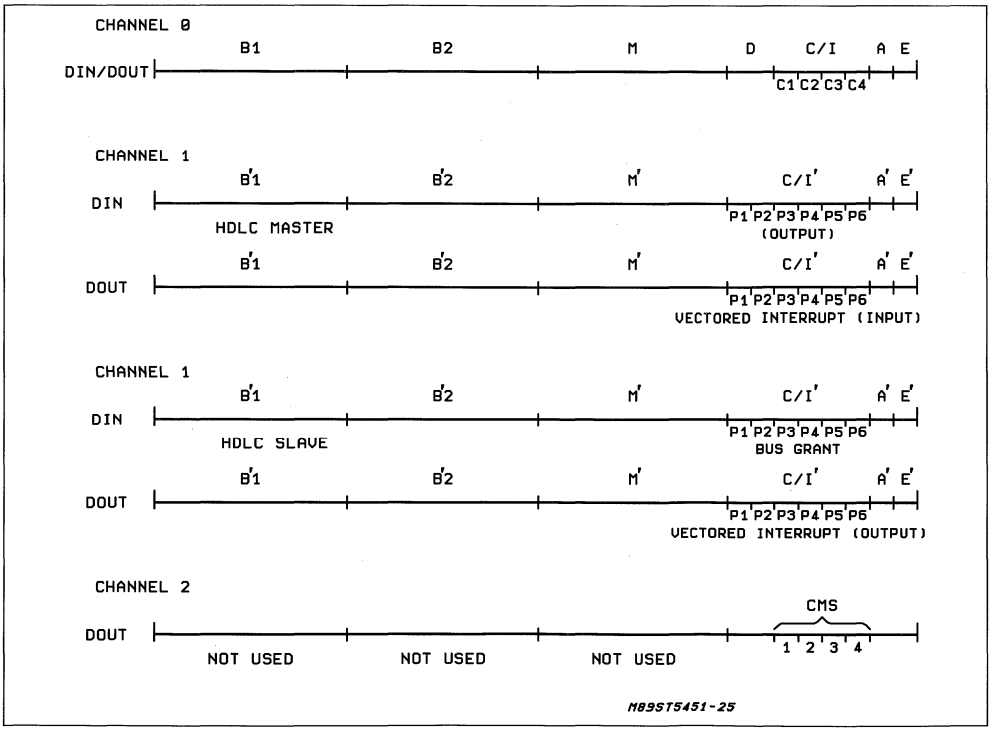


Figure 4: GCI-SCIT Channels Timing



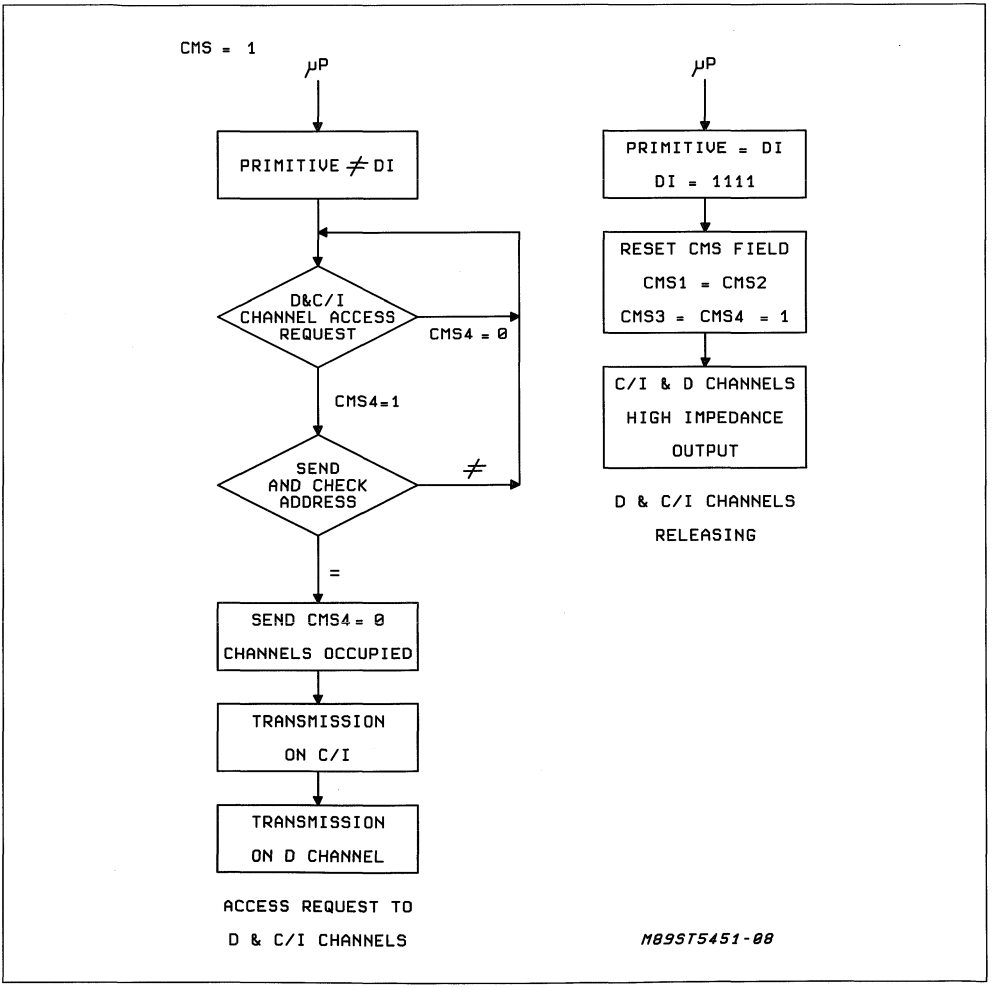
4 - 7 - DMA ACCESS

The HDLC controller has a DMA interface which is activated by DMA bit in MODE register.The DMA interface is available only when multiplexed bus is selected.
ST 5451 asserts DMA REQR or DMA REQX to request an exchange of bytes between the FIFOS and the external memory.
The external DMA controller asserts DMA ACKR or DMA ACKX to access the FIFOS.
These signals are equivalent to E/DS/RD functions.
During DMA access, CS/CE pin must be inactive; AS and E/DS/RD signals can be present.
Outside DMA Access, all registers are accessible by the µP except the FIFOS.

FRAME RECEPTION:
When one block has been stored in RFIFO, DMA REQ R pin goes low and RPF (or RME) interrupts the µP. The DMA controller reads the RFIFO. After the RME interrupt, the frame length will be available in RFBC register. The block is acknowledged by RMC command.

FRAME TRANSMISSION:
When a 32 byte block is free in XFIFO, DMA request goes low and XPR interrupts the µP. The DMA controller can write data in the XFIFO. At the end of the frame, the µP send XME to HDLC controller; CRC and closing flag will be sent by the HDLC controller.

Figure 5: D and C/I channels Access Procedure



4 - 8 - INTERRUPT PROCEDURE

4 - 8 - 1 - HDLC CHANNELS

4 - 8 - 1 - 1 - RECEIVE DIRECTION

RRE and RPF interrupts

RPF bit (register ISTA0) set high to indicate the HDLC controller has received a block of 32 bytes which is not a complete message.

This bit remains high until it is erased by the microprocessor.

As for each bit of ISTA0 register, except the extension bits of ISTA1 and ISTA2 (EXI1, EXI2), the way to erase RPF is to write a "0" at its location and to write a "1" at the location of the others (for example 7FH into ISTA0 to erase RME). The processing order is:

- put Mask0 on ISTA0 (if Mask Off)
- (Read FIFOR) X 32
- Write ISTA0 to erase RPF (BFH)
- Write RMC to "1" for asking for another block of the frame
  (NB: RMC, RMD are automatically erased by the controller)
- Remove Mask0

RME bit (register ISTA0) set high to indicate the HDLC controller has received a short frame or the last block of a large frame. The message is now complete, the bit remains high until it is erased by the microprocessor. The processing order is:

- put Mask0 on ISTA0 (if upper level Mask Off)
- Read RFBC with a mask on the 3 most significant bits, to know the number "N" of transfers to do
- (Read FIFOR) x N for data
- Read FIFOR for status on the frame
- Write ISTA0 to erase RME (7FH)
- Write RMC or RMD to "1" for asking for another frame.

RF0 interrupts

RF0 is a bit of the interrupt register ISTA0 set high to indicate an overflow of the receive FIFO has been detected, either because more than 8 frames cannot be stored or because more than 64 bytes can't be stored. This information is also stored into the status of the concerned frame (RDO).

The processing order of the microprocessor is:

- Looking for RPF and RME bits and pop - up the frames. Then look for the status and throw down the frame concerned. In general case, only one frame is lost.

4 - 8 - 1 - 2 - TRANSMIT DIRECTION

XPR Interrupt

XPR is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has a free block of 32 bytes. This bit remains high until the microprocessor write a byte into the block and erase this bit into ISTA0; if another block is free, XPR get high again immediately.

The processing order of the microprocessor is in non DMA Mode:

- Put Mask0 on ISTA0 (if upper level Mask Off)
- Write at least one byte into FIFOX
- Write ISTA0 to erase XPR
- Write XHF to "1" for launching the transmit operation of block (a block is not necessarily 32 bytes)
  or write XME to "1" for launching the transmit of a short frame or of the last part of a frame
- Remove masks

In DMA Mode two general cases are possible:

1) The external DMA controller works by "pages" less or equal to 32 bytes. The "process" of the DMAC is a short frame transmission and the processor must give an XME at the end of the DMAC process (refer to figure 2).

2) The DMA controller works by "pages" of more than 32 bytes. It's process is the transfer of the whole frame.
The circuit doesn't need an XHF at the end of an intermediate 32 byte block; since it has reached 32 bytes written into the current fifo, it begins the transfer and toggles on the second fifo as soon as the first is full. (At this moment an XME is possible if the 32nd byte was the end of the frame - case 1) and then, a 33rd write operation into the fifo generates an internal XHF and the frame following blocks are expected.

- In the two cases the flow control is done between DMAC and ST5451 by the way of REQX and ACKX signals

The processing order is:

- Put Mask0
- Give order to DMAC to begin transfer
- Wait for DMAC end of process
- Write ISTA to erase on XPR
- Write XME to signal the end of the frame to the ST5451 (otherwise the ST5451 will put "underrun" interrupt, as soon as its two blocks are free).

XDU Interrupt

XDU is a bit of the interrupt register ISTA0 coming high to indicate HDLC controller has detected an underrun (a frame is being transmitted and no more bytes are available into the FIFO).

The HDLC controller finish the frame by transmitting an "Abort" and no more data can be transmitted even in NHF mode. To be sure XDU is seen by the MIcroprocessor, XDU interrupt bit must be erased in ISTA0 in addition of XRES security procedure

The transmit control is frozen and the only way to reinitialize a transmit session is to write an XRES, after erasing XDU.

4 - 8 - 2 - M CHANNELS INTERRUPTS EOM, RMR, XMR, RAB

Receive Direction

RMR 1/2 is a bit of interrupt register ISTA 1/2 coming high to indicate the M (or M') channel controller has received a valid byte on receiving channel (two identical consecutive bytes).

The microprocessor processing order is;

1. Erasing RMR 1/2 interrupt into ISTA 1/2
2. Read MONR 1/2 register.

This order can't be inverted because, as long as MONR isn't read, the receive state machine is locked in wait state, a new byte can't be acknowledged and so, a new interrupt can't be done.

More, if MONR is read first, the receive state machine is ready for receiving a new byte and create another interrupt. So, if the interrupt bit corresponding to the previous frame isn't erased before a new byte arrives, this byte won't be seen (the microprocessor won't be informed) and the controller will be locked waiting for MONR read.

XAB 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an abort (two conscutive bytes not identical) as long as this interrupt isn't erased, the receiver is locked in wait state.

EOM 1/2 is a bit of the interrupt register coming high to indicate the receive controller has detected an end of message. As long as the interrupt isn't erased, the receiver is locked in wait state.

Transmit Direction

XMR 1/2 is a bit of the interrupt register coming high to indicate a byte can be written into MONX. The processing order is:

1. Erasing XMR bit
2. Writing a new byte into MONX.

If this order is inverted, the new byte will be transmitted and a new XMR may be erased before being seen by the microprocessor.

RAB 1/2 is a bit of the interrupt register coming high to indicate the remote receiver has reported an abort detection. The processing order is:

1. Erasing RAB bit
2. Erasing XMR bit
3. Writing a new byte into MONX.

If a write operation of the new byte is done before the RAB erasing, the byte will be lost and the transmitter will stay waiting for it.

4 - 8 - 3 - CI CHANNEL INTERRUPTS

CIC 1/2 is a bit of ISTA 1/2 interrupt register coming high to indicate a valid byte has been detected by the command indicate receive controller, and readable into CIR 1/2 register. The processing order is:

1. Erasing CIC bit
2. Reading CIR register.

If this order is inverted, a next byte may be unseen by the microprocessor. It is recommended to work with "Ping Pong" protocol on CI channels, as non flow control is done.

4 - 9 - SOFTWARE RESET PROCEDURES

4 - 9 - 1 - XRES (Transmit Direction)

XRES is a level sensitive command of CMDR which initialize the transmit process.

- XPR interrupt bit is erased
- XDU interrupt bit is not erased (security procedure)
- All data in FIFOs are lost
- After an XRES, the microprocessor must wait for an XPR before writing new data.

The processing order is:

- Writing a "1" into XRES (CMDR)
- Writing a "0" into XRES (CMDR)
- Read ISTA0 waiting XPR or enable XPR interrupt

4 - 9 - 2 - RHR (Receive Direction)

RHR is a level sensitive command of CMDR, which reinitialize the receive process.

- RME, RPF bits are erased
- RFO bit is erased
- All frames in FIFO R are lost
- If RHR is released (got down) at the time a frame is on line, the HDLC controller waits for a flag.

4 - 9 - 3 - M1RES, M2RES M/CI channels

MRES is a level sensitive command of CMDR which initialize the M/CI channel protocole in both directions.

XMR, RAB, RMR, CIC, XAB, EOM bits are erased by MRES.

After a clock programming (bit CRS), it's necessary to put MRES bit to initialize properly the M protocol.

TYPICAL APPLICATIONS

ST5451 HDLC controller may be used in TE, NT2, NT12 or LT.

Figures 6 to 8 illustrate three typical applications in multifunctional TE.

The D channel containing only signalling is processed by the LAPD controller and routed via a parallel µP interface to the terminal processor. The support of the LAPD protocol which is implemented by the HDLC controller device allows in cost senstive applications the use of a low cost microprocessor. See fig. 6.

Fig. 7 illustrates a configuration in which the D channel containing signalling data (SAPI s) as well as packet switched data (SAPI p) is processed by two controllers and two independent microprocessors.

Fig. 8 illustrates a configuration in which one microprocessor is connected to two controllers via a DMA controller.
D channel with LAPD signalling data and B channel LAPB packet data are processed by the same µP. A DMA controller performs device to memory transfers. It is a typical work station application.

Fig. 9 and 10 illustrate 2 typical applications in NT2 or exchange.

An NT2 or LT in fig.9 with eight D channel controllers connected to the GCI interface handle subscriber 0 to 7. Any GCI compatible transceiver (S or U) may be used to do the subscriber line interface; a GCI compatible exchange circuit may implement the system interface. This is one decentralized application.

Fig. 10 illustrates a centralized application. Using a switching net work, it is possible to connect:

up to thirty two 64 Kbit/s channels on a 2 Mb/s PCM highway to 32 B channel controllers

up to sixty four 64 Kbit/s channels on a 4 Mb/s PCM highway to 64 B channel controllers

up to two hundred fifty six D channels on a 4 Mb/s highway to 256 D channel controllers.

Figure 6: Low cost GCI terminal application

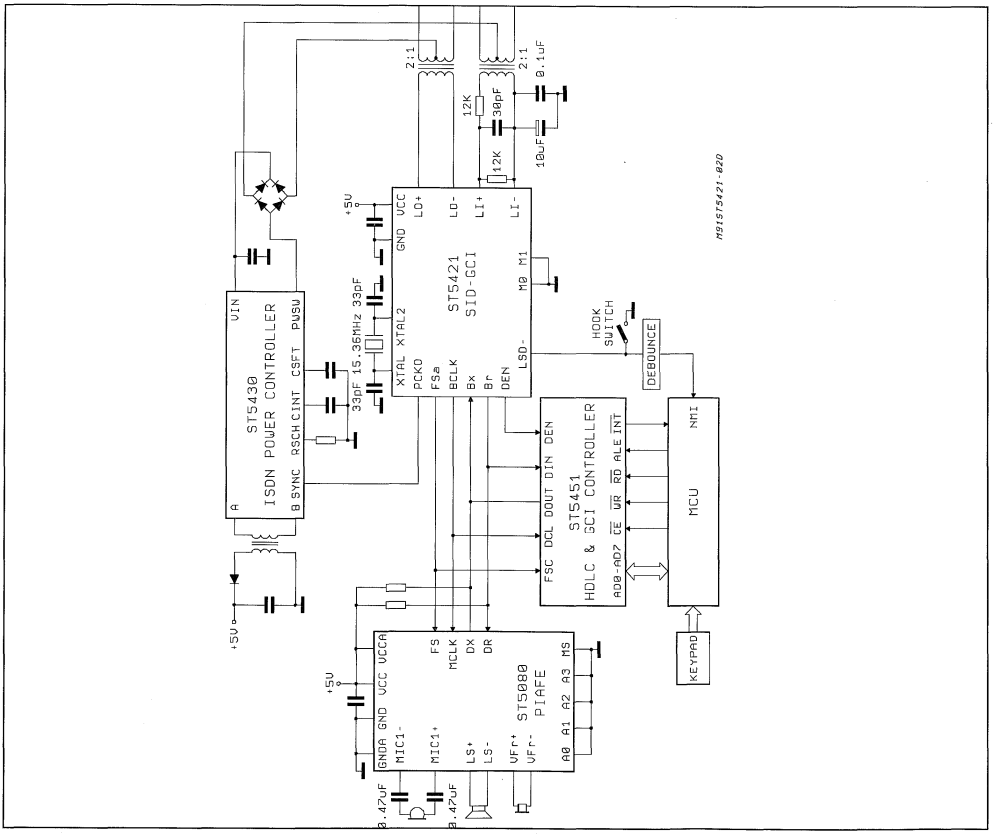


Figure 7: LAPB and LAPD protocol on the same D channel handlended with 2 different µPs

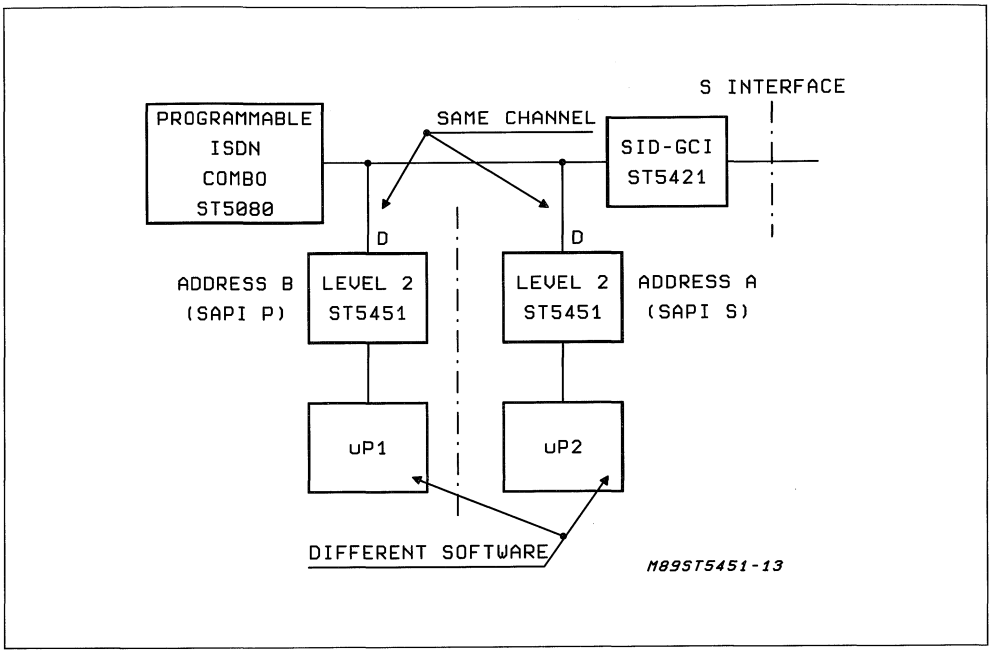


Figure 8: LAPB and LAPD protocol handling an B and D channel

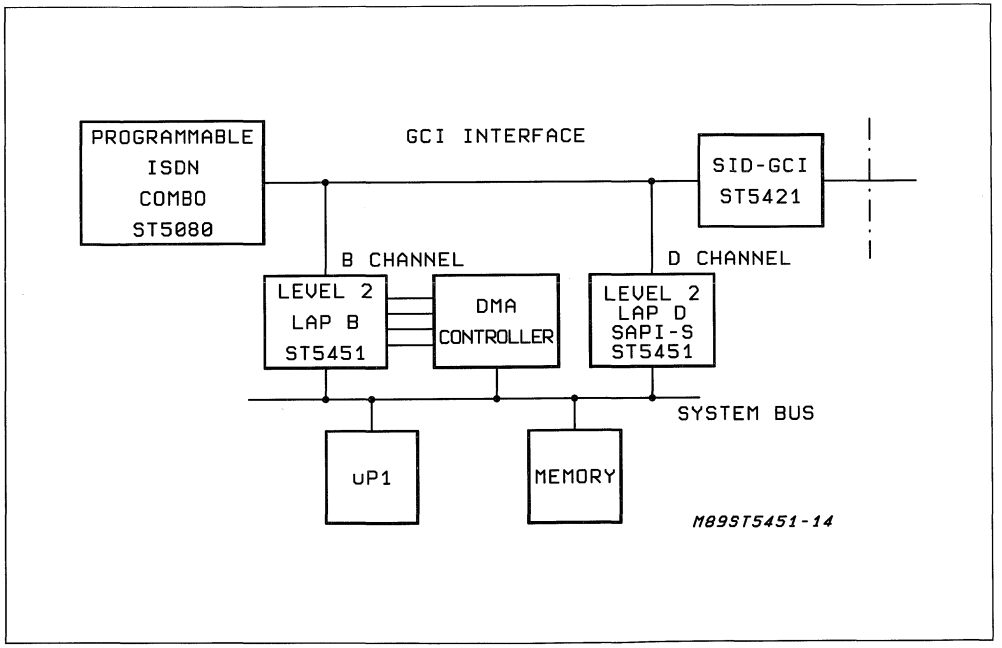


Figure 9: Decentralized D channel handling in NT2 or LT

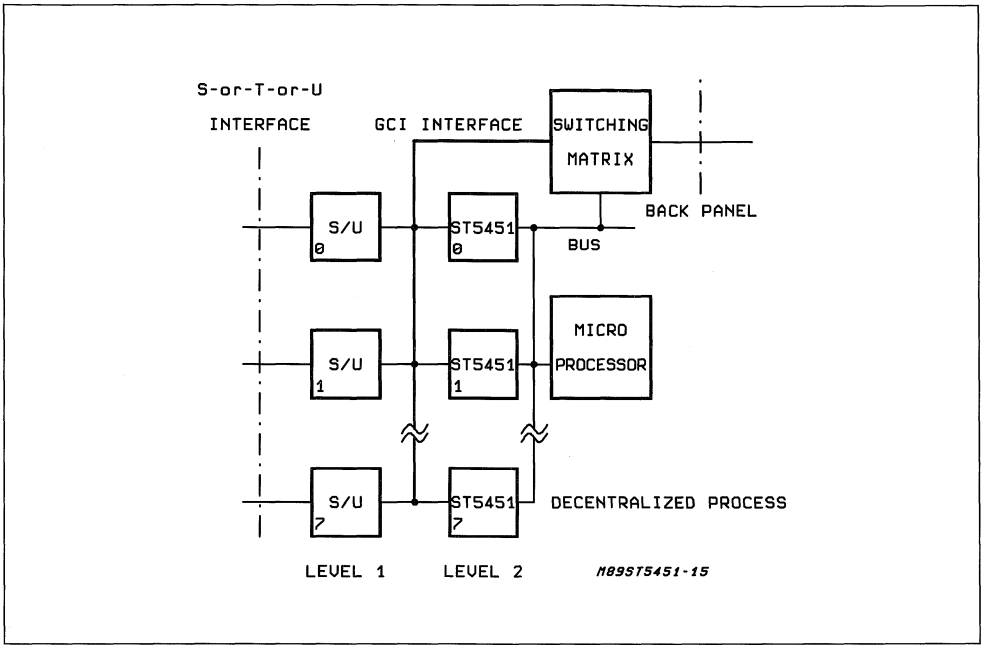


Figure 10: Centralized D channel handling in NT2 or LT

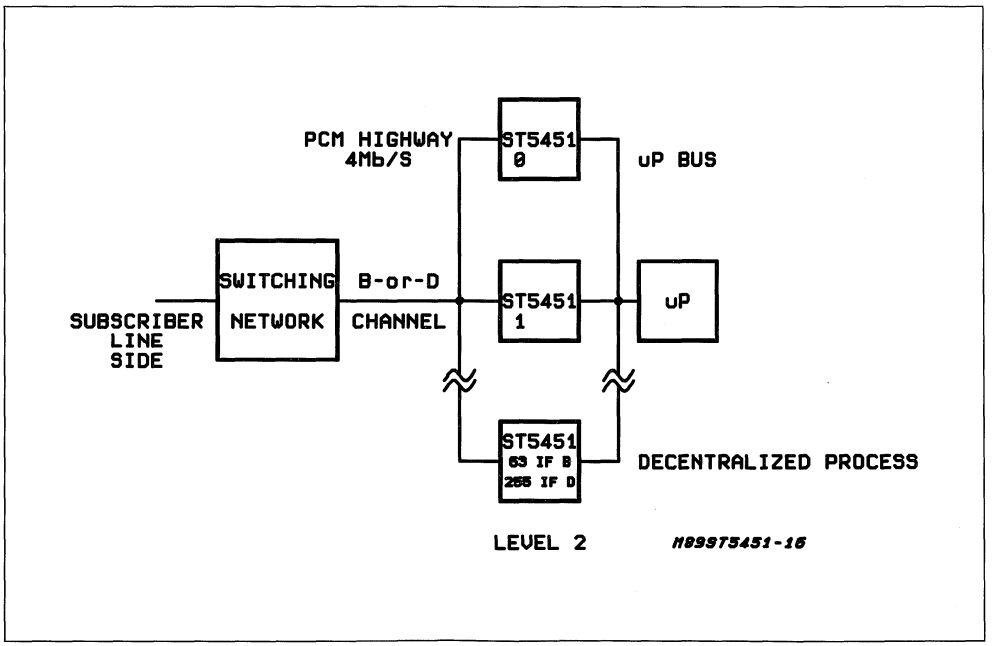


Figure 11: HDCL Frame Transmission Procedure

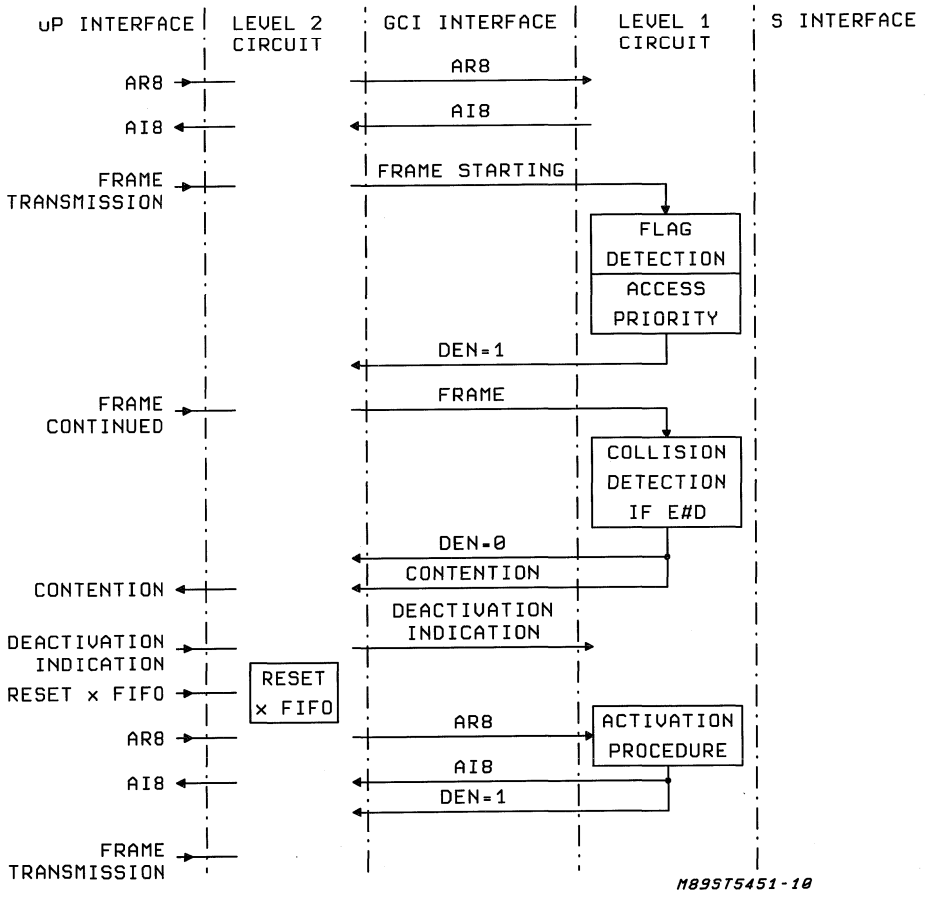


Figure 12: HDCL Frame Transmission Procedure in D Channel

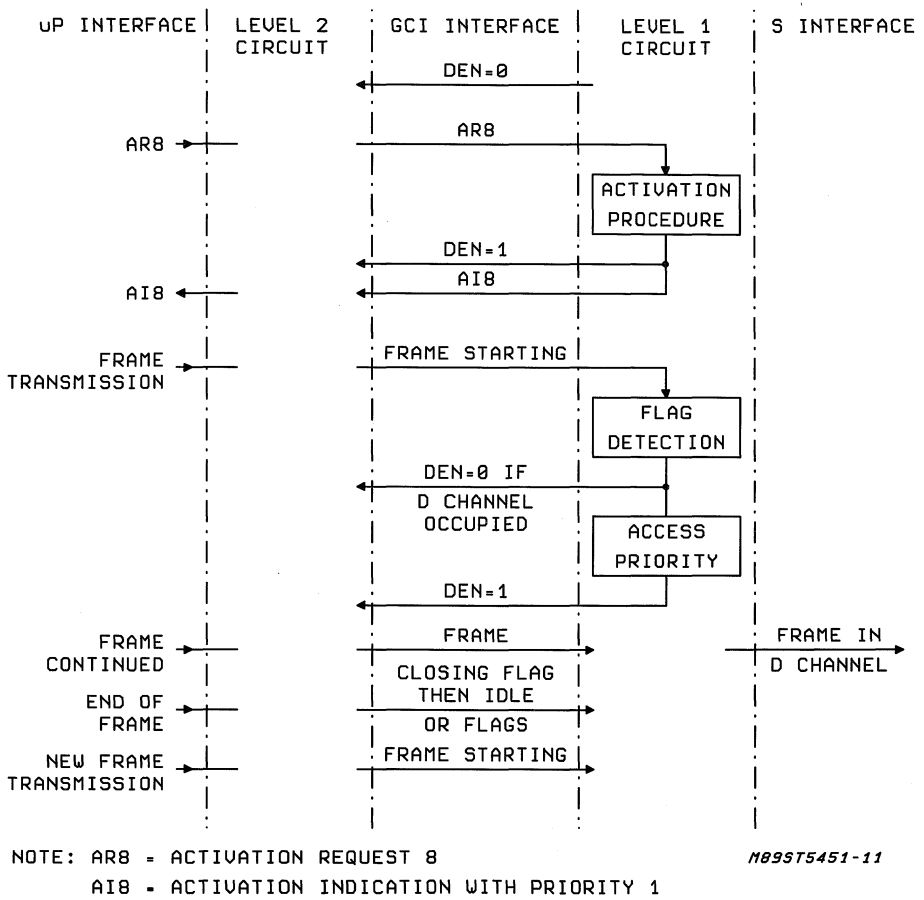
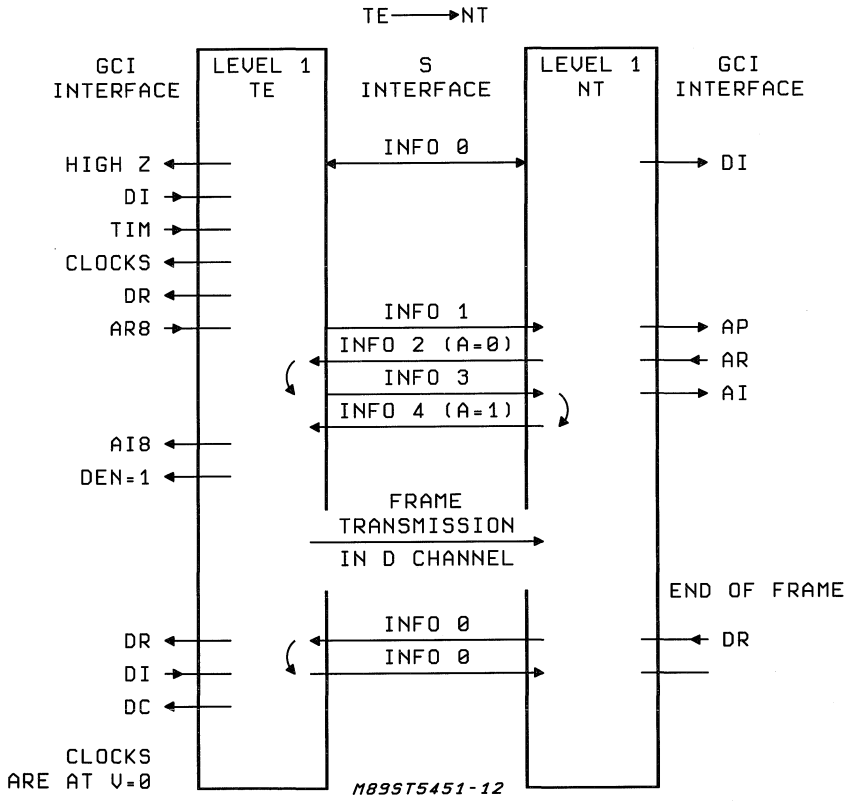


Figure 13: S Activation and Deactivation procedure



STATIC CHARACTERISTICS - GCI INTERFACE (T from 0 to 70°C, V_{DD} = 5 ± 0.25V).

Symbol	Parameter	Condition	Min.	Max.	Unit
VIH	High Level Input Voltage	Maximum leakage current : ± 10 µA	2.4	VDD+0,4	V
VIL	Low Level Input Voltage	Maximum leakage current : ± 10 µA	VSS-0,4	0,8	V
VOH	High Level Output Voltage	IOH = -0,4 µA	2,4		V
VOL	Low Level Output Voltage	IOL = 2mA		0,45	V
VOL	Low Level Output Voltage D_{OUT} . D_{in} . INT	IOL = 7mA		0,45	V
C	Input/Output Capacity			10	pF
C_{OUT}	Load Capacity DIN/DOUT			150	pF
	Load Capacity $\overline{INT}$			150	pF
	Load Capacity AD0/7			100	pF

DYNAMIC ELECTRICAL CHARACTERISTICS - GCI Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	64 x n x FSync $1 \leq n \leq 8$	512		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

DYNAMIC ELECTRICAL CHARACTERISTICS - Double Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	16 x n x FSync $1 \leq n \leq 64$	128		8192	KHz
t_{WCH}	Period of CLK High	50			ns
t_{WCL}	Period of CLK Low	50			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	30			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

ELECTRICAL CHARACTERISTICS - Single Clock Interface

Symbol	Parameter	Min.	Typ.	Max.	Unit
FSync	8 KHz		8		KHz
F_{CLK}	8 x n x FSync $1 \leq n \leq 64$	64		4096	KHz
t_{WCH}	Period of CLK High	80			ns
t_{WCL}	Period of CLK Low	80			ns
t_{RC}	Rise Time of CLK			10	ns
t_{FC}	Full Time of CLK			10	ns
t_{HCF}	Hold Time: CLK - FS	0			ns
t_{SFC}	Set-up Time: FS - CLK	100			ns
t_{DCD}	Delay Time: CLK High to data valid. out: 150 pF			80	ns
t_{DCZ}	Delay Time: to Data Disabled	0		80	ns
t_{DFD}	Delay Time: FSync. High to data valid. count: 150 pF. Applies only if Sync rises later than CLK raising edge.			80	ns
t_{SDC}	Set-up Time: Data valid to CLK receive edge.	30			ns
t_{HDC}	Hold Time: CLK low to data invalid.	30			ns

Figure 14: GCI Timing

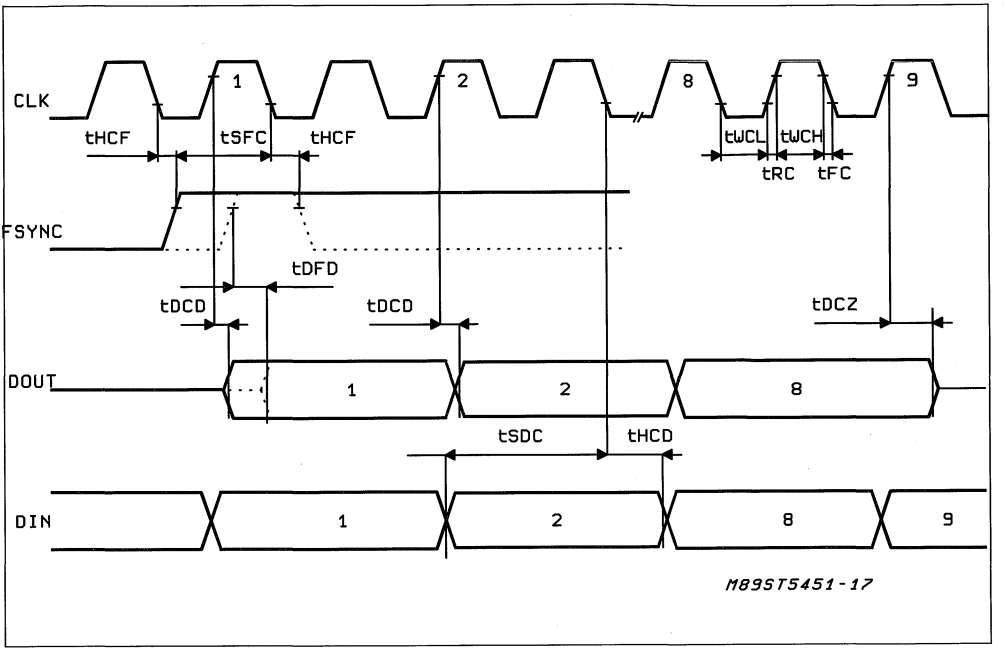


Figure 15: Single Clock Diagram

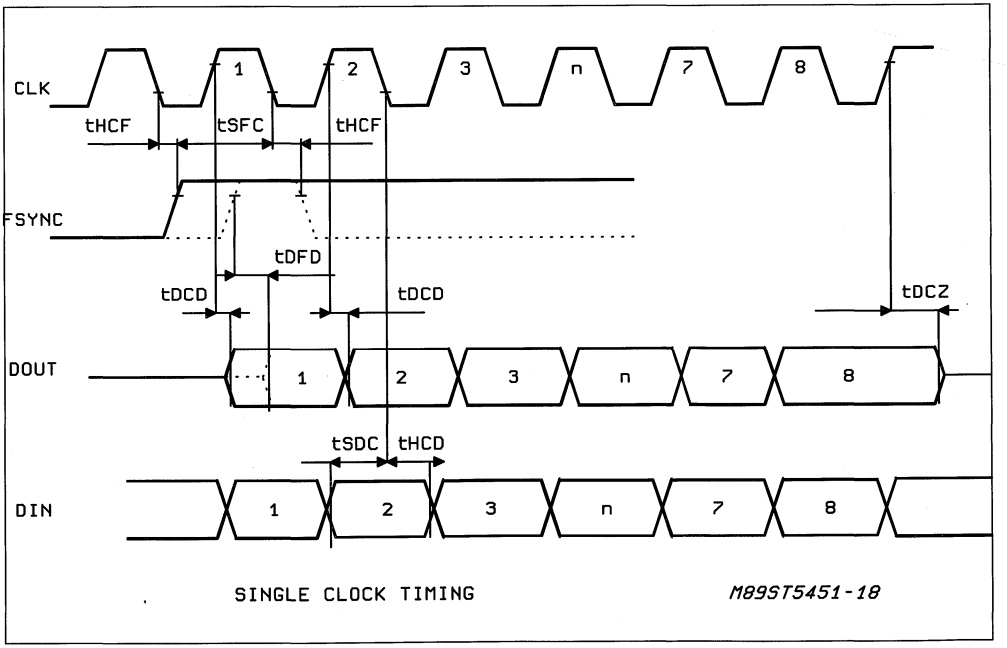
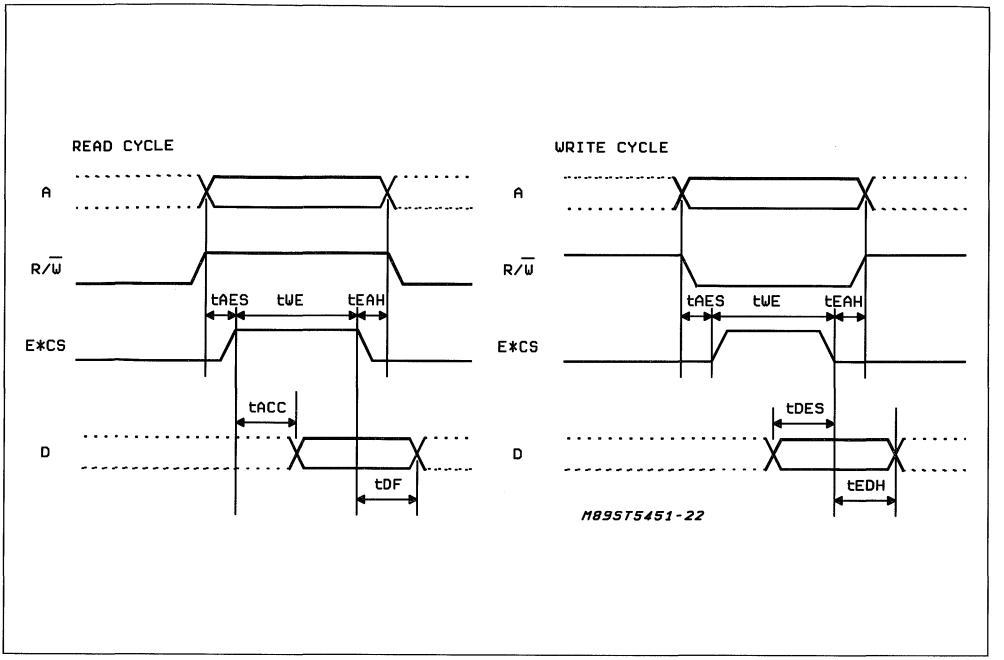


Figure 16: Non-multiplexed µP bus timing



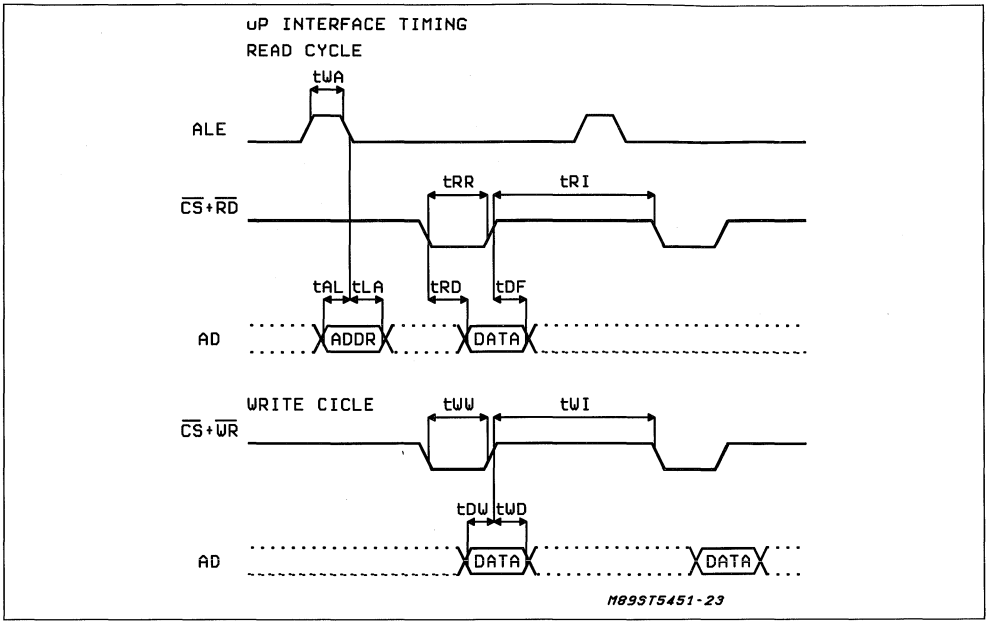
READ CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After E	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. Setup	20		ns
t_{ACC}	Data Delay from E		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WE}	Minimum Width of E	110		ns

WRITE CYCLE (Non-multiplexed mode)

Symbol	Parameter	Min.	Max.	Unit
t_{EAH}	Address Hold After	10		ns
t_{EAH}	R/$\overline{W}$ Hold After E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E.CS Setup	20		ns
t_{DES}	Data to End of E Setup	35		ns
t_{EDH}	End of E.CS to Data hold	10		ns
t_{WE}	Minimum Width of E	60		ns
t_{RW}	Minimum Width of RESET	100		ns

Figure 17: Multiplexed Intel-like µP bus timing



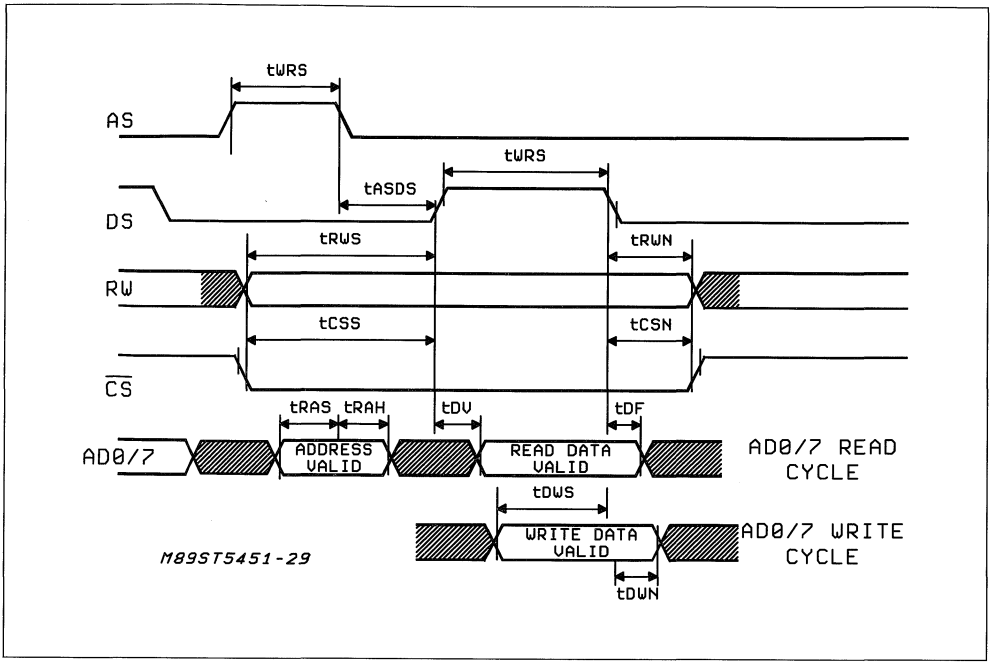
READ CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{LA}	Address Hold After ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		110	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	$\overline{CE}$ to $\overline{RD}$ or $\overline{WR}$ set-up t_{CSS}	20		ns
t_{CSH}	$\overline{CE}$ hold after $\overline{RD}$ to $\overline{WR}$ t_{CSH}	10		ns

WRITE CYCLE (Multiplexed Intel Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{WW}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns

Figure 18: Multiplexed Motorola-like µP bus timing



Symbol	Parameter	Min.	Max.	Unit
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS low to DS high	10		ns
t_{RWS}	RW to DS setup	20		ns
t_{RWH}	RW hold after DS	10		ns
t_{CSS}	CS to DS setup	20		ns
t_{CSH}	CS hold after DS	10		ns
t_{AAS}	Address to AS setup	20		ns
t_{AAH}	Address hold after AS	10		ns

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DV}	Data Valid after DS		110	ns
t_{DF}	Output Flat Delay		25	ns

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit
t_{DWS}	Data to DS setup	35		ns
t_{DWH}	Data Hold after DS	10		ns

DMA BUS TIMING (Reception Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{ACC}	Data Delay from ACKR		110	ns
t_{DF}	Output Float Delay		25	ns
$t_{W\overline{AR}}$	Minimum width $\overline{ACKR}$	110		ns
t_{WAR}	Minimum width ACKR	70		ns
t_{DRAR}	REQR Delay from ACKR		80	ns

Figure 19: DMA frame reception timing

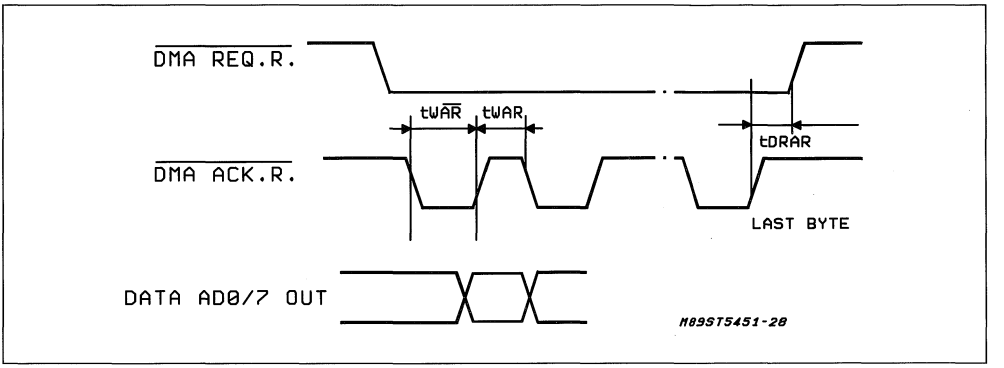
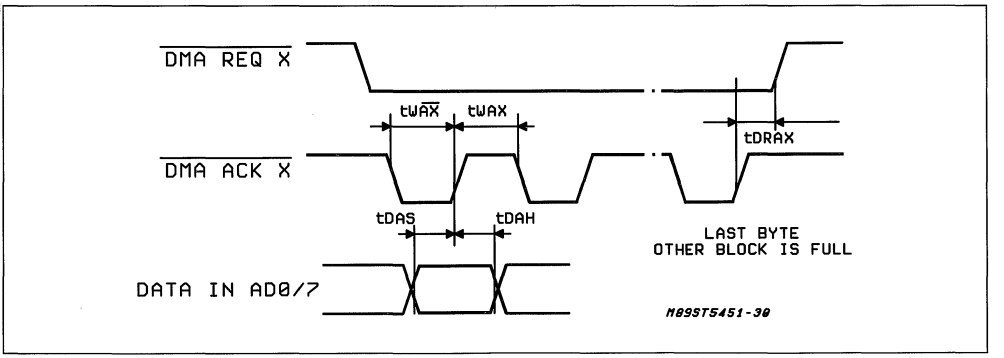


Figure 20: DMA frame transmission timing



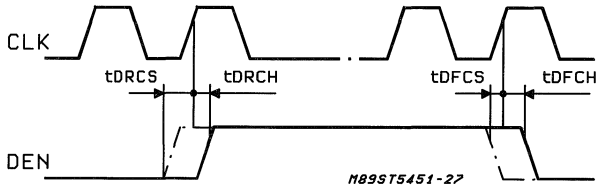
DMA BUS TIMING (Transmission Mode)

Symbol	Parameter	Min.	Max.	Unit
t_{DAS}	Data Setup to ACKX	35		ns
t_{DAH}	Data Hold from ACKX	10		ns
$t_{W\overline{AX}}$	Minimum width $\overline{ACKX}$	60		ns
t_{WAX}	Minimum width ACKX	70		ns
t_{DRAX}	REQX Delay from ACKX	80		ns

DEN TIMING

Symbol	Parameter	Min.	Max.	Unit
t_{DRCS}	DEN setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns
t_{DFCS}	DEN Setup to CLK		30	ns
t_{DRCH}	DEN Hold from CLK		30	ns

Figure 21: DEN Timing



SGS-THOMSON MICROELECTRONICS

ST5080

PIAFE
PROGRAMMABLE ISDN AUDIO FRONT END

ADVANCE DATA

FEATURES:

Complete CODEC and FILTER system including:

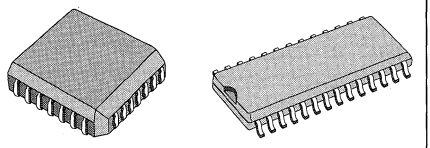
- PCM ANALOG TO DIGITAL AND DIGITAL TO ANALOG CONVERTERS
- TRANSMIT BAND-PASS FILTER
- ACTIVE RC NOISE FILTER
- RECEIVE LOW-PASS FILTER WITH SIN X/X CORRECTION
- MU-LAW OR A-LAW SELECTABLE COMPANDING CODER AND DECODER
- PRECISION VOLTAGE REFERENCE

Phones Features:

- DUAL SWITCHABLE MICROPHONE AMPLIFIER INPUTS. GAIN PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- LOUDSPEAKER AMPLIFIER AUXILIARY OUTPUT. ATTENUATION PROGRAMMABLE: 30 dB RANGE, 2 dB STEP.
- SEPARATE EARPIECE AMPLIFIER OUTPUT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP
- AUXILIARY SWITCHABLE EXTERNAL RING INPUT.
- TRANSIENT SUPRESSION SIGNAL DURING POWER ON.
- INTERNAL PROGRAMMABLE SIDETONE CIRCUIT. ATTENUATION PROGRAMMABLE: 15 dB RANGE, 1 dB STEP.
- INTERNAL RING OR TONE GENERATOR INCLUDING DTMF TONES, SINEWAVE OR SQUAREWAVE WAVEFORMS. ATTENUATION PROGRAMMABLE: 27 dB RANGE, 3 dB STEP.
- COMPATIBLE WITH HANDS-FREE CIRCUIT TEA7540.
- ON CHIP SWITCHABLE ANTI-ACOUSTIC FEED-BACK CIRCUIT (ANTI-LARSEN).

General Features:

- 60 mW OPERATING POWER (TYPICAL).
- 1.0 mW STANDBY POWER (TYPICAL).
- CMOS DIGITAL INTERFACES.
- SINGLE + 5V SUPPLY
- DIGITAL LOOPBACK TEST MODE.



PLCC28 **SO28**

ORDERING NUMBERS:

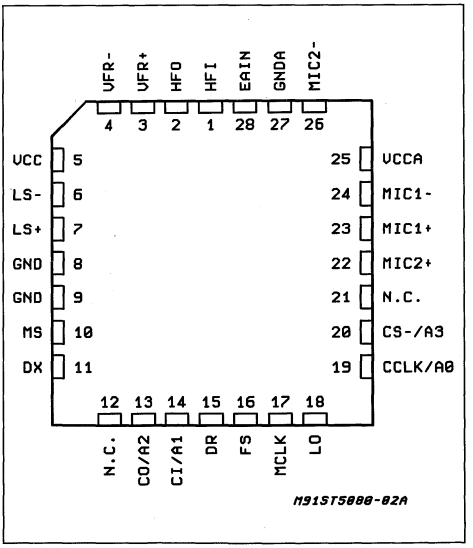
ST5080FN ST5080D

- PROGRAMMABLE DIGITAL AND CONTROL INTERFACES:
  - Digital PCM Interface associated with separate serial Control Interface MICROWIRE™ compatible.
  - GCI interface compatible.

APPLICATIONS:

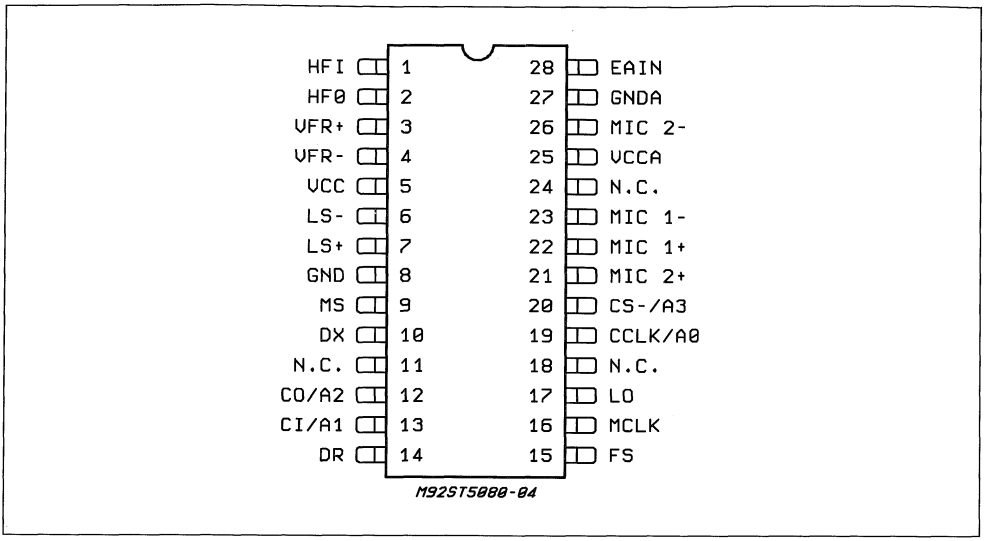
- ISDN TERMINALS.
- DIGITAL TELEPHONE SETS.

PLCC28 PIN CONNECTION (Top view)

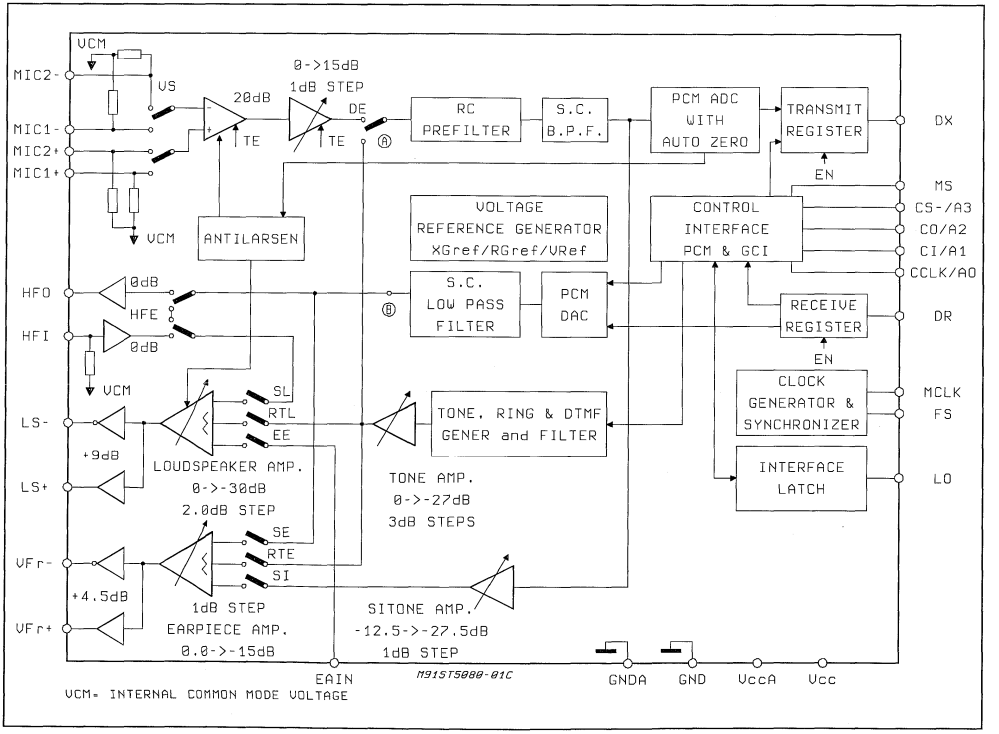


This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

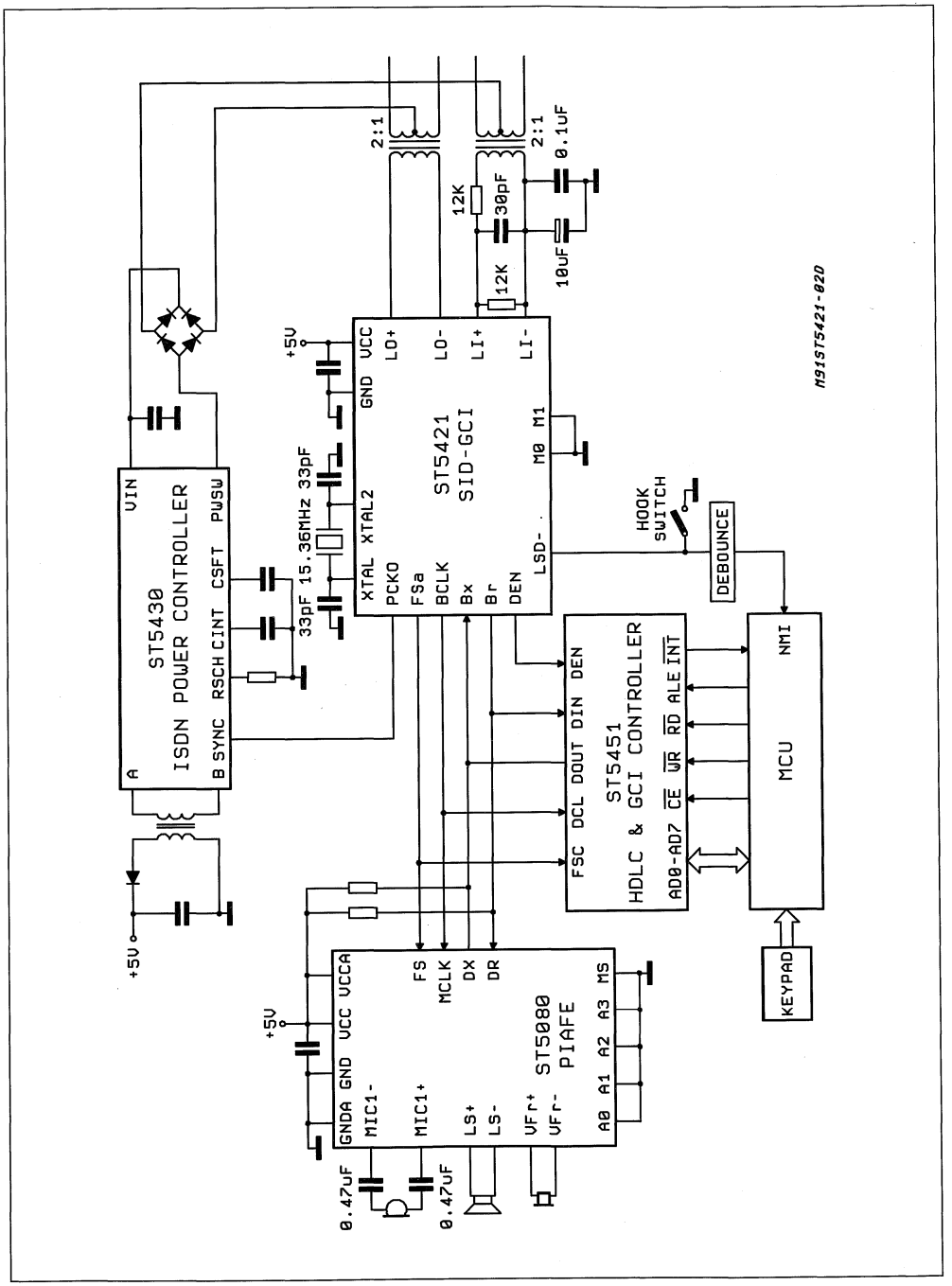
SO28 PIN CONNECTION (Top view)



BLOCK DIAGRAM



TYPICAL ISDN TELEPHONE SET APPLICATION



GENERAL DESCRIPTION

ST 5080 PIAFE is a combined PCM CODEC/FILTER device optimized for ISDN Terminals and Digital Telephone applications. This device is A-law and Mu-law selectable and offers a number of programmable functions accessed through a serial control channel.
Depending on mode selected, control channel is provided by means of a separate serial control channel MICROWIRE compatible or multiplexed with the PCM voice data channel in a GCI compatible format requiring only 4 digital interface pins. When separate serial control interface is selected, PCM interface is compatible with Combo I and Combo II families of devices such as ETC5057/54, TS5070/71.
PIAFE is built using SGS-THOMSON's advanced HCMOS process.
Transmit section of PIAFE consists of an amplifier with switchable high impedance inputs followed by a programmable gain amplifier, an active RC antialiasing pre-filter to provide attenuation of high frequency noise, an 8th order switched capacitor band pass transmit filter and an A-law/Mu-law selectable compandig encoder.
Receive section consist of an A-law/Mu-law selectable expanding decoder which reconstructs the analog sampled data signal, a 3400 Hz low pass filter with sin X/X correction followed by two separate programmable attenuation blocks and two power amplifiers: One can be used to drive an earpiece, and the other to drive a 50 Ω loudspeaker.
Programmable functions on PIAFE include a Ring/Tone generator which provides one or two tones and can be directed to earpiece or to loudspeaker.
A separate programmable gain amplifier allows gain control of the signal injected. Ring/Tone generator provides sinewave or squarewave signal with precise frequencies which may be also directed to the input of the Transmit amplifier for DTMF tone generation. An auxiliary analog input (EAIN) is also provided to enable for example the output of an external band limited Ring signal to the Loudspeaker. Transmit signal may be fed back into the receive ampifier with a programmable attenuation to provide a sidetone circuitry. A switchable anti-accoustic feed-back system cancels the larsen effect is in speech monitoring application. Two additional pins are provided for insertion of an external Handfree function in the Loudspeaker receive path.
An output latch controlled by register programming permits external device control.

PIN FUNCTIONS: PLCC28 / **(SO28)**

Pin	Name	Description
1,2 **(1, 2)**	HFI, HFO	Hands free I/Os: These two pins can be used to insert an external Handfree circuit such as the TEA 7540 in the receive path. HFO is an output which provides the signal issued from output of the receive low pass filter while HFI is a high impendance input which is connected directly to one of the inputs of the Loudspeaker amplifier.
3,4 **(3, 4)**	V_{Fr+}, V_{Fr-}	Receive analog earpiece amplifier complementary outputs, capable of driving load impedances between 100 and 400 Ω. These outputs can drive directly earpiece transductor. The signal at this output can drive be the summ of: - Receive Speech signal from D_R, - Internal Tone Generator, - Sidetone signal.
5 **(5)**	V_{CC}	Positive power supply input for the digital section. +5 V ± 5%.
6,7 **(6, 7)**	LS-,LS+	Receive analog loudspeaker amplifier complementary outputs, intended for driving a Loudspeaker: 80 mW on 50Ω load impedance can be provided at low distorsion meeting specifications. The signal at these outputs can be the summ of: - Receive Speech signal from D_R, - Internal Tone generator, - External input signal from EAIN input.
8,9 **(8)**	GND	Ground: All digital signals are referenced to this pin.

PIN FUNCTIONS (continued)

Pin	Name	Description
10 **(9)**	MS	Mode Select: This input selects COMBO I/II interface mode with separate MICROWIRE Control interface when tied high and GCI mode when tied low.
11 **(10)**	D_X	Transmit Data ouput: Data is shifted out on this pin during the assigned transmit time slots. Elsewhere D_X output is in the high impendance state. In COMBO I/II mode, voice data byte is shifted out from TRISTATE output D_X at the MCLK frequency on the rising edge of MCLK. In GCI mode, voice data byte and control bytes are shifted out from OPEN-DRAIN output D_X at half the MCLK. An external pull up resistor is needed.
12 **(11)**	N.C.	No Connected.
15 **(14)**	D_R	Receive data input: Data is shifted in during the assigned Received time slots. In the COMBO I/II mode, voice data byte is shifted in at the MCLK frequency on the falling edges of MCLK. In the GCI mode, PCM data byte and contol byte are shifted in at half the MCLK frequency on the receive rising edges of MCLK. There is one period delay between transmit rising edge and receive rising edge of MCLK.
16 **(15)**	FS	Frame Sync input: This signal is a 8kHz clock which defines the start of the transmit and receive frames. Either of three formats may be used for this signal: non delayed timing mode, delayed timing and GCI compatible timing mode.
17 **(16)**	MCLK	Master Clock Input: This signal is used by the switched capacitor filters and the encoder/decoder sequencing logic. Values must be 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz selected by means of Control Register CRO. MCLK is used also to shift-in and out data. In GCI mode, 2.56 MHz and 512 kHz are not allowed.
18 **(17)**	LO	Open drain output: a logic 1 written into DO (CR1) appears at LO pin as a logic 0 a logic 0 written into DO puts LO pin in high impedance.
21 **(18)**	N.C.	No Connected.
22 **(21)**	MIC2+	Alternative positive high impedance input to transmit pre-amplifier.
23 **(22)**	MIC1+	Positive high impedance input to transmit pre-amplifier for microphone symetrical connection.
24 **(23)**	MIC1-	Negative high impedance input to transmit pre-amplifier for microphone symetrical connection.
25 **(25)**	V_{CCA}	Positive power supply input for the analog section. +5 V ± 5%. V_{CC} and V_{CCA} must be directly connected together.
26 **(26)**	MIC2-	Alternative negative high impedance input to transmit pre-amplifier.
27 **(27)**	GNDA	Analog Ground: All analog signals are referenced to this pin. GND and GNDA must be connected together close to the device.
28 **(28)**	EAIN	External Auxiliary input: This input can be used to provide alternate signals to the Loudspeaker in place of Internal Ring generator. Input signal should be voice band limited.

Following pin definitions are used only when COMBO I/II mode with separate MICROWIRE compatible serial control port is selected. (MS input set equal one)

PIN FUNCTIONS (continued)

Pin	Name	Description
13 **(12)**	CO	Control data Output: Serial control/status information is shifted out from the PIAFE on this pin when CS- is low on the falling odges of CCLK.
14 **(13)**	CI	Control data Input: Serial Control information is shifted into the PIAFE on this pin when CS- is low on the rising edges of CCLK.
19 **(19)**	CCLK	Control Clock input: This clock shifts serial control information into CI and out from CO when the CS- input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
20 **(20)**	CS-	Chip Select input: When this pin is low, control information is written into and out from the PIAFE via CI and CO pins.

Following pin definitions are used only when the GCI mode is selected. (MS input set equal zero)

PIN FUNCTIONS (continued)

Pin	Name	Description
19,14,13,20 **(19,13,12,20)**	A0,A1,A2,A3	These pins select the address of PIAFE on GCI interface and must be hardwired to either V_{CC} or GND. A0,A1,A2,A3 refer to C4,C5,C6,C7 bits of the first address byte respectively.

FUNCTIONAL DESCRIPTION

Power on initialization:
When power is first applied, power on reset circuitry initializes PIAFE and puts it into the power down state. Gain Control Registers for the various programmable gain amplifiers and programmable switches are initialized as indicated in the Control Register description section. All CODEC functions are disabled. Digital Interface is configured in GCI mode or in COMBO I/II mode depending on Mode Select pin connection.
The desired selection for all programmable functions may be intialized prior to a power up command using Monitor channel in GCI mode or MICROWIRE port in COMBO I/II mode.

Power up/down control:
Following power-on initialization, power up and power down control may be accomplished by writing any of the control instructions listed in Table 1 into PIAFE with "P" bit set to 0 for power up or 1 for power down.
Normally, it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or in a separate single byte instruction.
Any of the programmable registers may also be modified while ST5080 is powered up or down by setting "P" bit as indicated. When power up or down control is entered as a single byte instruction, bit 1 must be set to a 0.
When a power up command is given, all de-activated circuits are activated, but output D_X will remain in the high impedance state on B time slots until the second Fs pulse after power up, even if a B channel is selected.

Power down state:
Following a period of activity, power down state may be reentered by writing a power down instruction.
Control Registers remain in their current state and can be changed either by MICROWIRE control interface or GCI control channel depending on mode selected.
In addition to the power down instruction, detection of loss MCLK (no transition detected) automatically enters the device in "reset" power down state with D_X output in the high impedance state and L0 in high impedance state.

Transmit section:
Transmit analog interface is designed in two stages to enable gains up to 35 dB to be realized. Stage 1 is a low noise differential amplifier providing 20 dB gain. A microphone may be capacitevely connected to MIC1+, MIC1- inputs, while the MIC2+ MIC2– inputs may be used to capacitively connect a second microphone (for digital handsfree operation) or an auxiliary audio circuit such as TEA 7540 Hands-free circuit. MIC1 or MIC2 source is selected with bit 7 of register CR4.
Following the first stage is a programmable gain amplifier which provides from 0 to 15 dB of additional gain in 1 dB step. The total transmit gain should be adjusted so that, at reference point A, see Block Diagram description, the internal 0 dBmO voltage is 0.739 V (overload level is 1.06 Vrms). Second stage amplifier can be programmed with bits 4 to 7 of CR5. To temporarily mute the transmit input, bit TE (6 of CR4) may be set low. In this case, the analog transmit signal is grounded and the sidetone path is also disabled.
An active RC prefilter then precedes the 8th order band pass switched capacitor filter. A/D converter has a compressing characteristic according to CCITT A or mu255 coding laws, which must be selected by setting bits MA, IA in register CR0. A precision on chip voltage reference ensures accurate and highly stable transmission levels.
Any offset voltage arising in the gain-set amplifier, the filters or the comparator is cancelled by an internal autozero circuit.
Each encode cycle begins immediatly at the beginning of the selected Transmit time slot. The total signal delay referenced to the start of the time slot is approximatively 195 µs (due to the transmit filter) plus 123 µs (due to encoding delay), which totals 320 µs. Voice data is shifted out on D_X during the selected time slot on the transmit rising adges of MCLK.

Receive section:
Voice Data is shifted into the decoder's Receive voice data Register via the D_R pin during the selected time slot on the 8 receive edges of MCLK.
The decoder consists of an expanding DAC with either A or MU255 law decoding characteristic which is selected by the same control instruction used to select the Encode law during intitialization. Following the Decoder is a 3400 Hz 6th order low pass switched capacitor filter with integral Sin X/X correction for the 8 kHz sample and hold.
0 dBmO voltage at this (B) reference point (see Block Diagram description) is 0.49 Vrms. A transcient suppressing circuitry ensure interference noise suppression at power up.
The analog speech signal output can be routed either to earpiece (V_{FR+}, V_{FR-} outputs) or to loudspeaker (LS+, LS- outputs) by setting bits SL and SE (1 and 0 of CR4).
Total signal delay is approximatively 190 µs (filter plus decoding delay) plus 62.5 µs (1/2 frame) which gives approximatively 252 µs.

Differential outputs V_{FR+},V_{FR-} are intended to directly drive an earpiece. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 4 to 7 in register CR6. Attenuations in the range 0 to -15 dB relative to the maximum level in 1 dB step can be programmed. The input of this programmable amplifier is the summ of several signals which can be selected by writing to register CR4.:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- Sidetone signal, the amplitude of which is programmed with bits 0 to 3 of register CR5

V_{FR+} and V_{FR-} outputs are capable of driving output power level up to 14mW into differentially connected load impedance between 100 and 400 Ω.

Differential outputs LS+,LS- are intended to directly drive a Loudspeaker. Preceding the outputs is a programmable attenuation amplifier, which must be set by writing to bits 0 to 3 in register CR6. Attenuations in the range 0 to -30 dB relative to the maximum level in 2.0 dB step can be programmed. The input of this programmable amplifier can be the summ of signals which can be selected by writing to register CR4:

- Receive speech signal which has been decoded and filtered,
- Internally generated tone signal, (Tone amplitude is programmed with bits 4 to 7 of register CR7),
- EAIN input which may be an alternate Ring signal or any voice frequency band limited signal. (An external decoupling capacitor of about 0.1µF is necessary).

Receive voice signal may be directed to output HFO by means of bit HFE in Register CR4. After processing, signal must be re-entered through input HF to Loudspeaker amplifier input. (An external decoupling capacitor of about 0.1µF is necessary).
LS+ and LS- outputs are capable of driving output power level up to 80 mW into 50 Ω differentially connected load impedance at low distortion meeting PCM channel specifications. When the signal source is a Ring squarewave signal, power levels up to approximatively 200 mW can be delivered.

Anti-acoustic feed-back for loudspeaker to handset microphone loop with squelch effect: on chip switchable anti-larsen for loudspeaker to handset microphone feedback is implemented. A 12dB depth gain control on both transmit and receive path is provided to keep constant the loop gain. On the transmit path the 12dB gain control is provided starting from the CR5 transmit gain definition; at the same time, on the receive path the 12dB gain control is provided starting from CR6 receive gain definition.

Digital and Control Interface:
PIAFE provides a choice of either of two types of Digital Interface for both control data and PCM.
For compatibility with systems which use time slot oriented PCM busses with a separate Control Interface, as used on COMBO I/II families of devices, PIAFE functions are described in next section.
Alternatively, for systems in which PCM and control data are multiplexed together using GCI interface scheme, PIAFE functions are described in the section following the next one.
PIAFE will automatically switch to one of these two types of interface by sensing the MS pin.
Due to Line Transceiver clock recovery circuitry, a low jitter may be provided on F_S and MCLK clocks. F_S and MCLK must be always in phase. For ST5421S Transceiver, as an example, maximun value of jitter amplitude is a step of 65 ns at each GCI frame (125µs). So, the maximum jitter amplitude is 130 ns pk-pk.

COMBO I/II mode.
Digital Interface (Fig. 1)
F_S Frame Sync input determines the beginning of frame. It may have any duration from a single cycle of MCLK to a squarewave. Two different relationships may be established between the Frame Sync input and the first time slot of frame by setting bit 3 in register CR0. Non delayed data mode is similar to long frame timing on ETC5057/ TS5070 series of devices (COMBO I and COMBO II respectively): first time slot begins nominally coincident with the rising edge of F_S. Alternative is to use delayed data mode, which is similar to short frame sync timing on COMBO I or COMBO II, in which F_S input must be high at least a half cycle of MCLK earlier the frame beginning. A time slot assignment circuit on chip may be used with both timing modes, allowing connection to one of the two B1 and B2 voice data channels.
Two data formats are available: in Format 1, time slot B1 corresponds to the 8 MCLK cycles following immediately the rising edge of FS, while time slot B2 corresponds to the 8 MCLK cycles following immediately time slot B1.
In Format 2, time slot B1 is identical to Format 1. Time slot B2 appears two bit slots after time slot B1. This two bits space is left available for insertion of the D channel data.
Data format is selected by bit FF (2) in register CR0. Time slot B1 or B2 is selected by bit T0 (0) in Control Register CR1.
Bit EN (2) in control register CR1 enables or disables the voice data transfer on D_X and D_R as

Figure 1: Digital Interface Format

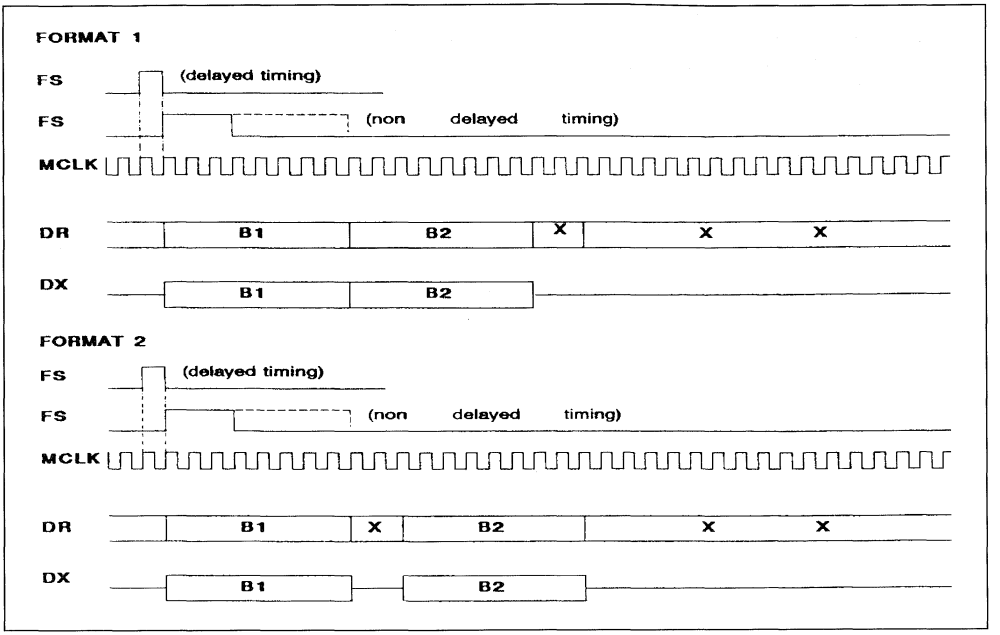
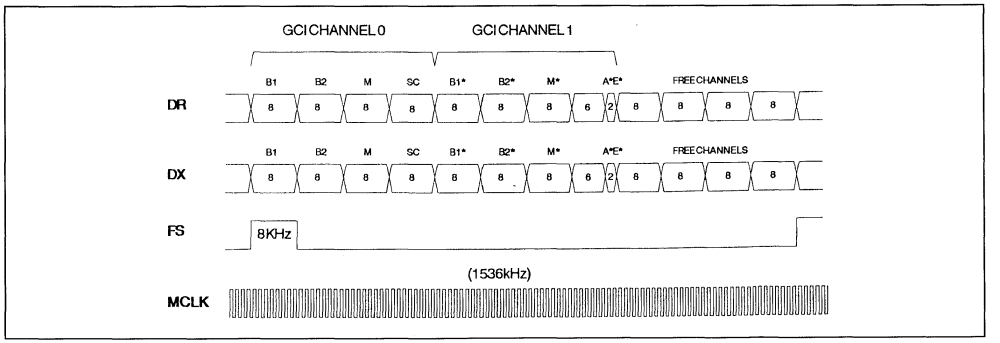


Figure 2: GCI Interface Frame Structure



appropriate. During the assigned time slot, D_X output shifts data out from the voice data register on the rising edges of MCLK. Serial voice data is shifted into D_R input during the same time slot on the falling edges of MCLK.
D_X is in the high impedance Tristate condition when in the non selected time slots.

Control Interface:
Control information or data is written into or read-back from PIAFE via the serial control port consisting of control clock CCLK, serial data input CI and output CO, and Chip Select input, CS-. All control instructions require 2 bytes as listed in Table 1, with the exception of a single byte power-up/down command.
To shift control data into ST5080, CCLK must be pulsed high 8 times while CS- is low. Data on CI input is shifted into the serial input register on the rising edge of each CCLK pulse. After all data is shifted in, the content of the input shift register is decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide CS- pulse or may follow the first contiguously, i.e. it is not mandatory for CS- to return high in between

the first and second control bytes. At the end of the 2nd control byte, data is loaded into the appropriate programmable register. CS- must return high at the end of the 2nd byte.
To read-back status information from PIAFE, the first byte of the appropriate instruction is strobed in during the first CS- pulse, as defined in Table 1. CS- must be set low for a further 8 CCLK cycles, during which data is shifted out of the CO pin on the falling edges of CCLK.
When CS- is high, CO pin is in the high impedance Tri-state, enabling CO pins of several devices to be multiplexed together.
Thus, to summarise, 2 byte READ and WRITE instructions may use either two 8-bit wide CS- pulses or a single 16 bit wide CS- pulse.

Control channel access to PCM interface:
It is possible to access the B channel previously selected in Register CR1.
A byte written into Control Register CR3 will be automatically transmitted from D_X output in the following frame in place of the transmit PCM data.
A byte written into Control Register CR2 will be automatically sent through the receive path to the Receive amplifiers.
In order to implement a continuous data flow from the Control MICROWIRE interface to a B channel, it is necessary to send the control byte on each PCM frame.
A current byte received on D_R input can be read in the register CR2. In order to implement a continuous data flow from a B channel to MICROWIRE interface, it is necessary to read register CR2 at each PCM frame.

GCI COMPATIBLE MODE

GCI interface is an European standardized interface to connect ISDN dedicated components in the different configurations of equipment as Terminals, Network Terminations, PBX, etc...
In a Terminal equipment, this interface called SCIT for Special Circuit Interface for Terminals allows for example connection between:

- ST5421 (SID-GCI) and ST5451 (HDLC/GCI controller) used for 16 kbit/s D channel packet frames processing and SID control,
- Peripheral devices connected to a 64 kbit/s B channel and ST5451 used for GCI peripheral control.

ST5080 may be assigned to one of the B channels present on the GCI interface and is monitored via a control channel which is multiplexed with the 64 kbit/s Voice Data channels.

Figure 2 shows the frame structure at the GCI interface. Two 256 kbit/s channel are supported.

a)GCI channel 0: It is structured in four subchannels:
- B1 channel 8 bits per frame
- B2 channel 8 bits per frame
- M channel 8 bits per frame ignored by PIAFE
- SC channel 8 bits per frame ignored by PIAFE

Only B1 or B2 channel can be selected in PIAFE for PCM data transfer.

b)GCI channel 1: It is structured also in four subchannels:
- B1* channel 8 bits per frame
- B2* channel 8 bits per frame
- M* channel 8 bits per frame
- SC* which is structured as follows:

6 bits ignored by PIAFE
A* bit associated with M* channel
E* bit associated with M* channel.
B1* or B2* channel can be selected in PIAFE for PCM data transfer.
M* channel and two associated bits E* and A* are used for PIAFE control.

Thus, to summarize, B1, B2, B1* or B2* channel can be selected to transmit PCM data and M* channel is used to read/write status/command peripheral device registers. Protocol for byte exchange on the M* channel uses E* and A* bits.

Physical Interface
The interface is physically constitued with 4 wires:

Input Data wire:	D_R
Output Data wire:	D_X
Bit Clock:	MCLK
Frame Synchronization:	F_S

Data is synchronized by MCLK and F_S clock inputs.
F_S insures reinitialization of time slot counter at each frame beginning. The rising edge or FS is the reference time for the first GCI channel bit.
Data is transmitted in both directions at half the MCLK input frequency. Data is transmitted on the the rising edge of MCLK and is sampled one period after the transmit rising edge, also on a rising edge.
Note: Transmit data may be sampled by far-end device ie SID ST5421 on the falling edge 1.5 period after the transmit rising edge.
Unused channel are high impedance. Data outputs are OPEN-DRAIN and need an external pull up resistor.

COMBO activation/deactivation
ST5080 is automatically set in power down mode when GCI clocks are idle. GCI section is reactivated when GCI clocks are detected. PIAFE is completly reactivated after receiving of a power up command.

Exchange protocol on M* channel
Protocol allows a bidirectional transfer of bytes between ST5080 and GCI controller with acknowledgment at each received byte. For PIAFE, standard protocol is simplified to provide read or write register cycles almost identical to MICROWIRE serial interface.

Write cycle
Control Unit sends through the GCI controller following bytes:
- First byte is the chip select byte. The first four bits indicate the device address: (A3,A2,A1,A0). The four last bits are ignored. ST5080 compare the validated byte received internally with the address defined by pins A3, A2, A1, A0. If comparison is true, byte is acknowledged, if not, ST5080 does not acknowledge the byte.

NOTE: An internal "message in progress" flag remains active till the end of the complete message transmission to avoid irrelevant acknowledgement of any further byte.
- Second byte is structured as defined in Table 1.
- Third byte is the Data byte to write into the Register as indicated in Table 1.

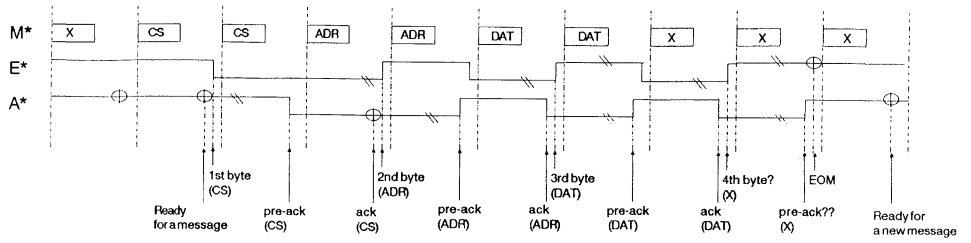
It is possible but optional to write to several different registers in a single message. In this case the Chip Select byte is sent only once at the beginning of the message, the device automatically toggles between address byte and data byte.

Read cycle
Control Unit sends two bytes. First byte is the chip select byte as defined above. Second byte is structured as defined in Table 1.
If PIAFE identifies a read-back cycle, bit 2 of byte 1 in Table 1 equal 1, it has to respond to the Control Unit by sending a single byte message which is the content of the addressed register.
It is possible but optional to request several different read-back register cycles in a single message but it is recommended to wait the answer before requesting a new read back to avoid loss of data. ST5080 responds by sending a single data byte message at each request.

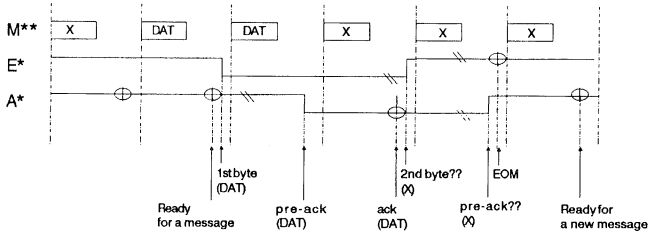
Received byte validation:
A received byte is validated if it is detected two consecutive times identical.

Exchange Protocol:
Exchange protocol is identical for both directions. Sender uses E* bit to indicate that it is sending a M* byte while receiver uses A* bit to acknowledge received byte.
When no message is transferred, E* bit and A* bit are forced to inactive state.
A transmission is initialized by sender putting E* bit from inactive state to active state and by sending first byte on M* channel in the same frame.
Transmission of a message is allowed only if A* bit from the receiver has been set inactive for at least two frames.
When receiver is ready, it validates the received byte internally when received in two consecutive frames identical. Then the receiver sets first A* bit from inactive to active state (pre-acknowlegement), and maintains A* bit active at least in the following frame (acknowledgement). If validation is not possible, (two last bytes received are not identical), receiver aborts the message setting A* bit active for only a single frame.
For the first byte received, Abort sequence is not allowed. PIAFE does not respond either if two last bytes are not identical or if the byte received does not meet the Chip Select byte defined by A0-A3 pins bias.
A second byte may be transmitted by the sender putting E* bit from active to inactive state and sending the second byte on the M* channel in the same frame. E* bit is set inactive for only one frame. If it remains inactive more than one frame, it is an end of message (i.e. not second byte available).
The second byte may be transmitted only after receiving the pre-acknowledgment of the previous byte transmitted (see Fig. 3). The same protocol is used if a third byte is transmitted. Each byte has to be transmitted at least in two consecutive frames.
The receiver validates current received byte as done on first byte and then set A* bit in the next two frames first from active to inactive state (pre-acknowledgement), and after from inactive to active state (acknowledgement). If the receiver cannot validate the received current byte (two bytes received are not identical), it pre-acknowledges normally, but let A* bit in the inactive state in the next frame which indicates an abort request.
If a message sent by ST5080 is aborted, it will stop the message and wait for a new read cycle instruction from the controller.
A message received by ST5080 is acknowledged or aborted without flow Control.
Figures 3 gives timing of a write cycle. Most significant bit (MSB) of a Monitor byte is sent first on M* channel.
E* and A* bits are active low and inactive state on DOUT is high impedance.

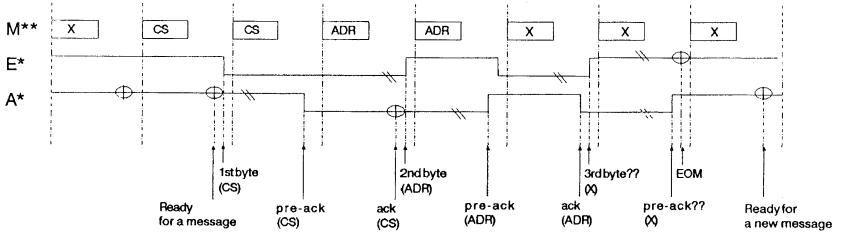
Figure 3: E and A bits Timing



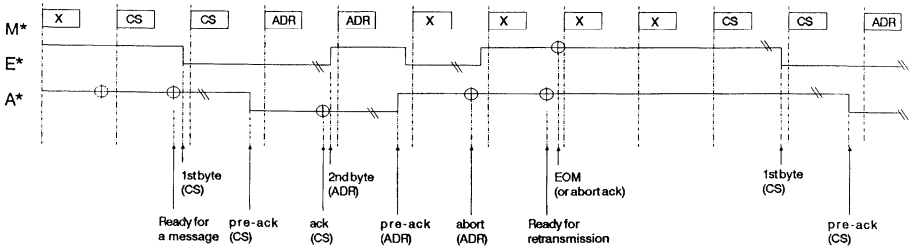
THREE BYTES MESSAGE - NORMAL TRANSMISSION



ONE BYTE MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE - NORMAL TRANSMISSION



TWO BYTES MESSAGE ABORTED ON THE SECOND AND RETRANSMITTED

PROGRAMMABLE FUNCTIONS

For both formats of Digital Interface, programmable functions are configured by writing to a number of registers using a 2-byte write cycle (not including chip select byte in GCI).

Most of these registers can also be read-back for verification. Byte one is always register address, while byte two is Data.

Table 1 lists the register set and their respective adresses.

Table 1: Programmable Register Intructions

Function	Address byte								Data byte
	7	6	5	4	3	2	1	0	
Single byte Power up/down	P	X	X	X	X	X	0	X	none
Write CR0	P	0	0	0	0	0	1	X	see CR0 TABLE 2
Read-back CR0	P	0	0	0	0	1	1	X	see CR0
Write CR1	P	0	0	0	1	0	1	X	see CR1 TABLE 3
Read-back CR1	P	0	0	0	1	1	1	X	see CR1
Write Data to receive path	P	0	0	1	0	0	1	X	see CR2 TABLE 4
Read data from D_R	P	0	0	1	0	1	1	X	see CR2
Write Data to D_X	P	0	0	1	1	0	1	X	see CR3 TABLE 5
Write CR4	P	0	1	0	0	0	1	X	see CR4 TABLE 6
Read-back CR4	P	0	1	0	0	1	1	X	see CR4
Write CR5	P	0	1	0	1	0	1	X	see CR5 TABLE 7
Read-back CR5	P	0	1	0	1	1	1	X	see CR5
Write CR6	P	0	1	1	0	0	1	X	see CR6 TABLE 8
Read-back CR6	P	0	1	1	0	1	1	X	see CR6
Write CR7	P	0	1	1	1	0	1	X	see CR7 TABLE 9
Read-back CR7	P	0	1	1	1	1	1	X	see CR7
Write CR8	P	1	0	0	0	0	1	X	see CR8 TABLE 10
Read-back CR8	P	1	0	0	0	1	1	X	see CR8
Write CR9	P	1	0	0	1	0	1	X	see CR9 TABLE 11
Read-back CR9	P	1	0	0	1	1	1	X	see CR9
Write Test Register CR10	P	1	0	1	0	0	1	X	reserved

NOTE 1: bit 7 of the address byte and data byte is always the first bit clocked into or out from: CI and CO pins when MICROWIRE serial port is enabled, or into and out from D_R and D_X pins when GCI mode selected.
X = reserved: write 0

NOTE 2: "P" bit is Power up/down Control bit. P = 1 Means Power Down.
Bit 1 indicates, if set, the presence of a second byte.

NOTE 3: Bit 2 is write/read select bit.

Table 2: Control Register CR0 Functions

7	6	5	4	3	2	1	0	Function		
F1	F0	MA	IA	DN	FF	B7	DL			
0	0							MCLK = 512 kHz		(1)
0	1							MCLK = 1.536 MHz	*	
1	0							MCLK = 2.048 MHz		
1	1							MCLK = 2.560 MHz		(1)
		0	X					Select MU-255 law	*	
		1	0					A-law including even bit inversion		
		1	1					A-law; No bit inversion		
				0				Delayed data timing	*	(1)
				1				Non delayed data timing		(1)
					0			B1 and B2 consecutive	*	(1)
					1			B1 and B2 separated		(1)
						0		8 bits time-slot	*	
						1		7 bits time-slot		
							0	Normal operation	*	
							1	Digital Loop-back		

*: state at power on initialization

(1): significant in COMBO I/II mode only

Table 3: Control Register CR1 Functions

7	6	5	4	3	2	1	0	Function		
HFE	ALE	DO	MR	MX	EN	T1	T0			
0								HFO / HFI pins disabled	*	
1								HFO / HFi pins enabled		
	0							Anti-larsen disabled	*	
	1							Anti-larsen enabled		
		0						L0 latch is put in high impedance	*	
		1						L0 latch set to 0		
			0					D_R connected to rec. path	*	(1)
			1					CR2 connected to rec. path		(1)
				0				Trans path connected to D_X	*	(1)
				1				CR3 connected to D_X		(1)
					0			voice data transfer disable	*	
					1			voice data transfer enable		
						0	0	B1 channel selected	*	
						0	1	B2 channel selected		
						1	0	B1* channel selected		(2)
						1	1	B2* channel selected		(2)

*: state at power on initialization

(1): significant in COMBO I / II mode only

(2): significant in GCI mode only.

Table 4: Control Register CR2 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	Data sent to Receive path or Data received from D_R input

Table 5: Control Registers CR3 Functions

7	6	5	4	3	2	1	0	Function
d7	d6	d5	d4	d3	d2	d1	d0	
msb							lsb	D_X data transmitted

Table 6: Control Register CR4 Functions

7	6	5	4	3	2	1	0	Function	
VS	TE	SI	EE	RTL	RTE	SL	SE		
0 1								MIC1 selected MIC2 selected	*
	0 1							Transmit input muted Transmit input enabled	*
		0 1						Internal sidetone disabled Internal sidetone enabled	*
			0 1					EAIN disconnected EAIN selected to Loudspeaker	*
				0 0 1 1	0 1 0 1			Ring / Tone muted Ring / Tone to Earpiece Ring / Tone to Loudspeaker Ring / Tone to Earpiece and Loudspeaker	*
						0 0 1 1	0 1 0 1	Receive signal muted Receive signal connected to earpiece amplifer Receive signal connected to loudspeaker amplifier Receive signal connected to loudspeaker and earpiece amplifier	*

state at power on initialization

Table 7: Control Register CR5 Functions

7	6	5	4	3	2	1	0	Function
Transmit amplifier				Sidetone amplifier				
0	0	0	0					0 dB gain *
0	0	0	1					1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					15 dB gain
				0	0	0	0	-12.5 dB gain *
				0	0	0	1	-13.5 dB gain
				-	-	-	-	in 1 dB step
				1	1	1	1	-27.5 dB gain

*: state at power on initialization

Table 8: Control Register CR6 Functions

7	6	5	4	3	2	1	0	Function
Earpiece amplifier				Loudspeaker				
0	0	0	0					0 dB gain *
0	0	0	1					-1 dB gain
-	-	-	-					in 1 dB step
1	1	1	1					-15 dB gain
				0	0	0	0	0 dB gain *
				0	0	0	1	-2 dB gain
				-	-	-	-	in 2 dB step
				1	1	1	1	-30 dB gain

*: state at power on initialization

Table 9: Control Register CR7 Functions

7	6	5	4	3	2	1	0	Function		
Tone gain				F1	F2	SN	DE	Attenuation	f1 V_{pp}	f2 V_{pp}
0	0	0	0					0 dB *	2.4 (1)	1.9 (1)
0	0	0	1					-3 dB	1.70	1.34
0	0	1	0					-6 dB	1.20	0.95
0	0	1	1					- 9 dB	0.85	0.67
0	1	0	0					-12 dB	0.60	0.47
0	1	0	1					-15 dB	0.43	0.34
0	1	1	0					-18 dB	0.30	0.24
0	1	1	1					-21 dB	0.21	0.17
1	X	X	0					-24 dB	0.15	0.12
1	X	X	1					-27 dB	0.10	0.08
				0	0			f1 and f2 muted		*
				0	1			f2 selected		
				1	0			f1 selected		
				1	1			f1 and f2 in summed mode		
						0		Squarewave signal selected		*
						1		Sinewave signal selected		
							0	Normal operation		*
							1	Tone / Ring Generator connected to Transmit path		

*: state at power on initialization

(1): value provided if f1 or f2 is selected alone.
if f1 and f2 are selected in the summed mode, f1=1.34 V_{pp} while f2=1.06 V_{pp}.
Output generator is 2.4 V_{pp}

X reserved: write 0

Table 10: Control Register CR8 Functions

7	6	5	4	3	2	1	0	Function
f17	f16	f15	f14	f13	f12	f11	f10	
msb							lsb	Binary equivalent of the decimal number used to calculate f1

Table 11: Control Register CR9 Functions

7	6	5	4	3	2	1	0	Function
f27	f26	f25	f24	f23	f22	f21	f20	
msb							lsb	Binary equivalent of the decimal number used to calculate f2

CONTROL REGISTER CR0

First byte of a READ or a WRITE instruction to Control Register CR0 is as shown in TABLE 1. Second byte is as shown in TABLE 2.

Master Clock Frequency Selection

A master clock must be provided to PIAFE for operation of filter and coding/decoding functions.
In COMBO I/II mode, MCLK frequency can be either 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz.
Bit F1 (7) and F0 (6) must be set during initialization to select the correct internal divider.
In GCI mode, MCLK must be either 1.536MHz or 2.048MHz.
512KHz and 2.56MHz are not allowed.
Default value is 1.536 MHz for both modes.
Any clock different from the default one must be selected prior a Power-Up instruction for both modes.

Coding Law Selection

Bits MA (5) and IA (4) permit selection of Mu-255 law or A law coding with or without even bit inversion.
After power on initialization, the Mu-255 law is selected.

	Mu 255 law								True A law even bit inversion								A law without even bit inversion							
	msb							lsb	msb							lsb	msb							lsb
Vin = + full scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0	1	1	1	1	1	1	1	1
Vin = 0 V	1 0	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 0	1 1	0 0	1 1	0 0	1 1	0 0	1 1	1 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
Vin = - full scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	1	1	1	1	1

MSB is always the first PCM bit shifted in or out of PIAFE.

Digital Interface timing

Bit DN=0 (3) selects digital interface in delayed timing mode while DN=1 selects non delayed data timing.
In GCI mode, bit DN is not significant.
After reset and if COMBO I/II mode is selected, delayed data timing is selected.

Digital Interface format

Bit FF=0 (2) selects digital interface in Format 1 where B1 and B2 channel are consecutive. FF=1 selects Format 2 where B1 and B2 channel are separated by two bits. (see digital interface format section).
In GCI mode, bit FF is not significant.

56+8 selection

Bit 'B7' (1) selects capability for PIAFE to take into account only the seven most significant bits of the PCM data byte selected.
When 'B7' is set, the LSB bit on D_R is ignored and LSB bit on D_X is high impedance. This function allows connection of an external "in band" data generator directly connected on the Digital Interface.

Digital loopback

Digital loopback mode is entered by setting DL bit(0) equal 1.
In Digital Loopback mode, data written into Receive PCM Data Register from the selected received time-slot is read-back from that Register in the selected transmit time-slot on D_X. Time slot is selected with Register CR1.
No PCM decoding or encoding takes place in this mode. Transmit and Receive amplifier stages are muted.

CONTROL REGISTER CR1

First byte of a READ or a WRITE instruction to Control Register CR1 is as shown in TABLE 1. Second byte is as shown in TABLE 3.

Hands-free I/Os selection

Bit HFE set to one enables HFI, HFO pins for connection of an external handfree circuit such as TEA 7540. HFO is an analog output that provides the receive voice signal. 0 dBMO level on that output is 0.491 Vrms ($1.4V_{pp}$). HFI is an analog high impedance input (10 KΩ typ.) intended to send back the processed receive signal to the Loudspeaker. 0 dBMO level on that input is 0.491Vrms.

Anti-larsen selection

Bit ALE set to one enables on-chip antilarsen and squelch effect system.

Latch output control

Bit DO controls directly logical status of latch output LO: ie, a "ZERO" written in bit DO puts output LO in high impedance, a "ONE" written in bit DO sets output LO to zero.

Microwire access to B channel on receive path
Bit MR (4) selects access from MICROWIRE Register CR2 to Receive path. When bit MR is set high, data written to register CR2 is decoded each frame, sent to the receive path and data input at D_R is ignored.
In the other direction, current PCM data input received at D_R can be read from register CR2 each frame.

Microwire access to B channel on transmit path
Bit MX (3) selects access from MICROWIRE write only Register CR3 to D_X output. When bit MX is set high, data written to CR3 is output at D_X every frame and the output of PCM encoder is ignored.

B channel selection
Bit 'EN' (2) enables or disables voice data transfer on D_X and D_R pins. When disabled, PCM data from DR is not decoded and PCM time-slots are high impedance on D_X.
In GCI mode, bits 'T1' (1) and 'T0' (0) select one of the four channels of the GCI interface.
In COMBO I/II mode, only B1 or B2 channel can be selected according to the interface format selected. Bit 'T1' is ignored.

CONTROL REGISTER CR2
Data sent to receive path or data received from D_R input. Refer to bit MR(4) in "Control Register CR1" paragraph.

CONTROL REGISTER CR3
D_X data transmitted. Refer to bit MX(3) in "Control Rgister CR1" paragraph.

CONTROL REGISTER CR4
First byte of a READ or a WRITE instruction to Control Register CR4 is as shown in TABLE 1. Second byte is as shown in TABLE 6.

Transmit Input Selection
MIC1 or MIC2 source is selected with bit VS (7).
Transmit input selected can be enabled or muted with bit TE (6).
Transmit gain can be adjusted within a 15 dB range in 1 dB step with Register CR5.

Sidetone select
Bit "SI" (5) enables or disables Sidetone circuitry. When enabled, sidetone gain can be adjusted with Register (CR5). When Transmit path is disabled, bit TE set low, sidetone circuit is also disabled.

External Auxiliary signal select
Bit "EE" (4) set to one connects EAIN input to the loudspeaker amplifier input.

Ring/Tone signal routing
Bits "RTL" (3) and RTE (2) provide select capability to connect on-chip Ring/Tone generator either to loudspeaker amplifier input or to earpiece amplifier input or both.

PCM receive data routing
Bits "SL" (1) and "SE" (0) provide select capability to connect received speech signal either to Loudspeaker amplifier input or to earpiece amplifier input or both.

CONTROL REGISTER CR5
First byte of a READ or a WRITE instuction to Control Register CR5 is as shown in TABLE 1. Second byte is as shown in TABLE 7.

Transmit gain selection
Transmit amplifier can be programmed for a gain from 0dB to 15dB in 1dB step with bits 4 to 7.
0 dBmO level at the output of the transmit amplifier (A reference point) is 0.739 Vrms (overload voltage is 1.06 Vrms).

Sidetone attenuation selection
Transmit signal picked up after the switched capacitor low pass filter may be fed back into the Receive Earpiece amplifier.
Attenuation of the signal at the output of the sidetone attenuator can be programmed from –12.5dB to -27.5dB relative to reference point A in 1 dB step with bits 0 to 3.

CONTROL REGISTER CR6
First byte of a READ or a WRITE instruction to Control Register CR6 is as shown in TABLE 1. Second byte is as shown in TABLE 8.

Earpiece amplifier gain selection:
Earpiece Receive gain can be programmed in 1 dB step from 0 dB to -15 dB relative to the maximum with bits 4 to 7.
0 dBmO voltage at the output of the amplifier on pins V_{Fr+} and V_{Fr-} is then 824.5 mVrms when 0dB gain is selected down to 146.6 mVrms when –15 dB gain is selected.

Loudspeaker amplifier gain selection:
Loudspeaker Receive amplifier gain can be programmed in 2 dB step from 0 dB to -30 dB relative to the maximum with bits 0 to 3.
0 dBmO voltage on the output of the amplifier on pins LS+ and LS- on 50 Ω is then 1.384 Vrms ($3.91V_{pp}$) when 0 dB gain is selected down to 43.7 mVrms ($123.6mV_{pp}$) when -30 dB gain is selected.

Current limitation is approximatively 150 mApk.

CONTROL REGISTER CR7:
First byte of a READ or a WRITE instruction to Control Register CR7 is as shown in TABLE 1. Second byte is as shown in TABLE 9.

Tone/Ring amplifier gain selection
Output level of Ring/Tone generator, before attenuation by programmable attenuator is 2.4 Vpk-pk when f1 generator is selected alone or summed with the f2 generator and 1.9 Vpk-pk when f2 generator is selected alone.
Selected output level can be attenuated down to -27 dB by programmable attenutator by setting bits 4 to 7.

Frequency mode selection
Bits 'F1' (3) and 'F2' (2) permit selection of f1 and/or f2 frequency generator according to TABLE 9.
When f1 (or f2) is selected, output of the Ring/Tone is a squarewave (or a sinewave) signal at the frequency selected in the CR8 (or CR9) Register.
When f1 and f2 are selected in summed mode, output of the Ring/Tone generator is a signal where f1 and f2 frequency are summed.
In order to meet DTMF specifications, f2 output level is attenuated by 2dB relative to the f1 output level.
Frequency temporization must be controlled by the microcontroller.

Waveform selection
Bit 'SN' (1) selects waveform of the output of the Ring/Tone generator. Sinewave or squarewave signal can be selected.

DTMF selection
Bit DE (0) permits connection of Ring/Tone/DTMF generator on the Transmit Data path instead of the Transmit Amplifier output. Earpiece feed-back may be provided by sidetone circuitry by setting bit SI or directly by setting bit RTE in Register CR4. Loudspeaker feed-back may be provided directly by setting bit RTL in Register CR4.

CONTROL REGISTERS CR8 AND CR9
First byte of a READ or a WRITE instruction to Control Register CR8 or CR9 is as shown in TABLE 1. Second byte is respectively as shown in TABLE 10 and 11.
Tone or Ring signal frequency value is defined by the formula:

$f1 = CR8 / 0.128$ Hz

and

$f2 = CR9 / 0.128$ Hz

where CR8 and CR9 are decimal equivalents of the binary values of the CR8 and CR9 registers respectively. Thus, any frequency between 7.8 Hz and 1992 Hz may be selected in 7.8 Hz step.
TABLE 12 gives examples for the main frequencies usual for Tone or Ring generation.

Table 12: Examples of Usual Frequency Selection

Description	f1 value (decimal)	Theoric value (Hz)	Typical value (Hz)	Error %
Tone 250 Hz	32	250	250	.00
Tone 330 Hz	42	330	328.2	−.56
Tone 425 Hz	54	425	421.9	−.73
Tone 440 Hz	56	440	437.5	−.56
Tone 800 Hz	102	800	796.9	−.39
Tone 1330 Hz	170	1330	1328.1	−.14
DTMF 697 Hz	89	697	695.3	−.24
DTMF 770 Hz	99	770	773.4	+.44
DTMF 852 Hz	109	852	851.6	−.05
DTMF 941 Hz	120	941	937.5	−.37
DTMF 1209 Hz	155	1209	1210.9	+.16
DTMF 1336 Hz	171	1336	1335.9	−.01
DTMF 1477 Hz	189	1477	1476.6	.00
DTMF 1633 Hz	209	1633	1632.8	.00
SOL	50	392	390.6	−.30
LA	56	440	437.5	−.56
SI	63	494	492.2	−.34
DO	67	523.25	523.5	+.04
RE	75	587.33	586.0	−.23
MI flat	80	622.25	625.0	+.45
MI	84	659.25	656.3	−.45
FA	89	698.5	695.3	−.45
FA sharp	95	740	742.2	+.30
SOL	100	784	781.3	−.34
SOL sharp	106	830.6	828.2	−.29
LA	113	880	882.9	+.33
SI	126	987.8	984.4	−.34
DO	134	1046.5	1046.9	+.04
RE	150	1174.66	1171.9	−.23
MI	169	1318.5	1320.4	+.14

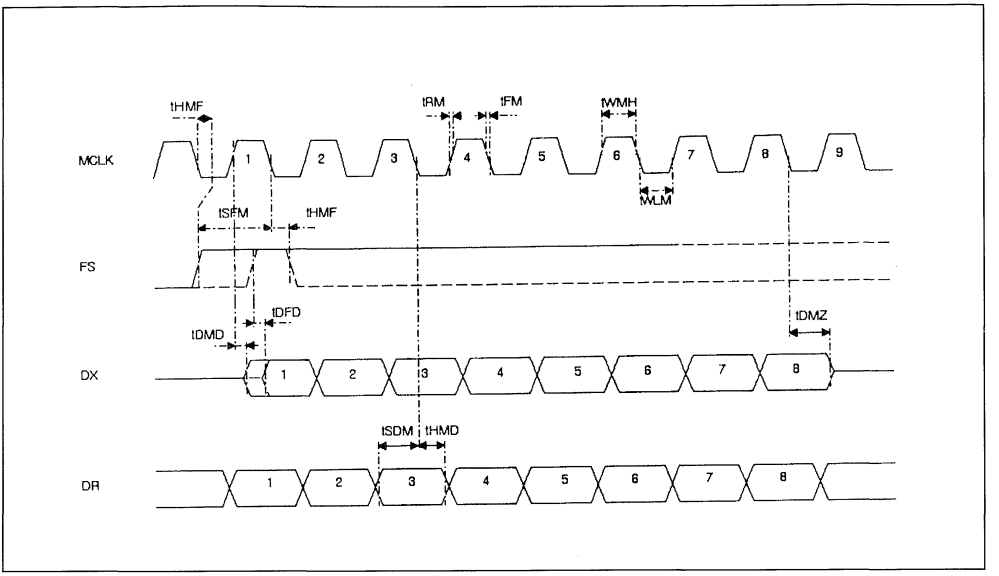
POWER SUPPLIES

While pins of PIAFE device are well protected against electrical misuse, it is recommended that the standard CMOS practise of applying GND before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

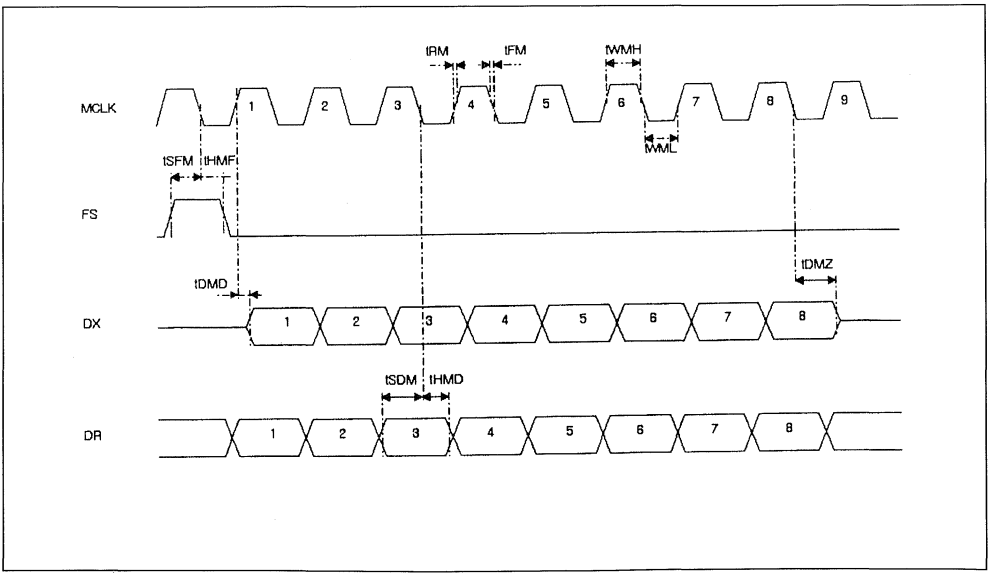
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A power supply decoupling capacitor of 0.1 µF should be connected from this common point to V_{CC} as close as possible to the device pins.

TIMING DIAGRAM

Non Delayed Data Timing Mode

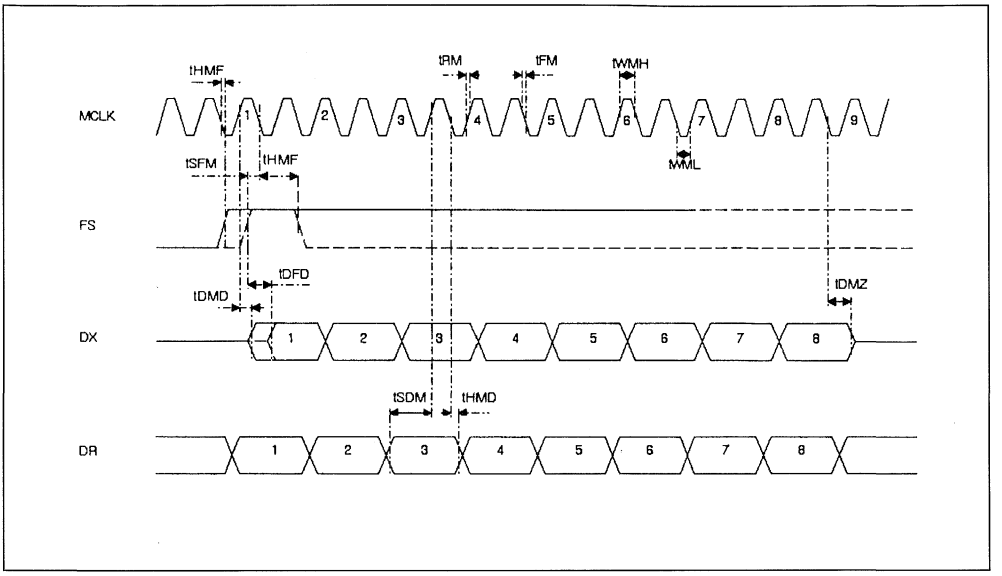


Delayed Data Timing Mode

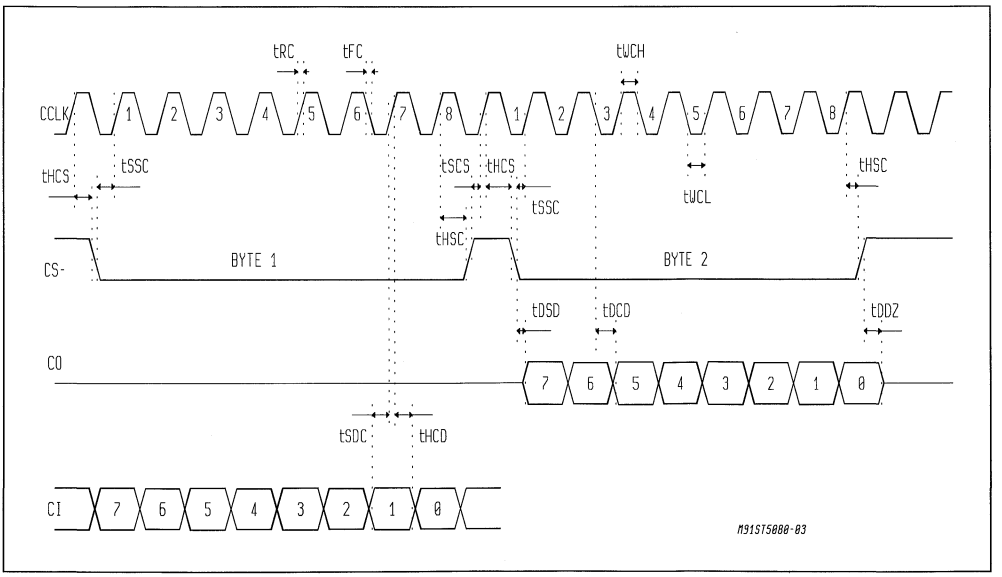


TIMING DIAGRAM (continued)

GCI Timing Mode



Serial Control Timing (MICROWIRE MODE)



ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
V_{CC} to GND	7	V
Voltage at V_{FxI}	V_{CC} + 1 to GND - 1	V
Current at V_{RxO} and LS	± 100	mA
Voltage at any digital input	V_{CC} + 1 to GND - 1	V
Current at any digital output	± 50	mA
Storage temperature range	- 65 to + 150	°C
Lead Temperature (soldering, 10s)	+ 300	°C

TIMING SPECIFICATIONS (unless otherwise specified, V_{CC} = 5V ± 5%, T_a = 0°C to 70°C ; typical characteristics are specified V_{CC} = 5V, T_A = 25 °C; all signals are referenced to GND, see Note 5 for timing definitions)

MASTER CLOCK TIMING

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{MCLK}	Frequency of MCLK	Selection of frequency is programmable (see table 2)		512 1.536 2.048 2.560		kHz MHz MHz MHz
t_{WMH}	Period of MCLK high	Measured from V_{IH} to V_{IH}	80			ns
t_{WML}	Period of MCLK low	Measured from V_{IL} to V_{IL}	80			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns

PCM INTERFACE TIMING (COMBO I / II and GCI modes)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
t_{HMF}	Hold Time MCLK low to FS low		0			ns
t_{SFM}	Setup Time, FS high to MCLK low		30			ns
t_{DMD}	Delay Time, MCLK high to data valid	Load = 100 pf			100	ns
t_{DMZ}	Delay Time, MCLK low to DX disabled		15		100	ns
t_{DFD}	Delay Time, FS high to data valid	Load = 100 pf ; Applies only if FS rises later than MCLK rising edge in Non Delayed Mode only			100	ns
t_{SDM}	Setup Time, D_R valid to MCLK receive edge		20			ns
t_{HMD}	Hold Time, MCLK low to D_R invalid		10			ns

SERIAL CONTROL PORT TIMING (Usual COMBO I / II mode only)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CCLK}	Frequency of CCLK				2.048	MHz
t_{WCH}	Period of CCLK high	Measured from V_{IH} to V_{IH}	160			ns
t_{WCL}	Period of CCLK low	Measured from V_{IL} to V_{IL}	160			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK high to CS– low		10			ns
t_{SSC}	Setup Time, CS– low to CCLK high		50			ns
t_{SDC}	Setup Time, CI valid to CCLK high		50			ns
t_{HCD}	Hold Time, CCLK high to CI invalid		50			ns
t_{DCD}	Delay Time, CCLK low to CO data valid	Load = 100 pF , plus 1 LSTTL load			60	ns
t_{DSD}	Delay Time, CS–low to CO data valid				50	ns
t_{DDZ}	Delay Time CS–high or 8th CCLK low to CO high impedance whichever comes first		15		80	ns
t_{HSC}	Hold Time, 8th CCLK high to CS– high		100			ns
t_{SCS}	Set up Time, CS– high to CCLK high		100			ns

Note 5: A signal is valid if it is above V_{IH} or below V_{IL} and invalid if it is between V_{IL} and V_{IH}.
For the purpoes of this specification the following conditions apply:
a) All input signal are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10ns, t_F < 10ns.
b) Delay times are measured from the inputs signal valid to the output signal valid.
c) Setup times are measured from the data input valid to the clock input invalid.
d) Hold times are measured from the clock signal valid to the data input invalid.

ELECTRICAL CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 5%, T_a = 0°C to 70°C ; typical characteristic are specified at V_{CC} = 5V, T_A = 25°C ; all signals are referenced to GND)

DIGITAL INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	All digital inputs (DC)			0.7	V
V_{IH}	Input High Voltage	All digital inputs (DC)	2.0			V
V_{IL}	Input Low Voltage	All digital inputs (AC)			0.4	V
V_{IH}	Input High Voltage	All digital inputs (AC)	2.7			V
V_{OL}	Output Low Voltage	D_X,I_L = -2.0mA; all other digital outputs, I_L = –1mA			0.4	V
V_{OH}	Output High Voltage	D_X,I_L = 2.0mA; all other digital outputs, I_L = 1mA	2.4			V
I_{IL}	Input Low Current	Any digital input, GND < V_{IN} < V_{IL}	-10		10	µA
I_{IH}	Input High Current	Any digital input, V_{IH} < V_{IN} < V_{CC}	-10		10	µA
I_{OZ}	Output Current in High impedance (Tri-state)	D_X and CO	-10		10	µA

ANALOG INTERFACES

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{MIC}	Input Leakage	GND < V_{MIC} < V_{CC}	-100		+100	µA
R_{MIC}	Input Resistance	GND < V_{MIC} < V_{CC}	50			kΩ
R_{LVFr}	Load Resistance	V_{Fr+} to V_{Fr-}	100			Ω
C_{LVFr}	Load Capacitance	from V_{Fr+} to V_{Fr-} ; R_{LVFr} > 100Ω			200	pf
R_{OVFr0}	Output Resistance	Steday zero PCM code applied to DR; I = ± 1mA		1.0		Ω
V_{OSVFr0}	Differential offset: Voltage at V_{Fr+}, V_{Fr-}	Alternatig ± zero PCM code applied to DR maximum receive gain; R_L = 100Ω	-100		+100	mV
R_{LLS}	Load Resistance	L_{S+} to L_{S-}		50		Ω
C_{LLS}	Load Capacitance	from L_{S+} to L_{S-}; R_{LLS} = 50Ω			200	pf
R_{OLS}	Output Resistance	Steady zero PCM code applied to DR; I ± 1mA		1		Ω
V_{OSLS}	Differential offset Voltage at L_{S+}, L_{S-}	Alternatig ± zero PCM code applied to DR maximum receive gain; R_L = 50Ω	–100		+100	mV

POWER DISSIPATION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_{CC0}	Power down Current	CCLK,CI = 0.4V; CS = 2.4V (µwire only) All other inputs active GCI mode only:		0.2 0.2		mA mA
I_{CC1}	Power Up Current	L_{S+}, L_{S-} and V_{Fr+}, V_{Fr-} not loaded		12.0		mA

TRANSMISSION CHARACTERISTICS (unless otherwise specified, V_{CC} = 5V ± 5%, T_a = 0°C to 70°C; typical characteristics are specified at V_{CC} = 5V, T_a = 25°C, MIC1/2 = 0dB_{m0}, D_R = 0dB_{m0} PCM code, f = 1015.625 Hz; all signal are referenced to GND)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Transmit path - Absolute levels at MIC1 / MIC2

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Transmit Amps connected for 0dB gain		73.9		mV_{RMS}
Overload level	A law selected		106.08		mV_{RMS}
Overload level	mu law selected		106.47		mV_{RMS}
0 dBM0 level	Transmit Amps connected for 15dB gain		13.14		mV_{RMS}
Overload level	A law selected		18.86		mV_{RMS}
Overload level	mu law selected		18.93		mV_{RMS}

TRANSMISSION CHARACTERISTICS (continued)

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at V_{FR}

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		824.5		mV_{RMS}
0 dBM0 level	Receive Amp programmed for - 15dB attenuation		146.6		mV_{RMS}

AMPLITUDE RESPONSE (Maximum, Nominal, and Minimum Levels)
Receive path - Absolute levels at L_S

Parameter	Test Condition	Min.	Typ.	Max.	Unit
0 dBM0 level	Receive Amp programmed for 0dB gain		1.384		V_{RMS}
0 dBM0 level	Receive Amp programmed for - 30dB gain		43.7		mV_{RMS}

AMPLITUDE RESPONSE
Transmit path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for maximum. Measure deviation of Digital PCM Code from ideal $0dB_{m0}$ PCM code at D_X	-0.30		0.30	dB
G_{XAG}	Transmit Gain Variation with programmed gain	Measure Transmit Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GXA, i.e. $G_{AXG} = G_{actual} - G_{prog.} - G_{XA}$	-0.5		0.5	dB
G_{XAT}	Transmit Gain Variation with temperature	Measured relative to G_{XA}. min. gain < G_X < Max. gain	-0.1		0.1	dB
G_{XAV}	Transmit Gain Variation with supply	Measured relative to G_{XA} G_X = Maximum gain	-0.05		0.05	dB
G_{XAF}	Transmit Gain Variation with frequency	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_X < Max. gain f = 60 Hz f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz to 5000 Hz f = 5000 Hz and up	 -1.5 -0.3 -0.8		 -26 -0.1 0.3 0.0 -14 -32 -40	 dB dB dB dB dB dB dB
G_{XAL}	Transmit Gain Variation with signal level	Sinusoidal Test method. Reference Level = $-10\ dB_{m0}$ V_{FXI} = $-40\ dB_{m0}$ to $+3\ dB_{m0}$ V_{FXI} = $-50\ dB_{m0}$ to $-40\ dB_{m0}$ V_{FXI} = $-55\ dB_{m0}$ to $-50\ dB_{m0}$	 -0.25 -0.5 -1.5		 0.25 0.5 1.5	 dB dB dB

AMPLITUDE RESPONSE

Receive path

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAE}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $V_{Fr\pm}$	-0.3		0.3	dB
G_{RAL}	Receive Gain Absolute Accuracy	Receive gain programmed for maximum Apply 0 dB_{m0} PCM code to D_R Measure $L_{S\pm}$	-0.6		0.6	dB
G_{RAGE}	Receive Gain Variation with programmed gain	Measure Earpiece Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAE, i.e. $G_{RAGE} = G_{actual} - G_{prog.} - G_{RAE}$	-0.5		0.5	dB
G_{RAGL}	Receive Gain Variation with programmed gain	Measure Loudspeaker Gain over the range from Maximum to minimum setting. Calculate the deviation from the programmed gain relative to GRAL, i.e. $G_{RAGL} = G_{actual} - G_{prog.} - G_{RAL}$	-1.0		1.0	dB
G_{RAT}	Receive Gain Variation with temperature	Measured relative to GRA. (LS and V_{Fr}) min. gain < GR < Max. gain	-0.1		0.1	dB
G_{RAV}	Receive Gain Variation with Supply	Measured relative to GRA. (LS and V_{Fr}) 4.75 < V_{CC} < 5.25V, GR = Max.	-0.05		0.05	dB
G_{RAF}	Receive Gain Variation with frequency (Earpiece or Loudspeaker)	Relative to 1015,625 Hz, multitone test technique used. min. gain < G_R < Max. gain f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 4000 Hz	 -0.3 -0.3 -0.8		 0.3 0.3 0.0 -14	 dB dB dB dB

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
G_{RAL}	Receive Gain Variation with signal level (Earpiece)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0.5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB
G_{RAL}	Receive Gain Variation with signal level (Loudspeaker)	Sinusoidal Test Method Reference Level = –10 dBm0 D_R = 0 dBm0 to +3 dBm0 D_R = -40 dBm0 to 0 dBm0 D_R = -50 dBm0 to -40 dBm0 D_R = -55 dBm0 to -50 dBm0	 -0.25 -0.25 -0,5 -1.5		 0.25 0.25 0.5 1.5	 dB dB dB dB

ENVELOPE DELAY DISTORTION WITH FREQUENCY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
DXA	Tx Delay, Absolute	f = 1600 Hz		320		µs
DXR	Tx Delay, Relative	f = 500 - 600 Hz f = 600 - 800 Hz f = 800 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		225 125 50 20 55 80 130		µs µs µs µs µs µs µs
DRA	Rx Delay, Absolute	f = 1600 Hz		252		µs
DRR	Rx Delay, Relative	f = 500 - 1000 Hz f = 1000 - 1600 Hz f = 1600 - 2600 Hz f = 2600 - 2800 Hz f = 2800 - 3000 Hz		10 30 105 135 185		µs µs µs µs µs

NOISE

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
NXC	Tx Noise, C weighted	V_{FxI} = 0V		16		dBrnC0
NXP	Tx Noise, P weighted	V_{FxI} = 0V		-70		dBm0p
NRC	Rx Noise, C weighted	Receive PCM code = Alternating Positive and Negative Code		18		dBrnC0
NRP	Rx Noise, P weighted	Receive PCM code = Positive Zero		-70		dBm0p
NRS	Noise, Single Frequency	V_{FxI} = 0V, Loop-around measurament from f = 0 Hz to 100 kHz		-50		dBm0
PPSRx	Positive PSRR, Tx	V_{FxI} = 0V, V_{CC} = 5.0 V_{DC} + 100 mV_{rms}; f = 0Hz to 50KHz	30			dB
PPSRp	Positive PSRR, Rx	PCM Code equals Positive Zero, V_{CC} = 5.0 VDC + 100 mVrms, measure $V_{Fr±}$ f = 0 Hz - 4 kHz f = 4 kHz - 50 kHz	30 30 30			dB dB dB
SOS	Spurious Out-Band signal at the output	DR input set to 0 dBm0 PCM code 300 - 3400 Hz Input PCM Code applied at DR 4600 Hz - 5600 Hz 5600 Hz - 7600 Hz 7600 Hz - 8400 Hz 8400 Hz - 100 kHz			 -40 -50 -50 -50	 dB dB dB dB

DISTORTION

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
S_{TDx} S_{TDr}	Signal to Total Distortion	Sinusoidal Test Methode (measured using C message weighting Filter) Level = 0 dBm0 to -30 dBm0 Level = -40 dBm0 Level = -45 dBm0	 36 29 24			 dBC dBC dBC
S_{DFx}	Single Frequency Distortion transmit	0 dBm0 input signal			-46	dB
S_{DFr}	Single Frequency Distortion receive	0 dBm0 input signal			-46	dB
IMD	Intermodulation	Loop-around measurament Voltage at VF_XI = -4 dBm0 to -21 dBm0, 2 Frequencies in the range 300 - 3400 Hz			-41	dB

CROSSTALK

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{Tx-r}	Transmit to Receive	Transmit Level = 0 dBm0, f = 300 - 3400 Hz DR = QuietPCM Code			-65	dB
C_{Tr-x}	Receive to Transmit	Receive Level = 0 dBm0, f = 300 - 3400 Hz VF_XI = 0V			-65	dB

SGS-THOMSON MICROELECTRONICS

GS1T70-D540

ISDN DC-DC CONVERTER

PRELIMINARY DATA

FEATURES

- Wide input voltage range: 25V to 115V
- Peak input overvoltage withstand: 1kV for 1.2/50µs
- Peak overvoltage withstand on Output 2 (40V): 250V for 10/700µs
- Positive or negative input voltage polarity
- High efficiency (80% min., 85% typ. at max. load)
- Input and output filtering
- Short-circuit protection on both outputs
- Input power during shortcircuit within specification
- Minimum current drain during stand-by condition: 10µA for Vi < 18V
- Input-output isolation voltage: 4000V 10/700µs pulse
- Output1-output2 isolation voltage: 2000V 10/700µs pulse
- Mechanical dimensions (L x W x H): 50.8mm x 50.8mm x 18mm (2"x 2"x 0.71")

DESCRIPTION

The **GS1T70-D540** converter has been designed for the "U" interface of an ISDN-NTBA (Network Termination Basic Access) system with either **4B3T** or **2B1Q** standard trasmission.

It meets the requirements of the following specifications:

EN 60950

CCITT I.430

CCITT G.960

CCITT G.961

ETS 300 002

ETS 300 012

ETS 300 047 (ISDN BASIC ACCESS, Safety and Protection).

Two isolated outputs, 5V/90mA and 40V/420mW are supplied. The converter offers short-circuit protection (short-circuit on 40V output doesn't affect 5V output and the input power never exceeds the limit of the specification), input either voltage polarity, 80% minimum efficiency at maximum load, input and output filtering to meet very stringent noise requirements.

The input and the output 2 (40V) stages are protected against differential overvoltage up to 1kV (1.2/50µs) and 250V (10/700µs) respectively. When the input voltage is below 18V, the converter offers a very high input impedance and a maximum quiescent current of 10µA.

These features allow the converter to operate directly connected to the telephone line without any external components.

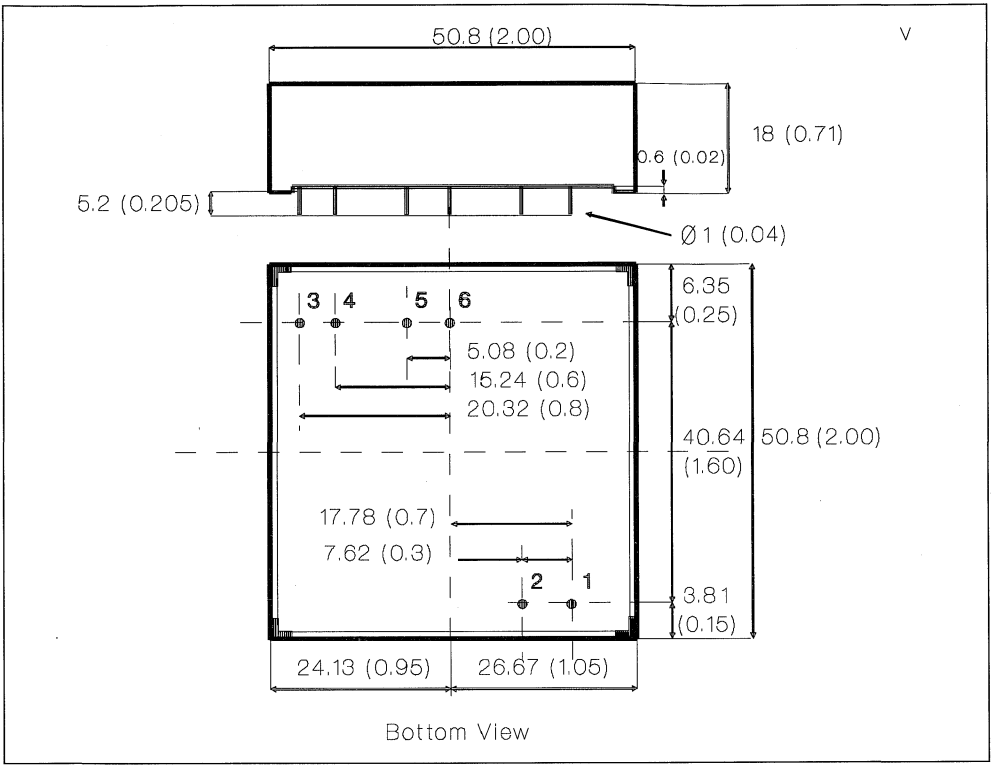
In addition, the wide operating input voltage range (25 to 115V) allows it to operate within the whole range of **LT** (Line Termination) battery voltage and its relevant line resistance.

4000V (10/700µs pulse) and 2000V (10/700µs pulse) isolation voltages are provided between input to outputs and between outputs respectively.

ELECTRICAL CHARACTERISTICS (Tamb.= 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Vi	Input Voltage	Vo1= 5V Po1= 10 to 450mW Vo2= 40V Po2= 0 to 420mW	25		115	V
Vipk	Input Transient Overvoltage	t= 1.2/50s (pulse)			1	kV
Vist	Start Up Input Voltage	See fig.2	28		44	V
Vo1	Output Voltage 1	Vi= 25 to 115V Po1= 10 to 450mW Po2= 0 to 420mW	4.75	5	5.25	V
Vo2	Output voltage 2	Vi= 25 to 115V Po1= 10 to 450mW Po2= 0 to 420mW	34	40	42	V
Vor1	Output Ripple Voltage 1	Vi= 25 to 115V Full Load BW= 0 to 20MHz		5	20	mVpp
Vor2	Output Ripple Voltage 2	Vi= 25 to 115V Full Load BW= 0 to 20MHz		10	30	mVpp
eN	Differential Input Noise Voltage	Vi= 25 to 115V Full Load BW= 0 to 20MHz		10	30	mVpp
Io1	Output Current 1	Vi= 25 to 115V Vo1= 5V Po2= 0 to 420mW	2		90	mA
Io1l	Output Current 1 Limit Initiation	Vi= 25 to 115V Vo1= 4.75 to 5.25V	110		130	mA
Io2	Output Current 2	Vi= 25 to 115V Vo2= 40V Po1= 10 to 450mW	0		10.5	mA
Iosc2	Output 2 Shortcircuit Current	Vi= 25 to 115V Output Shorted (Indefinite time)	9		14	mA
η	Efficiency	Vi= 70V Po1= 450mW Po2= 420mW	80	85		%
th	Hold Up Time on Output 1 [5V]	Vi= 115 to 0V Po1= 380mW Po2= 420mW		90		ms
		Vi= 115 to 0V Po1= 50mW Po2= 0mW		700		
Vis	Isolation Voltage	Input to Output 1 Input to Output 2 pulse= 10/700µs	4000			V
Vis	Isolation Voltage (pulse)	Output 1 to Output 2 pulse= 10/700µs	2000			V
Tstg	Storage Temperature Range		–40		+85	°C
Top	Operating Temperature Range		–20		+70	°C

CONNECTION DIAGRAM AND MECHANICAL DATA



Dimension in mm (inches)

PIN DESCRIPTION

PIN	FUNCTION
1	Input (25 to 115V, either polarity)
2	Input (25 to 115V, either polarity)
3	+5V Output
4	Return for +5V Output
5	+40V Output
6	Return for +40V Output

OUTPUT POWER CHARACTERIZATION - Maximum Input Power 800mW

LT (Line Termination) Battery Voltage = 44V to 71V Rs (Line Resistance) = 600Ω				LT (Line Termination) = 51V to 69V Rs (Line Resistance) = 750Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
800	Actived Emergency	240	420	800	Actived Emergency	240	420
350	Emergency	267	0	350	Actived	267	0
120	Deactived Emergency	41	47	120	Deactived Emergency	40	47
50	Deactived	28	0	50	Deactived	24	0

LT (Line Termination) Battery Voltage = 68V to 72V Rs (Line Resistance) = 1400Ω				LT (Line Termination) = 91V to 99V Rs (Line Resistance) = 2500Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
800	Actived Emergency	240	420	800	Actived Emergency	240	420
350	Emergency	270	0	350	Actived	256	0
120	Deactived Emergency	38	47	120	Deactived Emergency	36	47
50	Deactived	24	0	50	Deactived	24	0

LT (Line Termination) Battery Voltage = 80V to 115V Rs (Line Resistance) = 1800Ω				LT (Line Termination) = 105V to 115V Rs (Line Resistance) = 3100Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
800	Actived Emergency	240	420	800	Actived Emergency	240	420
350	Emergency	270	0	350	Actived	255	0
120	Deactived Emergency	37	47	120	Deactived Emergency	30	47
50	Deactived	24	0	50	Deactived	24	0

OUTPUT POWER CHARACTERIZATION - Maximum Input Power 950mW

LT (Line Termination) Battery Voltage = 44V to 71V Rs (Line Resistance) = 510Ω				LT (Line Termination) = 51V to 69V Rs (Line Resistance) = 680Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
950	Actived Emergency	360	420	950	Actived Emergency	360	420
450	Emergency	345	0	450	Actived	345	0
180	Deactived Emergency	93	47	180	Deactived Emergency	94	47
90	Deactived	61	0	90	Deactived	62	0

LT (Line Termination) Battery Voltage = 68V to 72V Rs (Line Resistance) = 1200Ω				LT (Line Termination) = 91V to 99V Rs (Line Resistance) = 2050Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
950	Actived Emergency	370	420	950	Actived Emergency	370	420
450	Emergency	350	0	450	Actived	340	0
180	Deactived Emergency	82	47	180	Deactived Emergency	75	47
90	Deactived	58	0	90	Deactived	45	0

LT (Line Termination) Battery Voltage = 80V to 115V Rs (Line Resistance) = 1500Ω				LT (Line Termination) = 105V to 115V Rs (Line Resistance) = 2085Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
950	Actived Emergency	370	420	950	Actived Emergency	370	420
450	Emergency	351	0	450	Actived	340	0
180	Deactived Emergency	80	47	180	Deactived Emergency	70	47
90	Deactived	52	0	90	Deactived	43	0

OUTPUT POWER CHARACTERIZATION - Maximum Input Power 1000mW

LT (Line Termination) Battery Voltage = 80V to 115V Rs (Line Resistance) = 1500Ω				LT (Line Termination) = 105V to 115V Rs (Line Resistance) = 2085Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1000	Actived Emergency	380	420	1000	Actived Emergency	380	420
450	Emergency	348	0	450	Actived	348	0
180	Deactived Emergency	92	47	180	Deactived Emergency	94	47
100	Deactived	68	0	100	Deactived	68	0

LT (Line Termination) Battery Voltage = 68V to 72V Rs (Line Resistance) = 1150Ω				LT (Line Termination) = 91V to 99V Rs (Line Resistance) = 2000Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1000	Actived Emergency	380	420	1000	Actived Emergency	380	420
450	Emergency	340	0	450	Actived	340	0
180	Deactived Emergency	89	47	180	Deactived Emergency	75	47
100	Deactived	67	0	100	Deactived	56	0

LT (Line Termination) Battery Voltage = 80V to 115V Rs (Line Resistance) = 1450Ω				LT (Line Termination) = 105V to 115V Rs (Line Resistance) = 2800Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1000	Actived Emergency	380	420	1000	Actived Emergency	380	420
450	Emergency	345	0	450	Actived	340	0
180	Deactived Emergency	80	47	180	Deactived Emergency	70	47
100	Deactived	60	0	100	Deactived	52	0

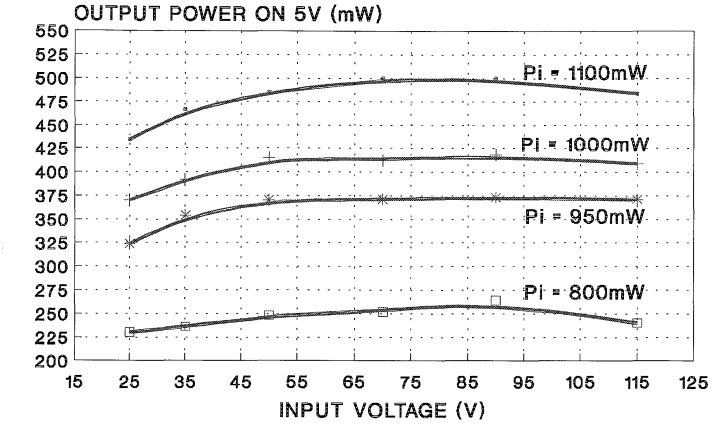
OUTPUT POWER CHARACTERIZATION - Maximum Input Power 1100mW

LT (Line Termination) Battery Voltage = 44V to 71V Rs (Line Resistance) = 430Ω				LT (Line Termination) = 51V to 69V Rs (Line Resistance) = 600Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1100	Actived Emergency	450	420	1100	Actived Emergency	450	420
600	Emergency	456	0	600	Actived	456	0
180	Deactived Emergency	92	47	180	Deactived Emergency	92	47
90	Deactived	61	0	90	Deactived	62	0

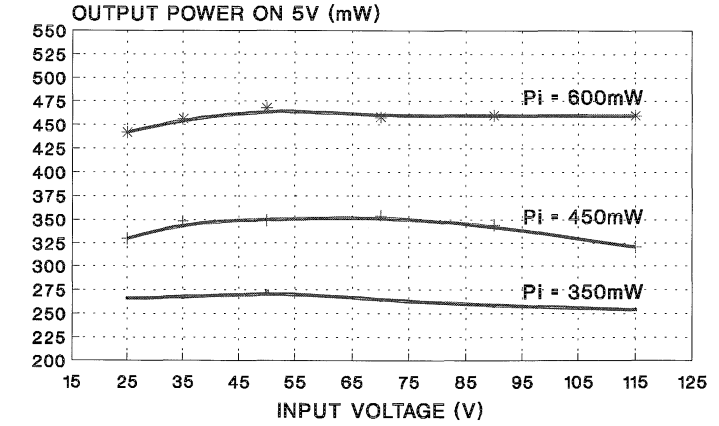
LT (Line Termination) Battery Voltage = 68V to 72V Rs (Line Resistance) = 1050Ω				LT (Line Termination) = 91V to 99V Rs (Line Resistance) = 1800Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1100	Actived Emergency	450	420	1100	Actived Emergency	450	420
600	Emergency	480	0	600	Actived	460	0
180	Deactived Emergency	90	47	180	Deactived Emergency	77	47
90	Deactived	59	0	90	Deactived	45	0

LT (Line Termination) Battery Voltage = 80V to 115V Rs (Line Resistance) = 1350Ω				LT (Line Termination) = 105V to 115V Rs (Line Resistance) = 2450Ω			
Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]	Input Power (mW)	NT Status	Output Power 1 (5V) [mW]	Output Power 2 (40V) [mW]
1100	Actived Emergency	450	420	1100	Actived Emergency	450	420
600	Emergency	458	0	600	Actived	457	0
180	Deactived Emergency	80	47	180	Deactived Emergency	70	47
90	Deactived	52	0	90	Deactived	40	0

OUTPUT POWER CHARACTERIZATION vs NT (Network Termination) STATUS



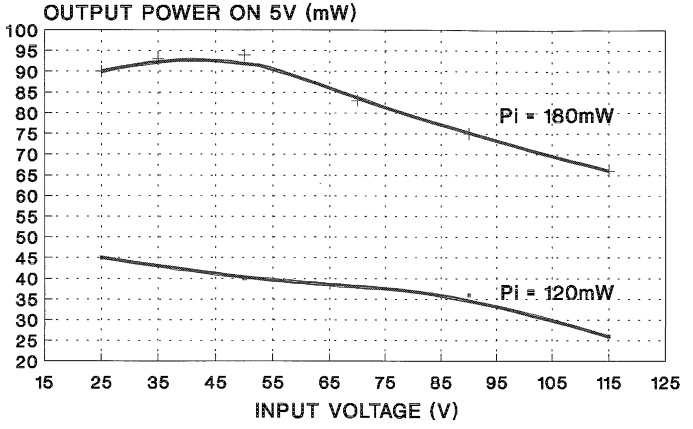
OUTPUT POWER ON 40V = 420mW
LINE RESISTANCE (Rs) = 0 ohm



OUTPUT POWER ON 40V = 0mW
LINE RESISTANCE (Rs) = 0 ohm

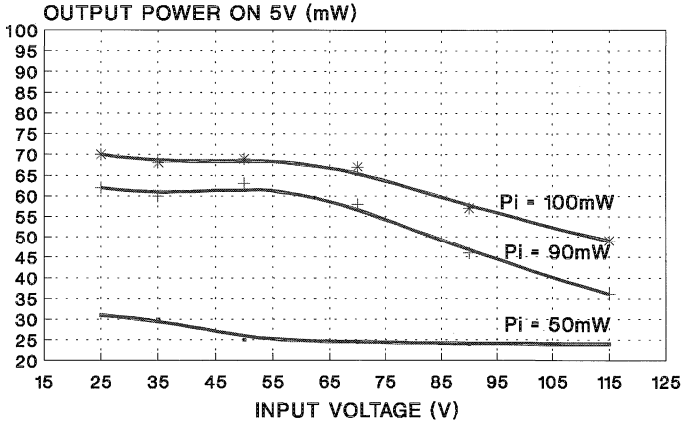
OUTPUT POWER CHARACTERIZATION vs NT (Network Termination) STATUS (Continued)

NT Status = DEACTIVED EMERGENCY
INPUT POWER = 120 to 180mW



OUTPUT POWER ON 40V = 47mW
LINE RESISTANCE (Rs) = 0 ohm

NT Status = DEACTIVED
INPUT POWER = 50 to 100mW



OUTPUT POWER ON 40V = 0mW
LINE RESISTANCE (Rs) = 0 ohm

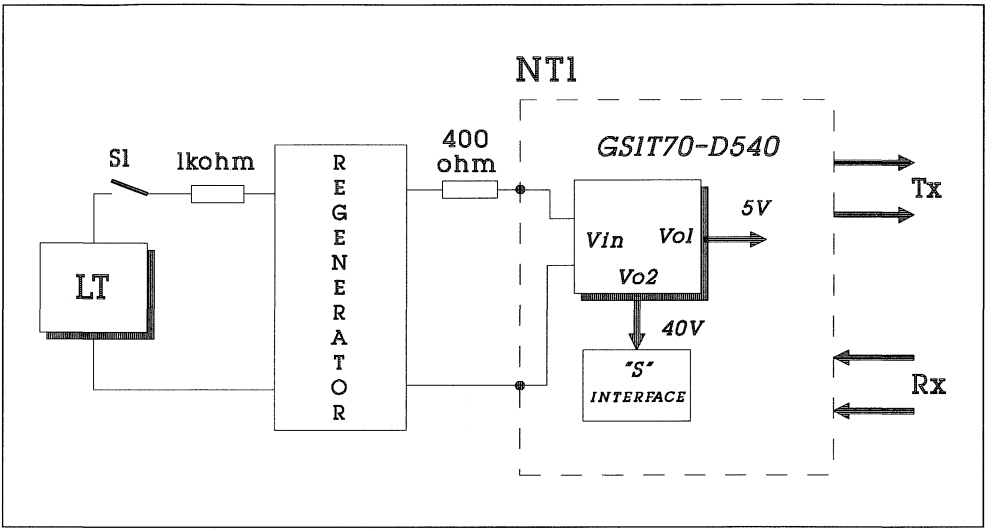
START-UP BEHAVIOUR

Start-Up Test

The converter is able to operate with very long telephone line according to Fig. 1.

Test conditions:
LT Voltage : 92V
Stimulus : Switch on S1
Results : after t= 5s 4.75V ≤ Vo1 [5V] ≤ 5.25V
34V ≤ Vo2 [40V] ≤ 42V

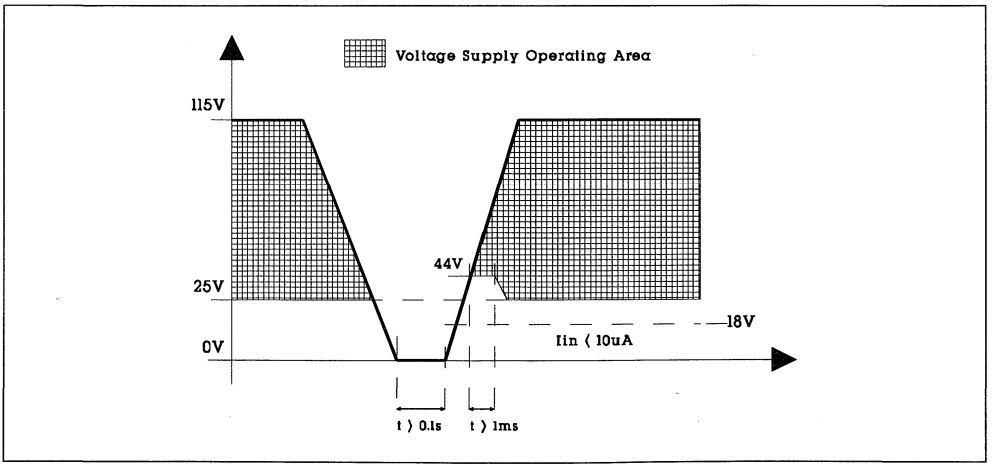
Fig. 1



Voltage Supply Operating Area

Fig. 2 shows the Voltage Supply Operating area during a switching OFF-ON sequence. The start-up voltage is 44V maximum. When the input voltage is below 18V the maximum quiescent currentis lower than 10mA.

Fig. 2



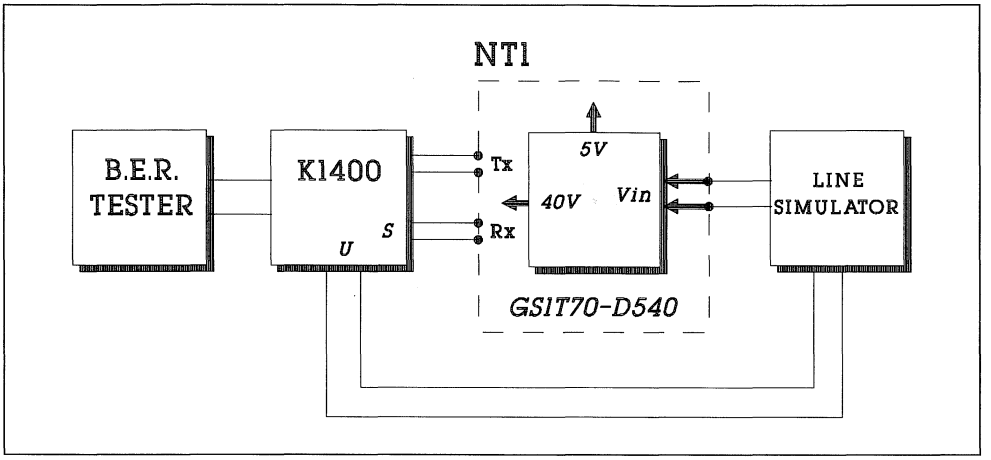
Bit Error Ratio Test

No one bit errors have been detected according to the set-up of Fig. 3.

Test conditions:

NT Status : Actived
Stimulus : pseudocasual
B.E.R. Tester : HP 3780
Line Simulator : DLS 100
Simulator : K1400 Siemens

Fig. 3



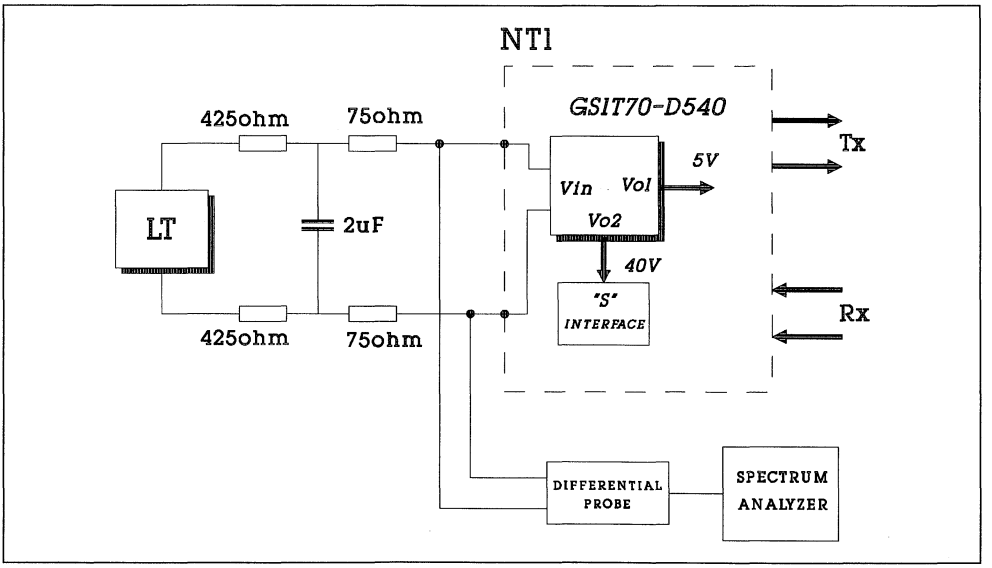
Noise Injected on the "U" Interface

The noise injected on the "U" interface is less than 1mVRMS according to the test set-up of Fig. 4.

Test conditions:

NT Status : Deactived
Stimulus : None

Fig. 4



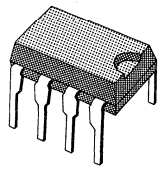
TRIBALANCED PROTECTION FOR ISDN INTERFACES

PRELIMINARY DATASHEET

DESCRIPTION

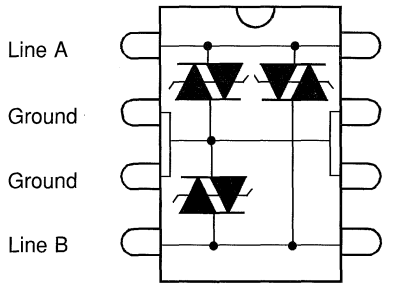
TRIBALANCED PROTECTION

- Dedicated devices for ISDN interfaces and high speed data telecom lines protection.
- It's a tripolar TRISIL with low capacitance providing :
  - Low capacitances from lines to ground : allowing high speed transmission without signal attenuation.
  - Good capacitance balance (Line A / Line B) in order to insure the longitudinal balance of the line.
  - Fixed breakdown voltage in both common and differential modes.
  - The same surge current capability in both common and differential modes.
- Breakdown voltage :
  - TPI80 : V_{BR} = 80V
  - TPI120 : V_{BR} = 120V



DIL 8
(Plastic)

SCHEMATIC DIAGRAM



IN ACCORDANCE WITH FOLLOWING STANDARDS :

CCITT K17 - K20	10/700 µs	1.5 kV
	5/310 µs	38 A
VDE 0433	10/700 µs	2 kV
	5/200 µs	50 A
CNET	0.5/700 µs	1.5 kV
	0.2/310 µs	38 A

ABSOLUTE RATINGS (limiting values) (- 40°C < Ta < + 85°C)

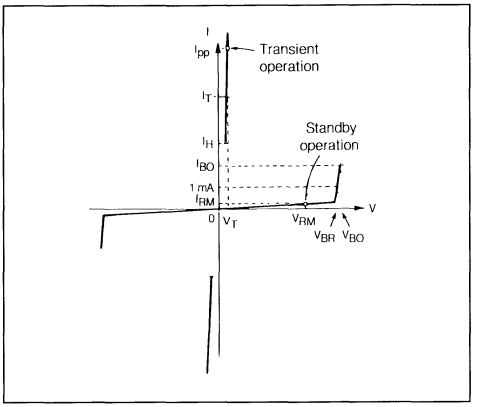
Symbol	Parameter		Values	Unit
I_{PP}	Peak Pulse Current	10/1000 µs 5/320 µs 2/10 µs	30 40 90	A
I_{TSM}	Non Repetitive Peak on-state Current F = 50 Hz	t = 1 s t = 10 ms	3.5 5	A
T_{stg} T_j	Storage and Junction Temperature Range		- 55 to + 150 150	°C

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
Rth (j-l)	Junction-leads thermal resistance	125	°C/W

ELECTRICAL CHARACTERISTICS

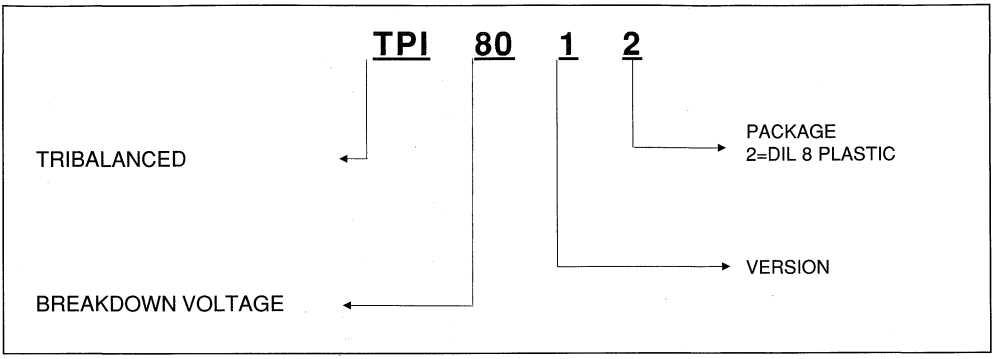
Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{BO}	Breakover voltage
I_H	Holding current
V_T	On-state voltage
I_{BO}	Breakover current
I_{PP}	Peak pulse current



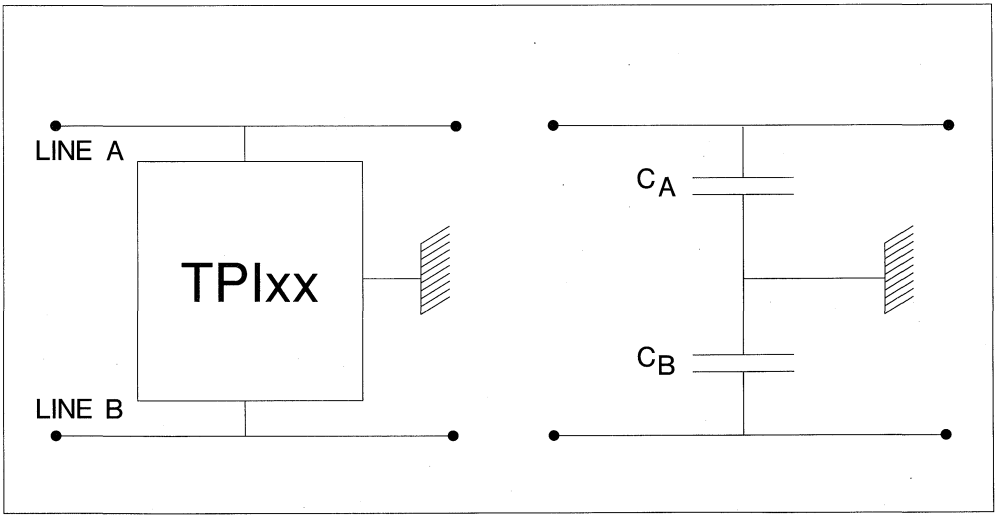
Types	I_{RM} @ V_R		V_{BR} @ I_R		V_{BO} tp=10ms	I_{BO} tp=10ms	I_H I_T=2A tp=10ms
	max		min		max	max	min
	µA	V	V	mA	V	mA	mA
TPI80	10	70	80	1	120	800	150
TPI120	10	105	120	1	180	800	150

All parameters tested at 25°C, except where indicated

ORDER CODE



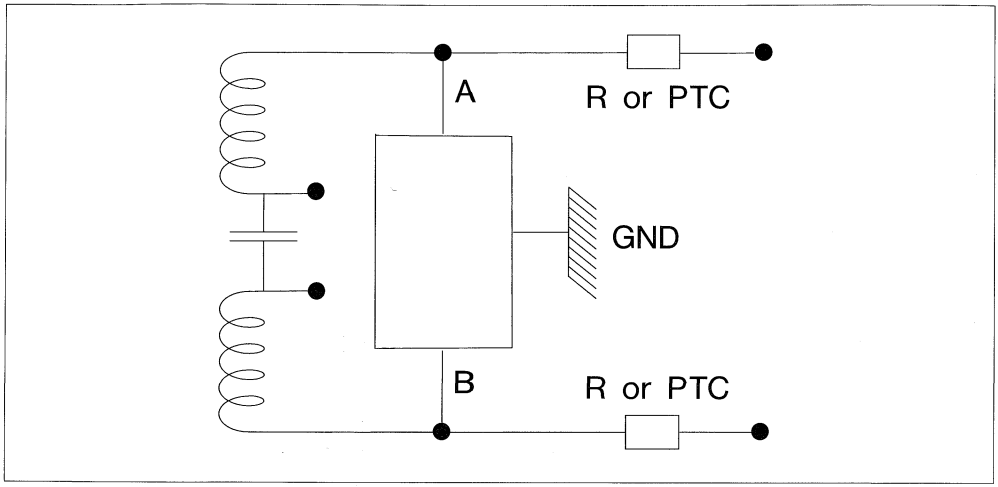
CAPACITANCE CHARACTERISTICS



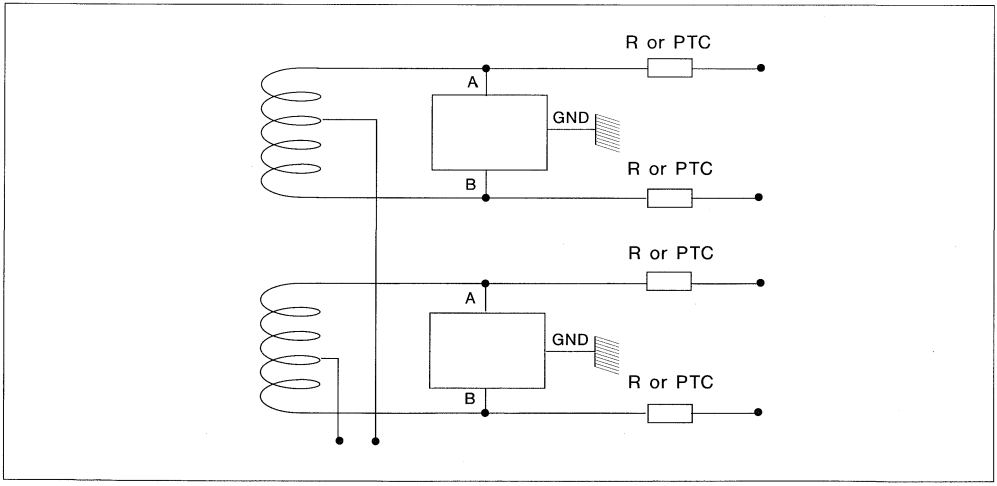
CONFIGURATION	C_A	C_B	$C_A - C_B$
	pf	pf	pf
	max	max	max
V_A = 0 V V_B = -56 V	50	70	20
V_A = -56 V V_B = 0 V	70	50	20

PROTECTION FUNCTION

U INTERFACE PROTECTION



S INTERFACE PROTECTION



This component use an internal diagram which permits to have symetrical characteristics with a good balanced behaviour.
This topology assumes the same fire level in positive and negative for differential or common mode surge.

DATACOM DATASHEETS

MK5021
SERIAL COMMUNICATIONS CONTROLLER

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SECTION 1: INTRODUCTION

The SGS - Thomson Serial Communications Controller (MK5021) is a VLSI semiconductor device which provides high speed synchronous serial data communications control for protocols using HDLC framing. The MK5021 will perform frame formating including: frame delimiting with flags, transparency (so-called "bit-stuffing"), FCS (CRC) generation and detection.

One of the outstanding features of the MK5021 is its buffer management which includes on-chip dual channel DMA. This feature allows users to receive and transmit multiple data frames at a time. (A conventional serial communications control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK5021 will move multiple blocks of receive and transmit data directily into and out of memory through the Host's bus. A possible system configuration for the MK5021 is shown in figure 1.

The MK5021 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI- 11, 8086, 8088, 8080, etc.

The MK5021 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins. All signal pins on the MK5021 are TTL compatible. This has the advantage of making the MK5021 independent of the physical interface. As shown in figure 1, line drivers and receivers are used for electrical connection to the physical layer.

SECTION 2: FEATURES

- CMOS
- Fully compatible with both 8 or 16 bit systems.
- System clock rate to 10 MHz.
- Data rate up to 7 Mbps.
- Implements HDLC (ADCCP) type frame formating.
- Frame formatting compatible with X.25, X.32, X.75, LAPB, ISDN LAPD, SS7, SDLC and more.
- Available in 52 PLCC.
- Pin compatible and architecturally the same as MK5025 (X.25/LAPD), MK5027 (CCS#7) and MK5029 (SDLC).
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- On chip DMA control with programmable burst length.
- Handles all HDLC frame formatting:
  - Zero bit insert and delete
  - FCS (CRC) generation and detection
  - Frame delimiting with flags
- Programmable minimum frame spacing on transmission (number of flags between frames).
- Selectable FCS (CRC) of 16 or 32 bits.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- All inputs and outputs are TTL compatible
- Programmable for full or half duplex operation

SECTION 3: OPERATIONAL DESCRIPTION

The SGS - Thomson Serial Communications Controller (MK5021) device is a VLSI product intended for high performance data communication applications requiring HDLC framing. The MK5021 will perform all frame formatting, such as: frame delimiting with flags, FCS (CRC) generation and detection, and zero bit insertion and deletion for transparency. The MK5021 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit.

The MK5021 can be used with any popular 16 or 8 bit microprocessor, such as the possible system configuration for the MK5021 as shown in figure 1.

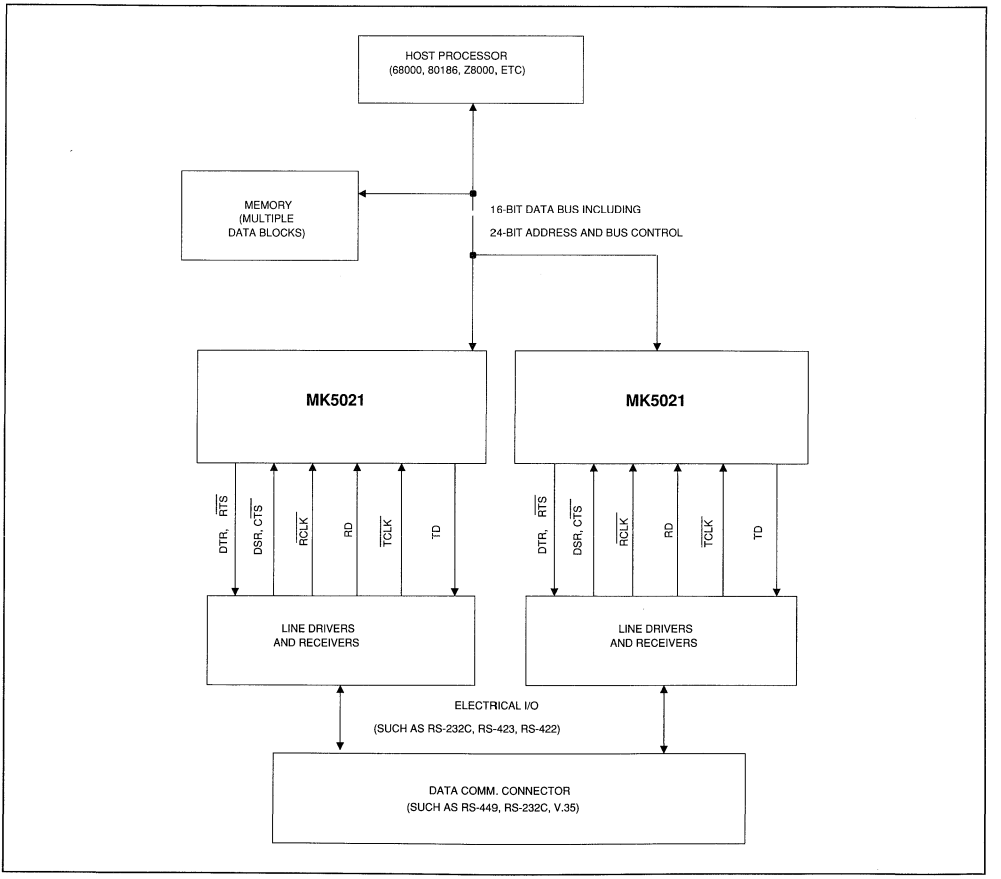
This document assumes that the processor has a byte addressable memory organization.

The MK5021 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. An I/O acceleration processor, could be used to off-load Network Level software from the Host.

The MK5021 may be operated in full or half duplex mode. In half duplex mode the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK5021 are TTL compatible. This has the advantage of making the MK5021 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

Figure 1: Possible System Configuration For The MK5021



3.1 Functional Blocks

Refer to the block diagram in Figure 2.

The MK5021 is primarily initialized and controlled through six 16-bit Control and Status Registers (CSR0 thru CSR5). The CSR's are accessed through two bus addressable ports, the Register Address Port (RAP), and the Register Data Port (RDP). The MK5021 may also generate an interrupt(s) to the Host. These interrupts are enabled and disabled through CSR0.
The on-chip microcontroller is used to control the movement of parallel receive and transmit data, and to handle the Address and Control field filtering.

3.1.1 Microcontroller

The microcontroller controls all of the other blocks of the MK5021. All frame processing and generation is performed by the microcontroller. All primitive processing and generation is also done here. The microcode ROM contains the control program of the microcontroller.

3.1.2 Receiver

Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (CRC).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver Over-Run.
7. Odd byte detection.

NOTE: If frames are received that have an odd number of bytes then the last byte of the frame is said to be an odd byte.

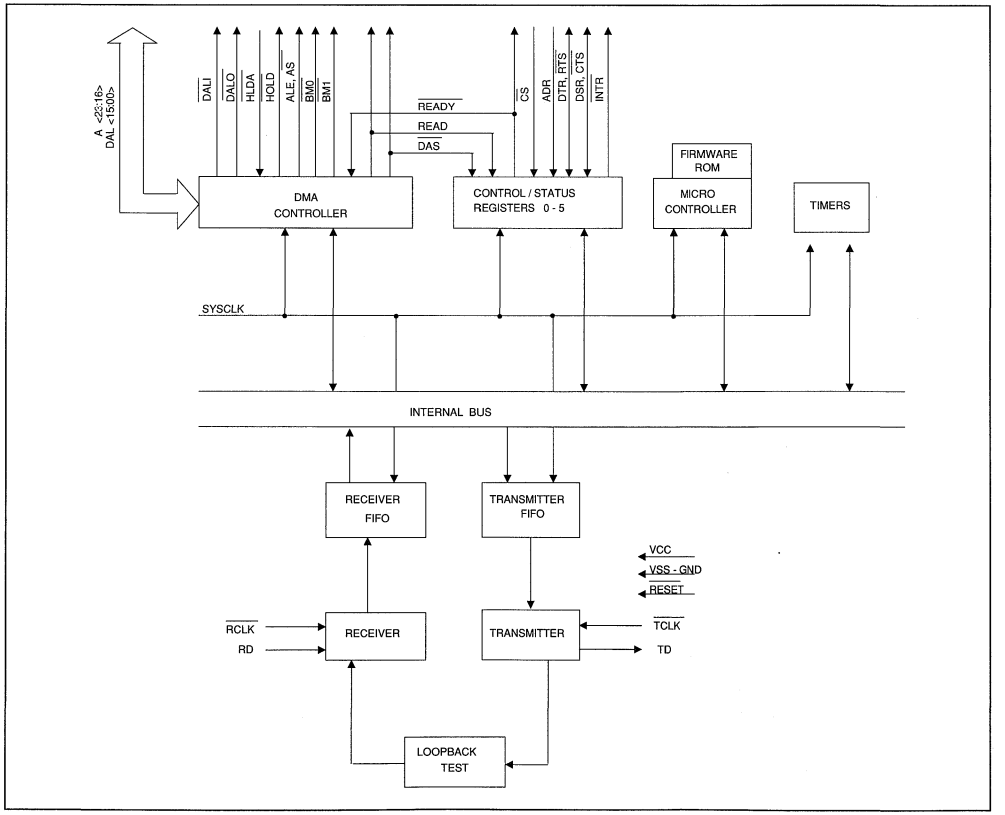
8. Detection of non-octet aligned frames, such frames are treated as invalid signal units.

3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.

Figure 2 : MK5021 Simplified Block Diagram



2. Generating and appending the FCS (CRC).
3. Framing outgoing frame with flags.
4. Zero bit insertion for transparency.
5. Transmitter Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS control.

3.1.4 Frame Check Sequence or Cyclic Redundancy Check

The FCS (CRC) on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynomial 16 bit:
$X^{16} + X^{12} + X^5 + 1$

Remainder 16 bit (if received correctly):
High order bit-->0001 1101 0000 1111

Polynomial 32 bit:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

Remainder 32 bit (if received correctly):
high order bit-->1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 2 bytes; 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmabiliy , along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK5021 must use the host bus. For more information, see Control/Status Register 4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK5021 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK5021. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to burst read data from the host's memory buffers; making both the MK5021 and the host bus more efficient.

3.1.7 DMA Controller

The MK5021 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK5021 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK5021 will begin transferring data to or from memory. The MK5021 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the $\overline{\text{BUSREL}}$ pin is driven low. In any case, it will complete all bus transfers before releasing bus mastership back to the host. If during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK5021 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode,it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed separately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on control status register 4.

3.1.8 Bus Slave Circuitry

The MK5021 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave.
The contents of these registers are listed in Section 4 and bus signal timing is described in Figures 9 and 10.

3.2 Buffer Management Overview

Refer to Fig. 3.

3.2.1 Initalization Block

Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 28 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST, and is accessed by the MK5021 during initialization. The Initialization Block is comprised of:

A. Mode of Operation.

B. Frame Address Values.

C. Counter/Timer Preset Values.

D. Location and size of Receive and Transmit Descriptor Rings.

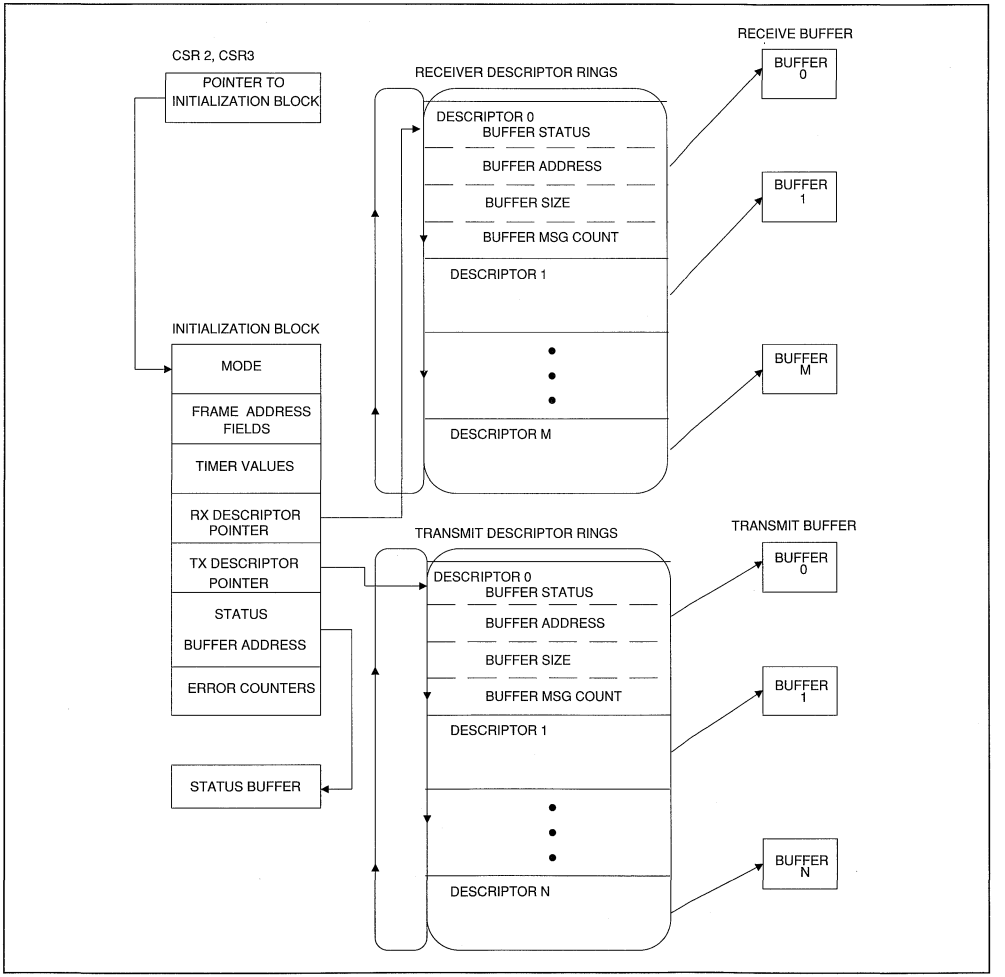
E. Location of status buffer.

F. Error Counter

3.2.2 The Circular Queue

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128

Figure 3 : MK5021 Buffer Management



buffers may be queued-up on a descriptor ring awaiting execution by the MK5021. The descriptor ring has a descriptor assigned to each buffer. Each descriptor holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each descriptor also contains two control bits called OWNA and OWNB, which denote whether the MK5021, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5021 owns the buffer, the MK5021 is allowed and commanded to transmit the buffer. When the MK5021 does not own the buffer, it will not transmit that buffer. For receive, when the MK5021 owns a buffer, it may place received data into that buffer.
Conversely, when the MK5021 does not own a receive buffer, it will not place received data into that buffer.

The MK5021 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5021 tests the next descriptor in the descriptor ring in a "look ahead" manner. If the frame is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK5021 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.
The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, protocol parameters, etc. The starting address for the Initialization block, IADR, is defined in the CSR2 and CSR3 registers inside the MK5021.

3.2.3 Frame Format

The frame format supported by the MK5021 is shown below. Each frame may consist of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field, an FCS (CRC) of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags transmitted is programmable through the Mode Register in the Initialization Block. Received frames may have only one flag between adjacent frames.

F	A	C	INFO	FCS	F
8	8/16	8/16	8*n	16/32	8

3.3 PIN CONNECTION

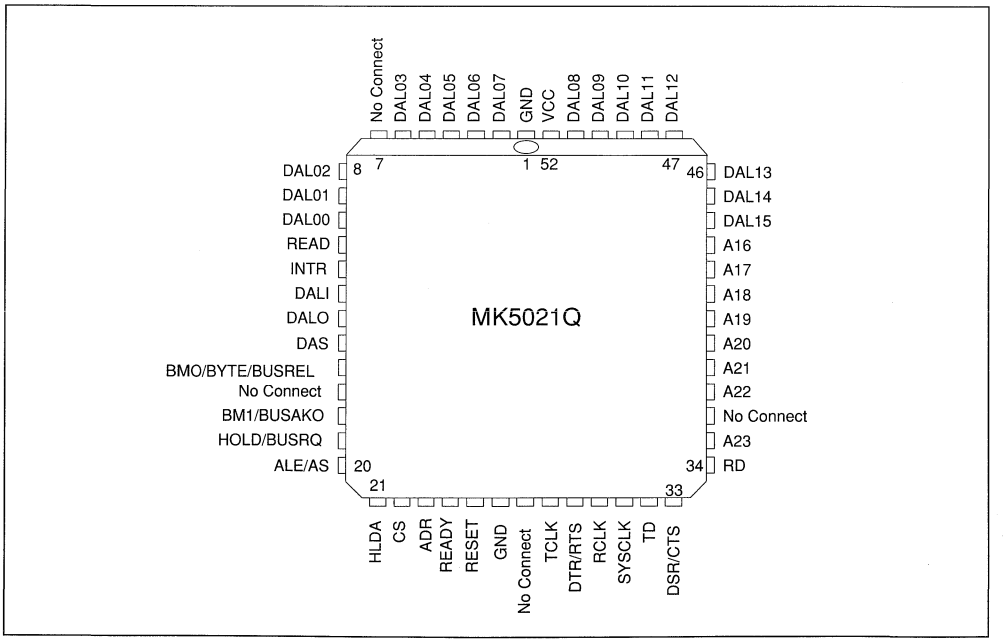


TABLE 1 - PIN DESCRIPTION

LEGEND:

I	Input only	O	Output only
IO	Input / Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Note: Pin out shows is for 52 pin PLCC.

Signal Name	Pin(s)	Type	Description
DAL<15:00>	2-10 44-51	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	11	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5021 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK5021 as a Bus Slave : READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK5021 as a Bus Master : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
$\overline{\text{INTR}}$	12	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.DAL IN is an external bus transceiver control line.
$\overline{\text{DALI}}$	13	O/3S	DALI is driven by the MK5021 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK5021 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.
$\overline{\text{DALO}}$	14	O/3S	DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5021 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by the MK5021 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{\text{DAS}}$	15	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. This signal is driven by the MK5021 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
$\overline{\text{BMO}}$ BYTE $\overline{\text{BUSREL}}$	16	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5021 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16

TABLE 1 - PIN DESCRIPTION CONTINUED

Signal Name	Pin(s)	Type	Description
$\overline{BM1}$ $\overline{BUSAKO}$	18	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = $\overline{BMO}$ (O/3S) I/O PIN 16 = $\overline{BM1}$ (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. MK5021 drives these lines only as a Bus Master. MK5021 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. $\overline{BM1}$ $\overline{BM0}$ TYPE OF TRANSFERLOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE If CSR4<00> BCON = 1, I/O PIN 15 = $\overline{BYTE}$ (O/3S) I/O PIN 16 = $\overline{BUSAKO}$ (O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5021 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE $\overline{BUSAKO}$ is a bus request daisy chain output. If MK5021 is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If MK5021 is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high. Note: All transfers are entire word unless the MK5021 is configured for 8 bit operation.
$\overline{HOLD}$ $\overline{BUSRQ}$	19	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0, I/O PIN 17 = $\overline{HOLD}$ $\overline{HOLD}$ request is asserted by MK5021 when it requires a DMA cycle, if $\overline{HLDA}$ is inactive, regardless of the previous state of the $\overline{HOLD}$ pin. $\overline{HOLD}$ is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1, I/O PIN 17 = $\overline{BUSRQ}$ $\overline{BUSRQ}$ is asserted by MK5021 when it requires a DMA cycle if the prior state of the $\overline{BUSRQ}$ pin was high and $\overline{HLDA}$ is inactive. $\overline{BUSRQ}$ is held low for the entire ensuing bus transaction.

TABLE 1 - PIN DESCRIPTION CONTINUED

Signal Name	Pin(s)	Type	Description
ALE $\overline{AS}$	20	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK5021 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = $\overline{AS}$ As $\overline{AS}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{AS}$ can be used by a slave device to strobe the address into a register. $\overline{AS}$ is effectively the inversion of ALE.
$\overline{HLDA}$	21	I	HOLD ACKNOWLEDGE is the response to $\overline{HOLD}$. When $\overline{HLDA}$ is low in response to MK5021's assertion of $\overline{HOLD}$, the MK5021 is the Bus Master. $\overline{HLDA}$ should be deasserted ONLY after $\overline{HOLD}$ has been released by the MK5021.
$\overline{CS}$	22	I	CHIP SELECT indicates, when low, that the MK5021 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	23	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
$\overline{READY}$	24	IO/OD	When the MK5021 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, the MK5021 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be released after $\overline{DAS}$ or $\overline{CS}$ is negated.
$\overline{RESET}$	25	I	$\overline{RESET}$ is the Bus signal that will cause MK5021 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.

TABLE 1 - PIN DESCRIPTION CONTINUED

Signal Name	Pin(s)	Type	Description
$\overline{\text{TCLK}}$	28	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of $\overline{\text{TCLK}}$. The frequency of $\overline{\text{TCLK}}$ may not be greater than the frequency of SYSCLK.
DTR $\overline{\text{RTS}}$	29	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{\text{RTS}}$ or as programmable IO pin DTR. If configured as $\overline{\text{RTS}}$, the MK5021 will assert this pin if it has data to send and throughout the transmission of a signal unit.
$\overline{\text{RCLK}}$	30	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of $\overline{\text{RCLK}}$. The frequency of $\overline{\text{RCLK}}$ may not be greater than the frequency of SYSCLK.
SYSCLK	31	I	SYSTEM CLOCK. System clock used for internal timing of the MK5021. SYSCLK should be a square wave, of frequency up to 10 MHz.TRANSMIT DATA.
TD	32	O	Transmit serial data output.
DSR $\overline{\text{CTS}}$	33	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{\text{CTS}}$ or as programmable IO pin DSR. If configured as $\overline{\text{CTS}}$, the MK5021 will transmit all ones while $\overline{\text{CTS}}$ is high.
RD	34	I	RECEIVE DATA. Received serial data input.
A<23:16>	37-43	O/3S	Address bits <23:16> used in conjuction with DAL<15:00> to produce a 24 bit address. MK5021 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4<7> BAE bit.
VSS-GND	1,26		Ground Pins
VCC	52		Power Supply Pin +5.0 VDC + - 5%

SECTION 4: PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK5021.

4.1 Control and Status Registers

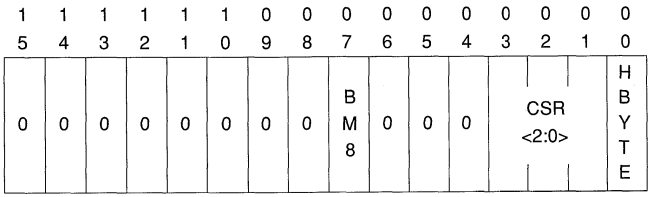
There are six Control and Status Registers (CSR's) resident within the MK5021. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP), thus requiring only two locations in the system memory or I/O map.

4.1.1 Accessing the Control and Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten or upon a bus reset. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

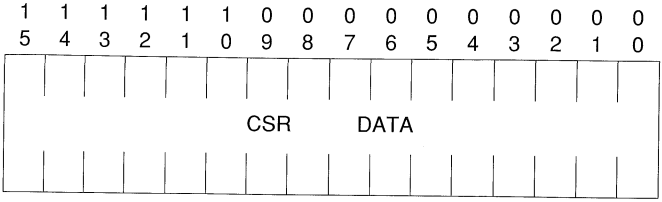
ADR	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

4.1.1.1 Register Address Port (RAP)



BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes.
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit transfers; this provides compatibility with 8 bit-microprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
6:04	RESERVED	Must be written as zeroes.
03:01	CSR<2:0>	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR<2:0> — CSR 0 — CSR0 1 — CSR1 2 — CSR2 3 — CSR3 4 — CSR4 5 — CSR5
00	HBYTE	Determines which byte is addressed for 8 bit mode. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful in 8 bit mode and must be written as zero if BM8=0. HBYTE READ/WRITE and cleared on bus reset.

4.1.1.2 Registers Data Port (RDP)



BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TDMD	STOP	DTX	DRX	TXON	RXON	INEA	INTR	MERR	MISS	ROR	TUR	PINT	TINT	RINT	0

BIT	NAME	DESCRIPTION
15	TDMD	TRANSMIT DEMAND, when set, causes MK5021 to access the Transmit Descriptor Ring without waiting for the transmit polltime interval to elapse. TDMD need not be set to transmit a frame, it merely hastens MK5021's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is Write With ONE ONLY and cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.
14	STOP	STOP, when set, indicates that MK5021 is operating in the Stopped phase of operation. All external activity is disabled and internal logic is reset. MK5021 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.
13	DTX	Transmitter ring disable prevents the MK5021 from further access to the Transmitter Descriptor Ring and terminates transmitter polling. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. TXON acknowledges changes to DTX, see below. DTX is READ/WRITE.
12	DRX	Disable the Receiver prevents the MK5021 from further access to the Receiver Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. RXON acknowledges changes to DRX, see below. DRX is READ/WRITE.
11	TXON	TRANSMITTER ON indicates that the transmit ring access is enabled. TXON is set as the Start primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing to this bit has no effect.

10	RXON	RECEIVER ON indicates that the receive ring access is enabled. RXON is set as the Start primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. RXON is READ ONLY; writing to this bit has no effect.
09	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low whenthe Interrupt Flag is set. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0 the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit, by Bus RESET, or by issuing a Stop primitive. INEA may not be set while in the Stopped phase.
08	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: MISS, MERR, RINT, TINT, PINT. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a Stop primitive.
07	MERR	MEMORY ERROR is set when the MK5021 is the Bus Master and $\overline{\text{READY}}$ has not been asserted within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the MK5021 releases the bus, the receiver and transmitter are turned off, and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
06	MISS	MISSED frame is set when the receiver loses a frame because it does not own a receive buffer indicating loss of data. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
05	ROR	RECEIVER OVERRUN indicates that the Receiver FIFO was full When the receiver was ready to input data to the Receiver FIFO. The frame being received is lost, but is probably recoverable if an upper level protocol is used. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
04	TUR	TRANSMITTER UNDERRUN indicates that the MK5021 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.

03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive. When PINT is set, an interrupt is generated if INEA =1. PINT is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. When TINT is set, an interrupt is generated if INEA =1. TINT is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
01	RINT	RECEIVER INTERRUPT is set after the MK5021 updates an entry in the Receive Descriptor Ring. When RINT is set, an interrupt is generated if INEA =1. RINT is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
00	0	This bit is READ ONLY and will always read as a zero.

4.1.2.2 Control and Status Register 1 (CSR1)

RAP <3:1> = 1

BIT	NAME	DESCRIPTION

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
UERR	UAV	0	0	UPRIM <3:0>				PLOST	PAV	0	0	PPRIM <3:0>			

15 UERR

USER PRIMITIVE ERROR is set by the MK5021 when a primitive is issued by the user which is in conflict with the current status of the chip. UERR is READ/CLEAR ONLY and is set by MK5021 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.

14 UAV

USER PRIMITIVE AVAILABLE is set by the user when a primitive is written into UPRIM. It is cleared by the MK5021 after the primitive has been processed. This bit is also cleared by a Bus RESET.

13:08 UPRIM

USER PRIMITIVE is written by the user, in conjunction with setting UAV, to control the MK5021 link procedures. The following primitives are available:

0 Stop: causes the MK5021 to enter the Stopped mode or phase. All DMA activity ceases, the transmitter transmits all ones, and all received data is ignored. Valid in all states except Stopped mode.

2 Init: instructs the MK5021 to read the initialization block from memory. Valid only in the Stopped mode or phase. This should be performed prior to the Start primitive after a bus reset or power up.

3 Start: instructs the MK5021 to enter the Data Transfer phase of operation. Data frames are transmitted and received out of the descriptor rings with no Address and Control fields prepended to the frames. If the PROM bit in CSR2 is set, then no address filtering is performed on received frames. Data Transfer Mode may be exited only with a Stop primitive or by a bus reset. Valid only in the Stopped phase.

4 Status Request: instructs the MK5021 to write the current chip status into the STATUS BUFFER. Valid in all states, but only after the Init primitive has been previously issued.

5 Self-Test Request: instructs the MK5021 to perform the built in internal self test. Valid only in the Stopped phase. See section 4.4.8 for the self test procedure.

8 Timer Start: Instructs the MK5021 to start Timer T1. Valid only after Start primitive has been issued.

9 Timer Stop: Instructs the MK5021 to stop Timer T1. Valid only after Start primitive has been issued.

07	PLOST		PROVIDER PRIMITIVE LOST is set by MK5021 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared and by a Bus RESET. Writing to this bit has no effect.
06	PAV		PROVIDER PRIMITIVE AVAILABLE is set by the MK5021 when a new provider primitive has been placed in PPRIM. PPRIM is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET. Under normal operation the host should clear the PAV bit after PPRIM is read.
05:00	PPRIM		PROVIDER PRIMITIVE is written by the MK5021, in conjunction with setting the PAV bit, to inform the user of chip control conditions. Valid Provider Primitives are as follows:
		2	Init Confirmation: indicates that the initialization has completed.
		8	Timer Expiration: Indicates Timer T1 has expired.

4.1.2.3 Control and Status Register 2 (CSR2)

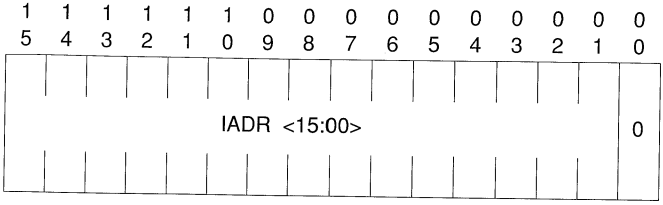
RAP<3:1> = 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	PROM	1	GLBLE	IADR<23:16>							

BIT	NAME	DESCRIPTION
15:11	0	Reserved, must be written as zeroes.
10	PROM	Address filtering is disabled if this bit is set (PROM = 1), and all uncorrupted incomming frames, including the Address field, are placed in the Received Descriptor Ring. This bit is READ/WRITE.
09	1	Must be written as one.
08	GLBLE	Setting this bit enables recognition of frames with global address (all 1's)if if address filtering is enabled (PROM = 0). This bit is READ/WRITE.
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

4.1.2.4 Control and Status Register 3 (CSR3)

RAP<3:1> = 3



BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word (lowest address)in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization block must begin on a word boundary.

4.1.2.5 Control and Status Register 4 (CSR4)

RAP<3:1> = 4

CSR4 allows redefinition of the bus master interface.

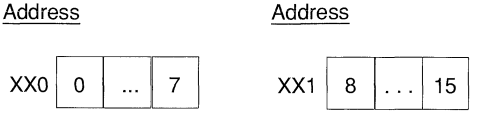
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FWM		BAE	BUSR	BSWPC	BURST	1:0	BSWPD	ACON	BCON

BIT	NAME	DESCRIPTION
15:10	0	Reserved, must be written as zeroes.
09:08	FWM	These bits define the FIFO watermarks. FIFO watermarks prevent the MK5021 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive data, data will only be transferred to the data buffers after the FIFO has at least N 16-bit words or an end of frame has been reached. Conversely, for transmit data, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows:

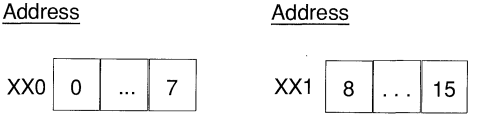
FWM<1:0>	N
11	1 word
10*	9 words
01	17 words
00	25 words

* Suggested setting

07	BAE	Bus Address Enable: if BAE is set then the A23-A20 pins are driven by the MK5021 constantly providing the ability to use A23-A20 for memory bus selection. If clear, A23-A20 behave identically to A19- A16.
06	BUSR	If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear then pin 15 is either $\overline{\text{BM0}}$ or BYTE depending on bit 00. For more information see the description for pin 15 in this document. BUSR is READ/WRITE and cleared on bus Reset.
05	BSWPC	This bit determines the byte ordering of all "non-data" DMA transfers. "Non-data DMA transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows the MK5021 to operate with memory organizations that have bits 07:00 at even addresses and with bits 15:08 at odd addressses or vice versa. BSWPC is Read/Write and cleared by BUS RESET. With BSWPC = 1:



This memory organization is used with the LSI 11 microprocessor and the 8086 microprocessor.
With BSWPC = 0:



This memory organization is used with the 68000 and the Z8000 microprocessors.

04:03 BURST

This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on bus Reset.

BURST<1:0>	8 bit mode	16 bit mode
00	2	1
10*	16	8
01	unlimited	unlimited

* Suggested setting

02 BSWPD

This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.

01 ACON

ALE CONTROL defines the assertive state of pin 18 when the MK5021 is a Bus Master. ACON is READ/ WRITE and cleared by Bus RESET.

ACON	PIN 18	NAME
0	ASSERTED HIGH	ALE
1	ASSERTED LOW	$\overline{AS}$

00 BCON

BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN16	PIN15	PIN17
0	$\overline{BM\ 1}$	$\overline{BM\ 0}$	$\overline{HOLD}$
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

4.1.2.6 Control and Status Register 5 (CSR5)

RAP<3:1> = 5
CSR5 facilitates control and monitoring of modem controls.

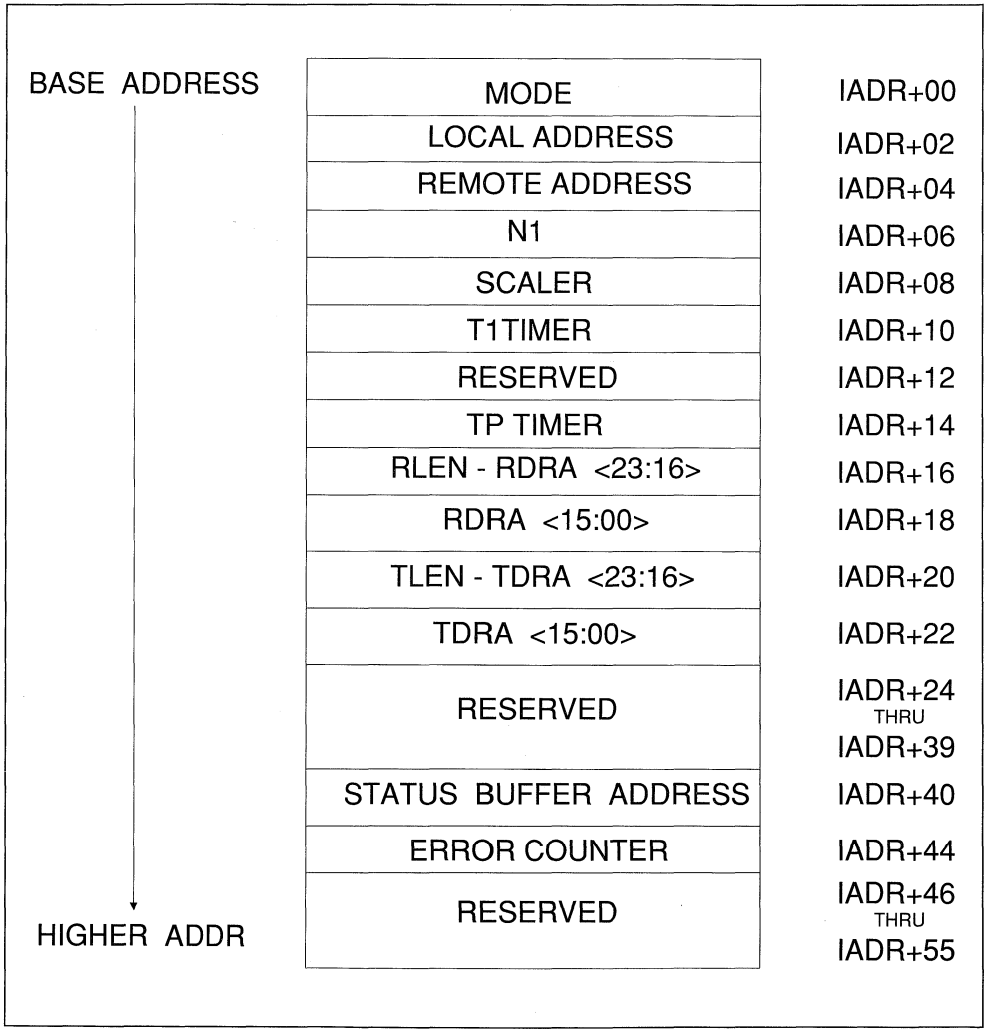
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	RTSEN	DTRD	DSRD	DTR	DSR

BIT	NAME	DESCRIPTION
15:05	0	Reserved, must be written as zeroes.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set, pin 26 becomes $\overline{RTS}$ and pin 30 becomes $\overline{CTS}$. $\overline{RTS}$ is driven low whenever the MK5021 has data to transmit and is kept low during transmission. $\overline{RTS}$ will be driven high after the closing flag of a signal unit is transmited if either no other frames are in the FIFO or if the minimum signal unit spacing is higher than 2 (see Mode Register). The MK5021 will not begin transmission and TD will remain HIGH if $\overline{CTS}$ is high. If RTSEN = 0 then pins 26 and 30 become programmable I/O pins DTR and DSR. The direction and behavior of DSR and DTR are controlled by the following bits.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR/RTS pin. If DTRD = 0, the DTR/RTS pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR/RTS pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR/CTS pin. If DSRD = 0, the DSR/CTS pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR/CTS pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR/RTS pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR/RTS pin.
0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR/CTS pin. If DSRD = 1 this bit becomes READ/WRITE and any value written to this bit appears on the DSR/CTS pin.

4.2 Initialization Block

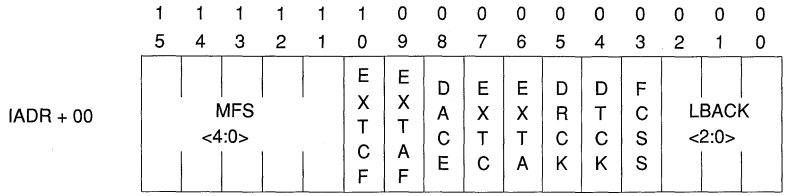
MK5021 initialization includes the reading of the initialization block in memory to obtain the operating parameters. The Initialization Block is defined below. Upon receiving an Init primitive, portions of the Initialization block are read by the MK5021. The remainder of the Initialization block will be read as needed by the MK5021.

Figure 4 : Initialization Block



4.2.1 Mode Register

The Mode Register allows alteration of the MK5021's operating parameters.



BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK5021. This only affects frames transmitted by the MK5021 and does not restrict the spacing of the frames received by the MK5021. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See the following table for encoding of this field.
10	EXTCF	Extended Control Force. If set along with EXTC, the receiver will assume the control field to be two octets long regardless of the first two bits of the control field. See EXTC below.
09	EXTAF	Extended Address Force. If set along with EXTA, the receiver will assume the address to be two otets long regardless of the first bit of the address. See EXTA below.
08	DACE	Address and control field extraction are disabled when DACE is set. Address and control fields are treated as data and placed in memory as such. DACE must be written with "1" for normal transparent data transfer operation, but can be set to "0" for doing address and control field filtering.
07	EXTC	Extended Control Field filtering is enabled when EXTC = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).
06	EXTA	Extended Address Field filtering is enabled when EXTA = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).

Number OF Flags	MFS<4:0>	Number OF Flags	MFS<4:0>
2	0	32	28
4	2	34	24
6	4	36	17
8	9	38	3
10	18	40	6
12	5	42	13
14	11	44	27
16	22	46	23
18	12	48	14
20	25	50	29
22	19	52	26
24	7	54	21
26	15	56	10
28	31	58	20
30	30	60	8
		62	16

05	DRFCS	Disable Receiver FCS (CRC). When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct. If the received frame is an even number of bytes, the first 16 bits of the FCS will be appended to the end (as indicated by MCNT) of the receive Receive buffer data.
04	DTFCS	Disable Transmitter FCS. When DTFCS = 0, the transmitter will generate and append the FCS to each signal unit. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames. Setting DTFCS=1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.
03	FCSS	FCS Select. When FCSS = 1, a 16 bit FCS is selected otherwise a 32 bit FCS is used.
02:00	LBACK	Loopback Control puts the MK5021 into one of several loopback configurations.

LBACK	DESCRIPTION
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock. Transmit clock must be supplied externally.
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with TD pin forced to all ones.
7	Silent clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. The TD pin is forced to all ones.

4.2.2 Address and Control Field Filtering

In the MK5021, address filtering and control field handling applies only to octet aligned frames received with good FCS. Any frame not meeting both of these conditions is discarded and the "Bad Frames Received" error counter (located at IADR + 44 of the Initialization Block) is incremented.

Address filtering is supported if the PROM bit (CSR2, bit 10) is 0. In this case, frames are accepted if the received Address field matches either the Local Address or the Remote Address as specified in the Initialization Block. The Local and Remote addresses may be either one or two octets in length according to the EXTA control bit described in the MODE register. If extended address mode filtering is selected, bit zero of the address field should be set to a zero if adherening to ADCCP/HDLC standards. If extended address filtering is not selected, frame adresses should be located in the lower order byte of their respective fields. The address filtering is a one octet compare if the extended address bit, EXTA is 0 (Mode register bit 06), or follows the HDLC rules for extended addressing if EXTA is 1. Frames not matching either address are ignored. Bit RADR in the Receive Message Descriptor (RMD0 <09>)indicates which of the two programmable adresses the frame matched. If address filtering is not used, these fields can just be written as zeroes.

Extended control field filtering is also possible using the EXTC bit (Mode Register bit 07), as shown in Table 1 and Table 2. If EXTC is 0 then the C-field is one octet for all frames. If however EXTC is set to 1, the MK5025 will look to see if either of the two least significant bits of the C-field is 0. If so, the frame is said to have an extended control field which is two octets. In addition, bits EXTAF and EXTCF (Mode Register bit 09 & 10) are useful to force extended address and control. If EXTAF is set along with EXTA, the receiver will assume the address field to be two bytes long regardless of the first bit of the address field. If EXTCF is set along with EXTC, the receiver will assume the contol field to be two bytes long regardless of the first two bits of that field.

For global adresses, the GLBLE bit is valid in transparent mode, depending upon the settings of the other bits in the Mode Register, as shown in Table 1 below. If bit GLBLE (CSR2 bit 08) is set to 1, then all frames with address "11111111" are accepted.

The following tables show the MK5021 address filtering options and the way in which it handles the received Address and Control fields.

Table 1. MK5021 Address Filtering Options

EXTA	EXTAF	XIDE	PROM	DACE	Address Filtering
0	0	0	0	0	Single octet filtering S&R (Send & Receive frame addresses)
X	X	X	1	X	No address filtering, all frames accepted
0	0	1	0	0	Single octet filtering S&R and global
0	X	X	X	1	Not allowed
1	0	0	0	0	Double octet filtering S&R per HDLC rules
1	0	0	0	1	Double octet filtering S&R per HDLC rules
1	1	0	0	0	Double octet filtering S&R regardless of A-filed LSB
0	1	X	X	0	Not allowed

Table 2. Address and Control Field Handling By The MK5021 Receiver

DACE	PROM	EXTA	EXTAF	EXTC	EXTCF	Address Field Handling	Control Field Handling
0	0	0	0	0	0	A filtered	CC → MEM1
0	0	0	0	1	0	A filtered	CC or EC → MEM1
0	0	1	0	0	0	A or EA filtered	CC → MEM1
0	0	1	1	0	0	EA filtered	CC → MEM1
0	0	1	0	1	0	A or EA filtered	CC or EC → MEM1
0	0	1	1	1	1	EA filtered	EC → MEM1
0	1	0	0	0	0	Not filtered, AA → MEM1	CC → MEM2
0	1	0	0	1	0	Not filtered, AA → MEM1	CC or EC → MEM2
0	1	1	0	0	0	Not filtered, AA or EA → MEM1	CC → MEM2
0	1	1	1	0	0	Not filtered, EA → MEM1	CC → MEM2
0	1	1	0	1	1	Not filtered, AA or EA → MEM1	EC → MEM2
1	0	x	x	x	x	First 2 octets always filtered	EC → MEM1
1	1	x	x	x	x	Total transparent mode	All data after opening flag & before FCS → memory

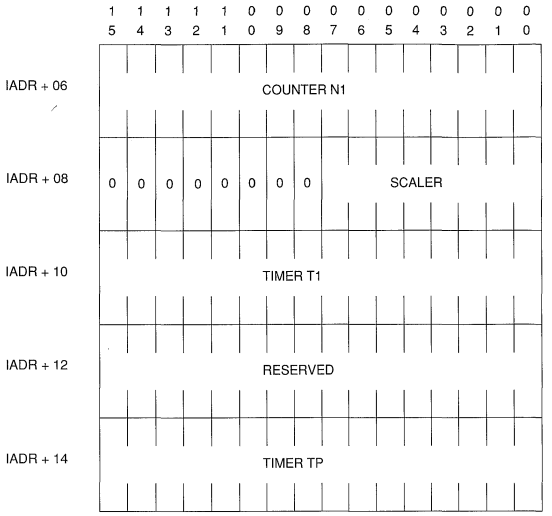
NOTES:

1. MEM1 is the first location and MEM2 is the second location where received data is loaded. MEM1 and MEM2 are each 16 bits wide.
2. C is the received, single octet, control field. CC →MEMx means the single octet control field C is loaded into both bytes of a 16 bit memory location. Similarly, A is a single octet address field, and AA →MEMx means the single octet address field A is loaded into both bytes of a 16 bit memory location.
3. EC is an extended control field (2 octets). If EXTC=1 and either of the 2 LSB's of the control filed is 0, the control field is considered extended, This determines whether CC or EC →MEMx. However, when EXTCF is set to 1, the control field is always extended .
4. EA is an extended address field (2 octets). "A or EA filtered" means that one octet of the A-field is filtered if the LSB = 1, or two octets are filtered if the LSB = 0. Similarly "AA or EA → MEM1" means that AA is loaded into memory if the LSB = 0; else, EA is loaded. This conforms to HDLC rules for extended address. However, if EXTAF is set to 1, two octets are filtered regardless of the LSB, and EA will be loaded into memory.
5. .PROM is CSR2 bit 10.
6. DACE, EXTA, EXTAF, EXTC, and EXTCF are as defined in the Mode register. X = Do not care.

4.2.3 Timers

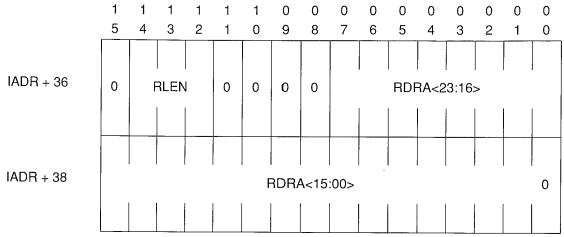
There are 3 independent counter-timers. The upper 8 bits of IADR+02 are used as a scaler for T1 and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is a 16 bit counter and is used to count the number of bytes in a frame.

The Host will write the period of N1, T1 and TP into the Initialization Block.



TIMER	DESCRIPTION
N1	MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame that exceeds this count will be discarded.
SCALER	TIMER PRESCALER. Timers T1 and TP are scaled by this number. The prescaler is incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. Note: a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8224 clock pulses).
T1	GENERAL PURPOSE TIMER. The T1 timer is started by issuing a Timer Start primitive 8, and is stopped by issuing a Timer Stop pimitive 9. A Timer Expiration provider primitive 8 indicates T1 has expired. This field must contain the two's complement of the period of Timer T1.
TP	TRANSMIT POLLING PERIOD. This scaled timer determines the length of time between transmit frame checks. Unless TDMD (see CSR0) is set or a frame is received, no attempt to transmit a frame in the transmit descriptor ring is made until TP expires. At TP expiration all transmit frames in the transmit descriptor ring will be sent. This field must contain the two's complement of the period of Timer T1.

4.2.4 Receive Descriptor Ring Pointer

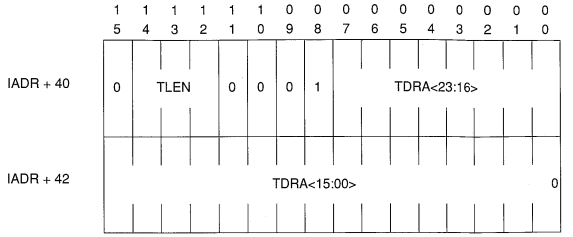


BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	RLEN	RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.

RLEN	Number Of entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

11:08	0	Reserved, must be written as zeroes.
07:00/15:00	RDRA	RECEIVE DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Receive Descriptor Ring. The Receive Descriptor Address must begin on a word boundary.

4.2.5 Transmit Descriptor Ring Pointer



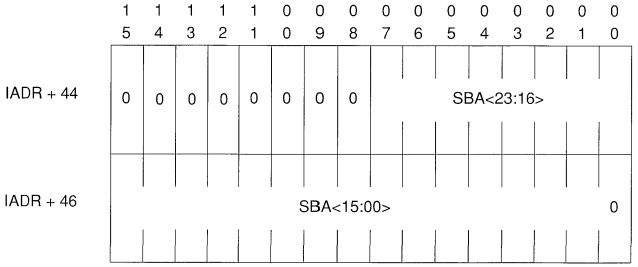
BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	TLEN	TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	Number Of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

11:09	0	Reserved, must be written as a zero.
08	1	Must be set to 1 to enable transmission from the Transmit Descriptor Ring.
07:00/15:00	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring. The Transmit Descriptor Ring Address must begin on a word boundary.

4.2.6 Status Buffer Address

BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as zeroes.
07:00/15:00	SBA	STATUS BUFFER ADDRESS points to a 7 word status buffer into which status information is placed upon the issuance of the Status Request primitive by the HOST. The status buffer must begin on a word boundary.



4.2.7 Error Counters One location in the Initialization buffer is reserved for use as an error counter which the MK5021 will increment. This counter is intended for use by the host CPU for statistical analysis. The MK5021 will only increment the counter, it is up to the user to clear and preset the counter.

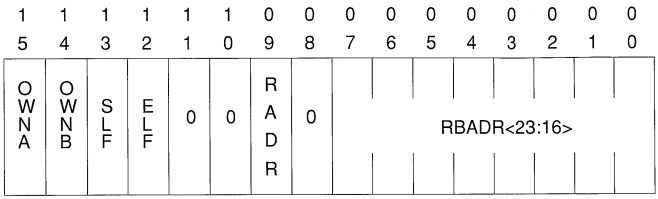
Memory Address	Error Counter
IADR + 44	Bad Frames Received - Bad FCS - Non-Octet Aligned - Aborted Frame
IADR + 46 thru IADR + 55	Reserved. Must be programmed as zeroes.

4.3 Receive and Transmit Descriptor Rings

Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

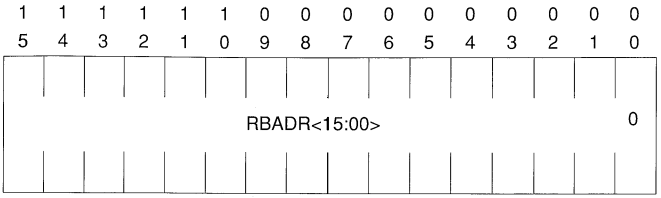
4.3.1 Receive Message Descriptor Entry

4.3.1.1 Receive Message Descriptor 0 (RMD0)



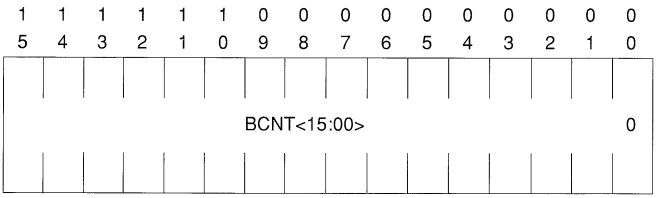
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK5021 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided a valid signal unit has been received. The Host sets the OWNA bit after emptying the buffer. Once the MK5021, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the SLAVE PROCESSOR owns the buffer when OWNA is a zero. The MK5021 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.
13	SLF	Start of Long Frame indicates that this is the first buffer used by MK5021 for this frame. It is used for data chaining buffers. SLF is set by the MK5021. NOTE: A "Long Frame" is any frame which needs data chaining.
12	ELF	End of Long Frame indicates that this the last buffer used by the MK5021 for this frame. It is used for data chaining buffers. If both SLF and ELF were set, the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK5021.
08	0	Reserved, must be written as zeroes.
09	RADR	With address filtering enabled, RADR indicates which of the 2 programmable addressses the frame matched. If set, the received address field matched the value in the Address Field 1 of the Initialization buffer. Otherwise it matched the value in the Address Field 2.
11:10	0	Reserved, must be written as zeroes.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5021.

4.3.1.2 Receive Message Descriptor 1 (RMD1)



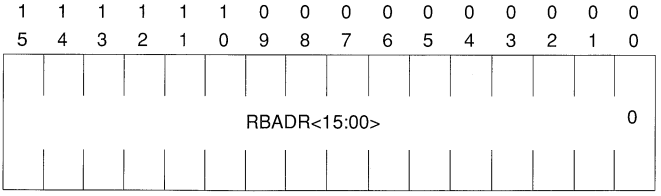
BIT	NAME	DESCRIPTION
15:01	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK5021. The receive buffers must be word aligned.

4.3.1.3 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK5021. The value of BCNT must be an even number.

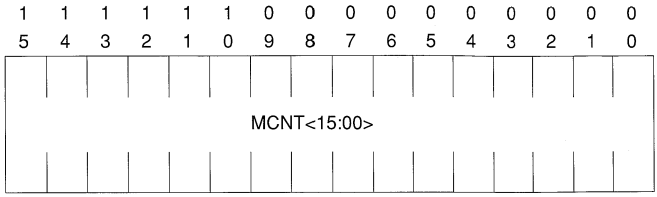
4.3.1.4 Receive Message Descriptor 3 (RMD3)



BIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the received signal unit. MCNT is valid only when ELF is set to a one. MCNT is written by MK5021 and read by the Host. If ELF is set to a zero the entire buffer has been utilized and the message byte count is given in BCNT above. The value of this field is expressed in two's complement.

4.3.2 Transmit Message Descriptor Entry

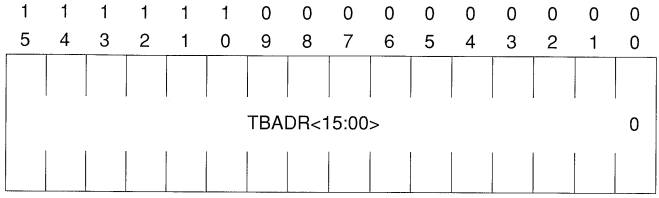
4.3.2.1 Transmit Message Descriptor 0 (TMD0)



BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK5021 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK5021 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the receiver. After the MK5021, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the I/O ACCELERATION PROCESSOR owns the buffer when OWNA is a zero. The MK5021 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.
13	SLF	Start of Long Frame indicates that this is the first buffer used by MK5021 for this frame. It is used for data chaining buffers. SLF is set by the Host. When not chaining, SLF should be set to a one. NOTE: A "Long Frame" is any frame which needs data chaining.
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK5021 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host. When not chaining, ELF should be set to a one.
11	1	This bit must be set for anything transmitted.
10:08	0	Reserved, must be written as zeroes.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5021.

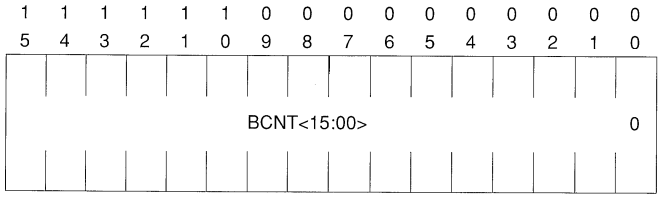
4.3.2.2 Transmit Message Descriptor 1 (TMD1)

BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK5021. The least significant bit is zero since the descriptor must be word aligned.



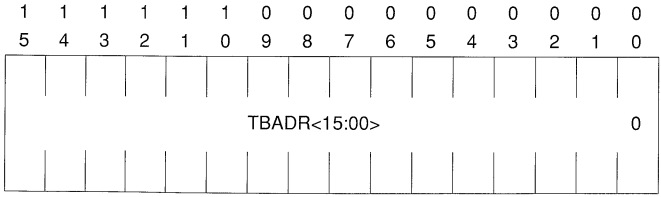
4.3.2.3 Transmit Message Descriptor 2 (TMD2)

BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the usable length of the buffer pointed to by this descriptor expressed in two's complement. This field is not used by the MK5021.



4.3.2.4 Transmit Message Descriptor 3 (TMD3)

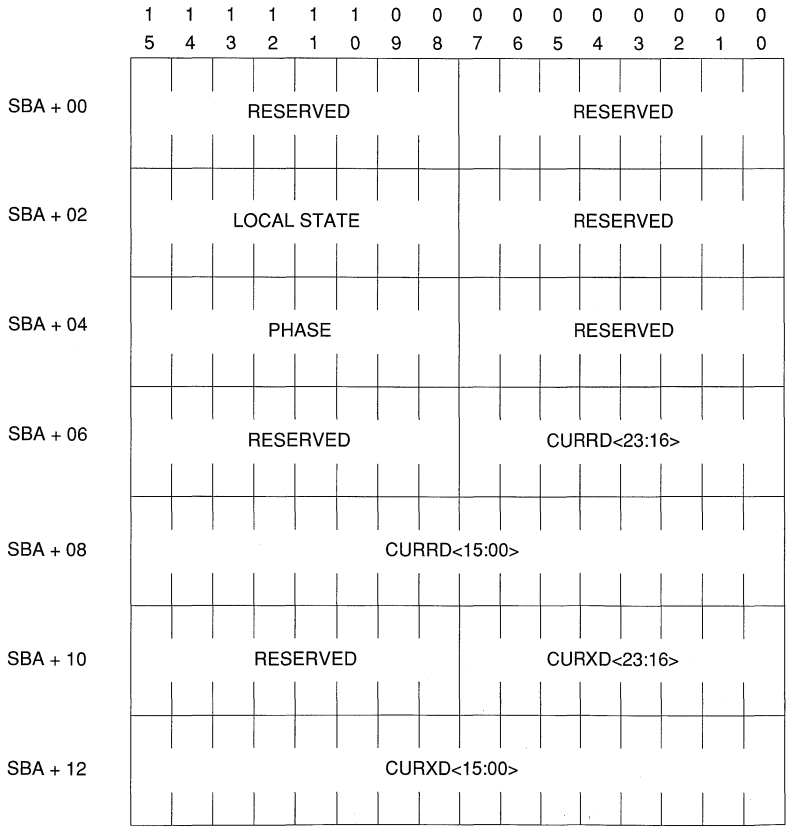
BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in octets, of the data contained in the corresponding buffer. The value of this field is expressed in two's complement.



4.3.3 Status Buffer

FIELD	DESCRIPTION
LOCAL STATE	Indicates the current state of operation for the device. 0: Normal Data Transfer State 4: Normal Disconnected State
PHASE	Indicates the current phase of operation for the device. -1: Stopped Mode 3: Data Transfer phase
CURRD:00	Current Receive Descriptor. This pointer indicates the position of the descriptor for the next receive buffer to be filled.
CURXD:00	Current Transmit Descriptor. This pointer indicates the position of the descriptor for the next transmit buffer to be transmitted.

MK5021 STATUS BUFFER



4.4 Detailed Programming Procedures

4.4.1 Initialization

The following procedure should be followed to intialize the MK5021:

1. Setup bus control information in CSR4.
2. Setup the Initialization Block and Desciptor Rings.
3. Load the address of the initialization block information into CSR's 2 and 3.
4. Issue the INIT primitive through CSR1 (write 4200H to CSR1) instructing the MK5021 to read the initialization block pointed to by CSR's 2 and 3.
5. Wait for the INIT confirmation primitive (CSR1 = 0242H) from the MK5021. Then clear the PAV bit in CSR1 (write 0040H to CSR1).
6. Issue the Start primitive through CSR1 (write 4300H to CSR1). Flags will now be continously transmitted.
7. Enable interrupts in CSR0 if desired.

4.4.2 Sending Data

Use the following procedure to send a frame:

1. Wait for the OWNA bit of the current transmit descriptor to be cleared, if it is not already.
2. Fill the buffer associated with the current transmit descriptor with the data to be sent, or set the de- scriptor buffer address to any already filled buffer.
3. Repeat steps 1 and 2 for the next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.

4.4.3 Receiving Data

The following procedure should be followed when receiving a frame:

1. Make sure the OWNA bit of the current receive descriptor is clear.
2. Read data out of the buffer associated with the current receive descriptor.
3. Set the OWNA bit of the current receive descriptor.
4. If the ELF bit of the current receive descriptor is clear, then go on to the next descriptor and repeat the above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

4.4.4 Disabling the MK5021

The following procedure should be followed to disable the MK5021:

1. Issue the STOP primitive through CSR1. This will disable the MK5021 from receiving or transmitting. The TD pin will be held high while the MK5021 is in the Stopped mode. The STOP bit in CSR0 will be set and interrupts will be disabled. If reception or transmission of a frame is in progress, then received data may be lost, and the transmitted frame will be aborted.

4.4.7 Re-enabling the MK5021

The same procedure should be followed for re-enabling the MK5021 as was used to initalize upon power up. If the Initialization Block and the hardware configuration have not changed, then steps 1,2,3, 4 and 5 of the intialization sequence may be omitted.

4.4.8 MK5021 Internal Self Test

The MK5021 contains an easy to use internal self test designed to test, with a high fault coverage, all of the major blocks of the device except the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.
The following procedure should be followed to execute the internal self test:

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK5021.
5. After the PAV bit is set, read CSR1. If bit 04 is set (CSR1 = 0), the self test passed, if bit 04 is clear, it failed. The success or failure of the test is futher indicated in the PPRIM field as follows:

PPRIM	RESULT
0	Passed self test.
1	Failed the reset test of the self test.
2	Failed the self test in the micro controller RAM.
3	Failed the self test in the ALU.
4	Failed the self test in the timers.
5	Failed the self test in the transmitter and/or receiver.
6	Failed the self test in the CSR's and/or bus master.
Otherwise	Failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHZ), then the MK5021 is unable to respond to the Self Test Request and will not complete successfully.

If the self test passes, then it may be immediately reexecuted from step 3, otherwise re-execution should proceed from step 1.

SECTION 5: ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias . . . . . –25 °C to + 100 °C
Storage Temperature . . . . . –65 °C to + 150 °C
Voltage on Any Pin with Respect to Ground . . . . . –0.5 V to V_{CC} + 0.5 V
Power Dissipation . . . . . 0.50 W

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to 70 °C, V_{CC} = +5 V ±5 percent unless otherwise specified

Symbol	Conditions	Min.	Typ.	Max.	Units
V_{IL}		–0.5		+0.8	V
V_{IH}		+2.0		V_{CC}+0.5	V
V_{OL}	@ I_{OL} = 3.2 mA			+0.5	V
V_{OH}	@ I_{OH} = –0.4 mA	+2.4			V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}			± 10	µA
I_{CC}	@ T_{SCT} = 100 ns		50		mA

CAPACITANCE

F=1 MHz

Symbol	Parameter	Min.	Max.	Units
C_{IN}	Capacitance on Inputs pins		10	pf
C_{OUT}	Capacitance on Output Pins		10	pf
C_{IO}	Capacitance on I/O pins		20	pf

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
1	SYSCLK	T_{SCT}	SYSCLK period		100		2000
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK	T_{SCF}	Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	TCLK	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$	CL = 50 pF	0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	CL = 50 pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$		5		

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

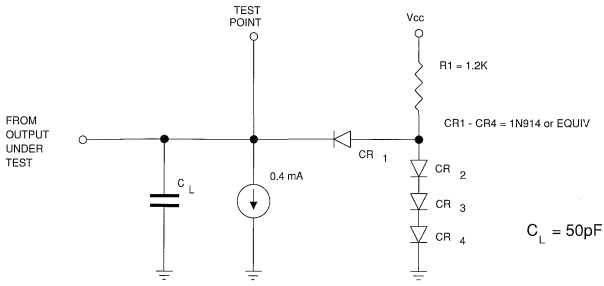
No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		140		
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD data rise time		0		8
19	RD	T_{RDF}	RD data fall time		0		8
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		30		
22	A/DAL	T_{DOFF}	Bus Master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master driver enable after falling edge of $\overline{HLDA}$	TSCT = 100 ns	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ pulse width		30		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time	TSCT = 100 ns	600		
27	A	T_{XAS}	Address setup time to falling edge of ALE		100		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		20		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus Master read)		55		
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus Master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$(Bus Master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus Master write)		250		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus Master write)		35		
36	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)	TSCT = 100 ns	0		35
37	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave write)		0		
38	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	ALE	T_{ALEW}	ALE width high		110		
40	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

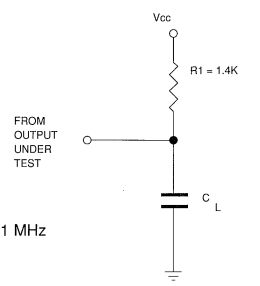
No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus Master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD} = 300 ns T_{SCT} = 100 ns	120		250
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus Master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus Master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus Master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus Master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus Master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus Master read)		35		
51	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus Master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
54	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600nS)	T_{SCT} = 100 nS			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus Master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)	T_{SCT} = 100 nS			35
60	$\overline{READY}$	T_{RSH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
61	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (Bus slave)	TSCT = 100 ns		200	

Figure 5a: TTL Output Load Diagram



NOTE: This load is used on all outputs except INTR, HOLD, READY.

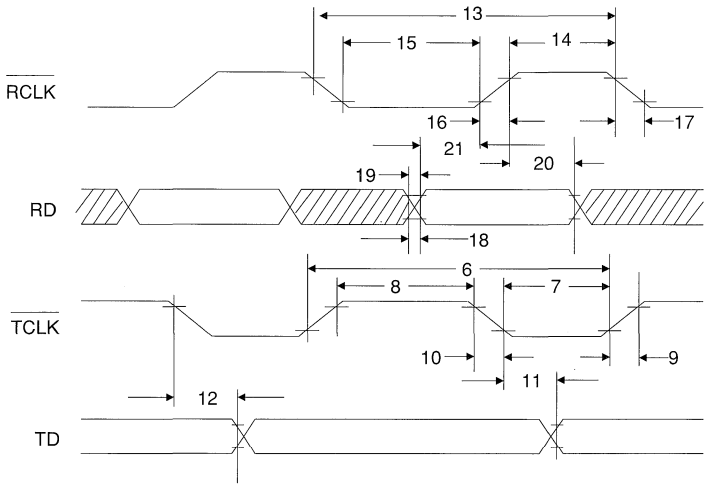
Figure 5B: Open Drain Output Load Diagram



C_L = 50pF min @ 1 MHz

NOTE: This load is used on open drain outputs INTR, HOLD, READY.

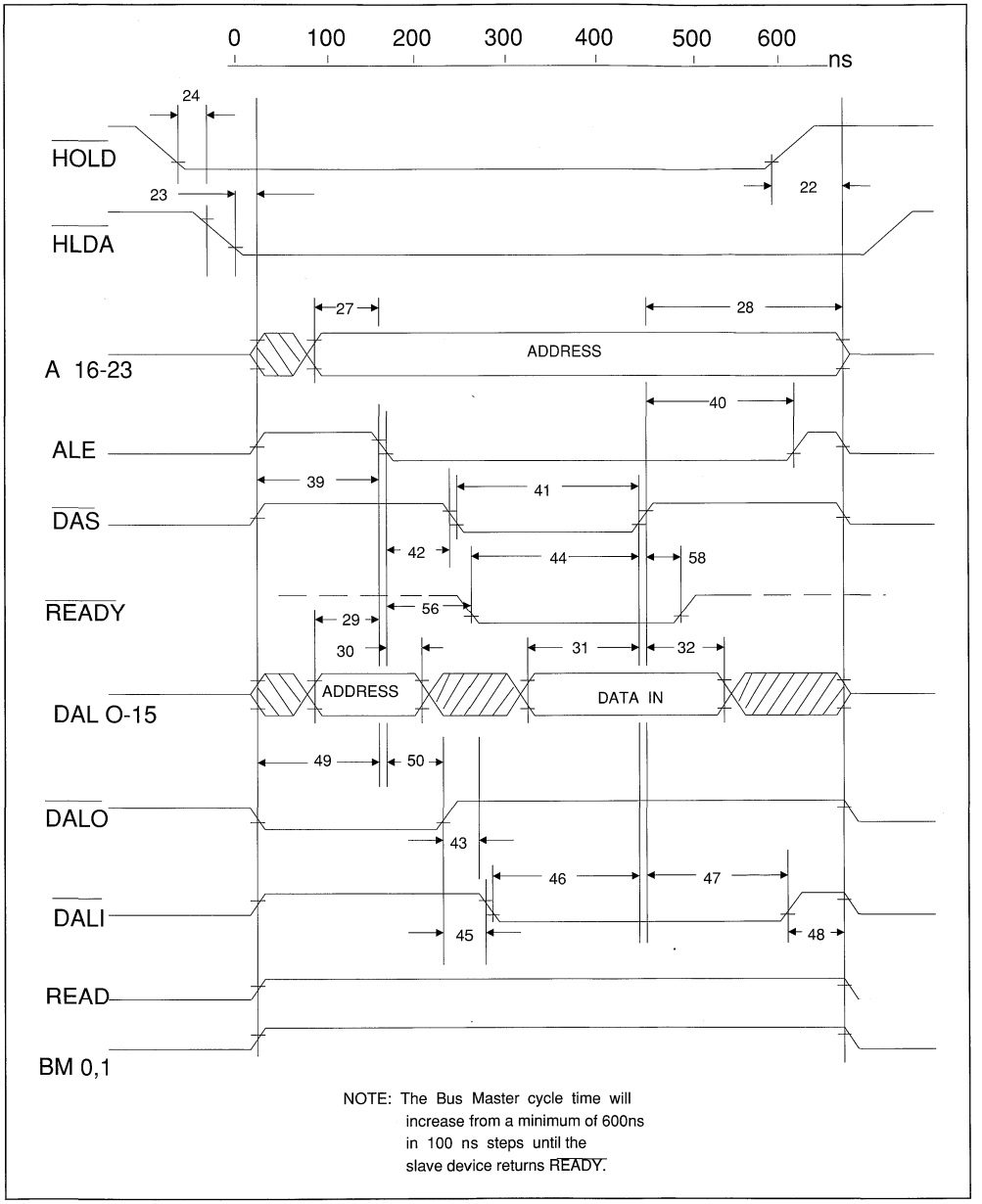
Figure 6: MK5021 Serial Link Timing Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

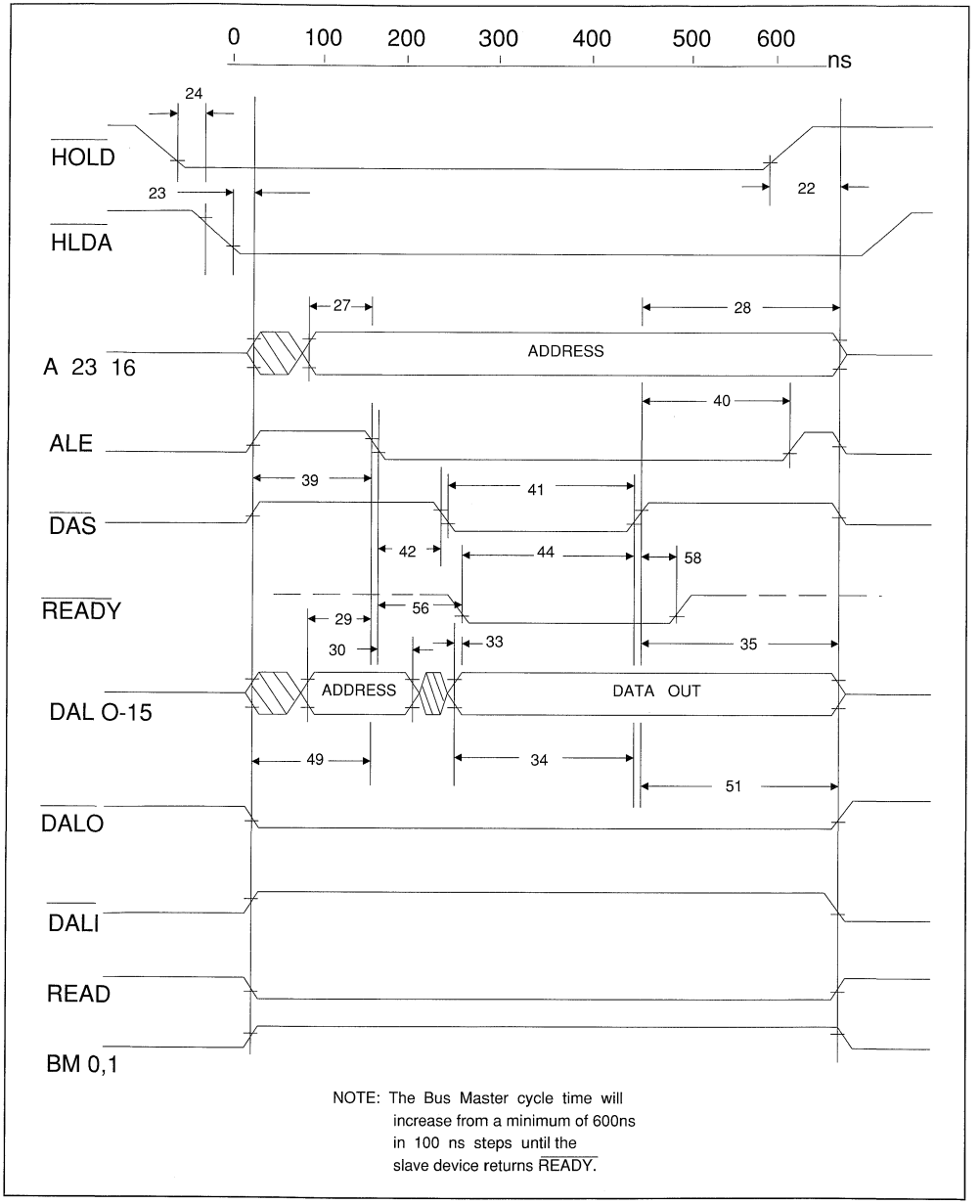
	"1"	"0"
OUTPUT	2.0 V	O.8 V
INPUT	2.0 V	O.8 V
FLOAT	10 %	90 %

Figure 7: MK5021 Bus Master Timing Diagram (Read)



NOTE: The Bus Master cycle time will increase from a minimum of 600ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 8: MK5021 Bus Master Timing Diagram (Write)



NOTE: The Bus Master cycle time will increase from a minimum of 600ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 9: MK5021 Bus Slave Timing Diagram (Read)

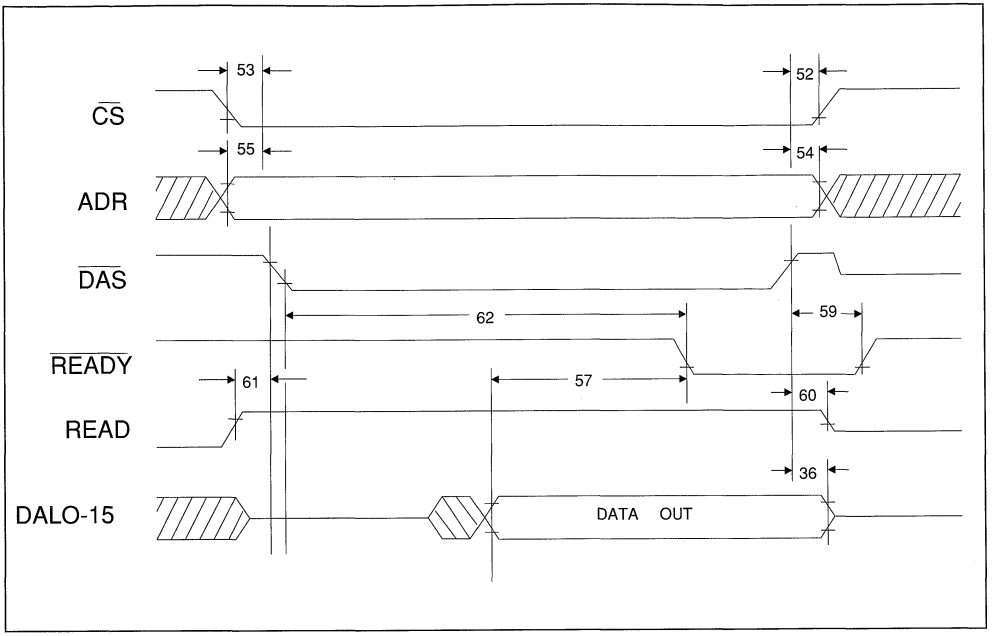
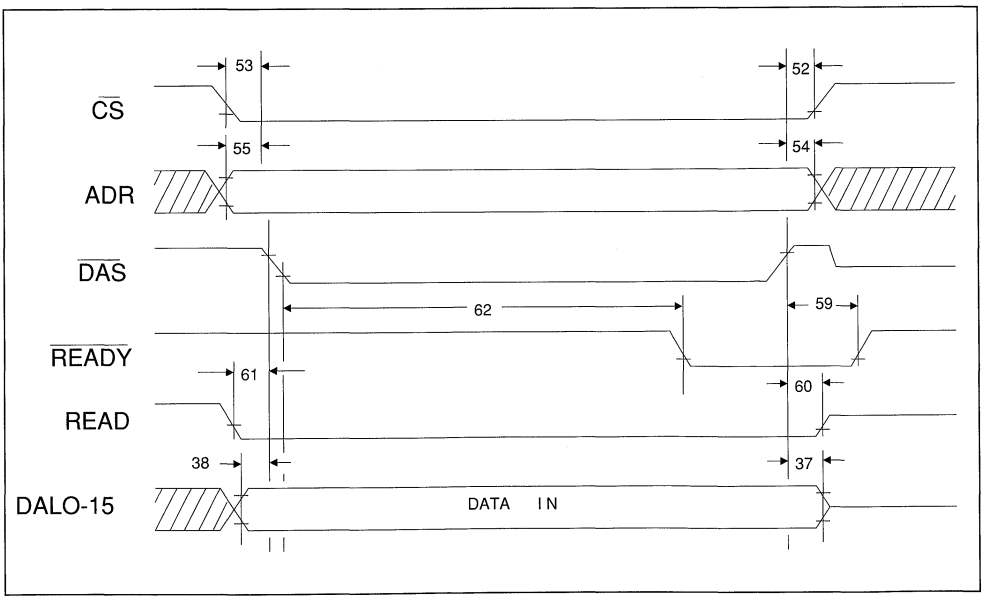


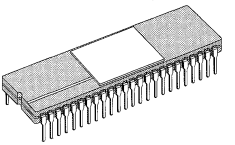
Figure 10: MK5021 Bus Slave Timing Diagram (Write)



CCITT X.25 LINK LEVEL CONTROLLER

PRELIMINARY DATA

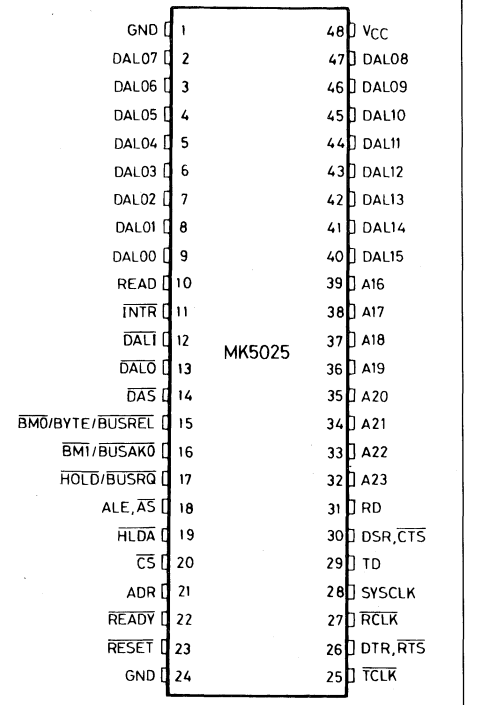
- CMOS
- FULLY COMPATIBLE WITH BOTH 8-BIT OR 16-BIT SYSTEMS
- SYSTEM CLOCK RATE TO 10MHz
- DATE RATE UP TO 7Mbps, WITH A 64-BYTE FIFO IN EACH DIRECTION
- COMPLETE DATA LINK LAYER IMPLEMENTATION
- COMPATIBLE WITH X.25 LAPB, ISDN LAPD, X.32, AND X.75 LINK LEVEL PROTOCOLS
- 48-PIN DIP NEARLY PIN-FOR-PIN COMPATIBLE WITH THE LANCE CHIP (MK7990)
- BUFFER MANAGEMENT INCLUDES :
  - initialization block
  - separate receive and transmit rings
  - variable descriptor ring and window size
- ON CHIP DMA CONTROL WITH PROGRAMMABLE BURST LENGTH
- SELECTABLE SINGLE OR EXTENDED CONTROL FIELD
- PROGRAMMABLE 1 BYTE OR 2 BYTES ADDRESS FIELD AND GLOBAL ADDRESS
- TRANSPARENT MODE WITH OR WITHOUT ADDRESS FILTERING ALLOWS DISABLING X.25 PROCESSING FOR CUSTOMIZED APPLICATIONS
- HANDLES ALL HDLC (ADCCP) FRAME FORMATTING :
  - zero bit insert and delete
  - FCS generation and detection
  - frame delimiters by flags
- FIVE PROGRAMMABLE TIMER/COUNTERS : T1, T3, TP, N1, N2
- HANDLES ALL ERROR RECOVERY, SEQUENCING, AND S AND U FRAME CONTROL
- SELECTABLE FCS OF 16 OR 32 BITS
- DATA LINK SERVICES :
  - compatible with ISO data link services
  - compatible with LAPD data link services
- TESTING FACILITIES :
  - built-in self test facility
  - 4 loopback modes
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE
- PROGRAMMABLE FOR FULL OR HALF DUPLEX OPERATION
- PROGRAMMABLE MINIMUM FRAME SPACING ON TRANSMIT (flags between frames)



CDIP48 **PLCC52**

(Order codes at the end of the datasheet)

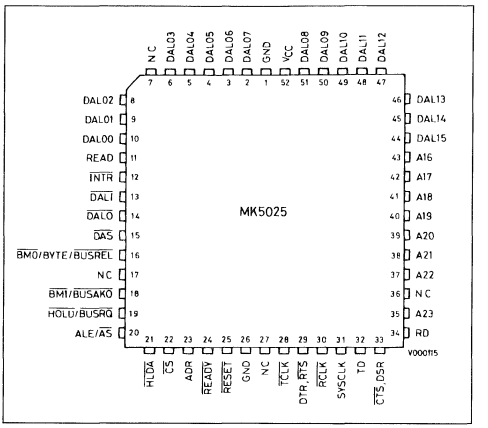
Figure 1 : MK5025 Dual in Line Pin Configuration.



GENERAL DESCRIPTION

The SGS-THOMSON X.25 Link Level Controller (MK5025) is a VLSI semiconductor device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, U (unnumbered) frame control, and S (supervisory) frame control. The MK5025 also supports X.32 (XID), X.75, and ISDN LAPD. The MK5025 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

Figure 2 : MK5025 Chip Carrier Pin Configuration.



PIN DESCRIPTIONS

DAL <07 : 00> (Input/Output ; 3-State). The time multiplexed Data/Address bus. During the address portion of the memory transfer, DAL <07 : 00> contains the lower 8 bits of the memory address. During the data portion of the memory address. During the data portion of a memory transfer, DAL <07 : 00> contains the read or write data, depending on the type of transfer.

READ (Input/Output ; 3-State). READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5025 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated by the MK5025 at all other times.

- MK5025 as a Bus Slave
  - READ = HIGH - Data is placed on the DAL lines by the chip.
  - READ = LOW - Data is taken off the DAL lines by the chip.
- MK5025 as a Bus Master
  - READ = HIGH - Data is taken off the DAL lines by the chip.
  - READ = LOW - Data is placed on the DAL lines by the chip.

$\overline{\text{INTR}}$ (Output ; Open Drain). INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set : MISS, MERR, ROR, TUR, RINT, TINT OR PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.

$\overline{\text{DALI}}$ (Output ; 3-State). DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by MK5025 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.

$\overline{\text{DALO}}$ (Output ; 3-State). DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5025 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by MK5025 when it driven the DAL lines during the data portion of a READ transfer or for the duration of a WRITE transfer.

$\overline{\text{DAS}}$ (Input/Output ; 3-State). DATA STROBE defines the data portion of a bus transaction. By definition data is stable and valid at the low to high transition of DAS. This signal is driven by the MK5025 while it is the BUS MASTER. During Bus Slave operations, this pin is used as an input. At all other times the signal is tristated.

$\overline{\text{BM0}}$, BYTE, $\overline{\text{BUSREL}}$ (Input/Output ; 3-State). I/O pins 15 (16) and 16 (18) are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 (16) becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5025 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear the pin 15 (16) is the output $\overline{\text{BM0}}$, and behaves as described below for pin 16 (18).

$\overline{\text{BM1}}$, $\overline{\text{BUSAKO}}$ (Output ; 3-State). Pin 15 (16) and 16 (18) are programmable through bit 00 of CSR4 (BCON).

If CSR4 <00> BCON = 0,
- I/O Pin 15 (16) = $\overline{\text{BM0}}$ (Output ; 3-State)
- I/O Pin 16 (18) = $\overline{\text{BM1}}$ (Output ; 3-State)

BYTE MASK <1 : 0> Indicates the byte(s) on the DAL to be read or written during this bus transition.

PIN DESCRIPTIONS (continued)

MK5025 drives these lines only as a Bus Master. MK5025 ignores the BM lines when it is a Bus Slave.

Byte selection is done as outlined in the following table :

BM1	$\overline{BM0}$	
LOW	LOW	Entire Word
LOW	HIGH	Upper Byte (DAL <15 : 08>)
HIGH	LOW	Lower Byte (DAL <07 : 00>)
HIGH	HIGH	None

If CSR4 <00> BCON = 1,
I/O Pin 15 (16) = $\overline{\text{BYTE}}$ (Output ; 3-State)
I/O Pin 16 (18) = $\overline{\text{BUSAKO}}$ (Output)

Byte selection is done using the BYTE line and DAL <00> latched during the address portion of the bus transaction. MK5025 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table :

BYTE	DAL <00>	
LOW	LOW	Entire Word
LOW	HIGH	Illegal Condition
HIGH	LOW	Lower Byte
HIGH	HIGH	Upper Byte

$\overline{\text{BUSAKO}}$ is a bus request daisy chain output. If MK5025 is not requesting the bus and it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ will be driven low. If MK5025 is requesting the bus when it receives $\overline{\text{HLDA}}$, $\overline{\text{BUSAKO}}$ will remain high.

$\overline{\text{HOLD}}$, $\overline{\text{BUSRQ}}$ (Input/Output ; Open Drain). Pin 17 (19) is configured through bit 0 of CSR4.

If CSR4 <00> BCON = 0
I/O Pin 17 (19) = $\overline{\text{HOLD}}$

$\overline{\text{HOLD}}$ request is asserted by MK5025 when it requires a DMA cycle regardless of the previous state of the $\overline{\text{HOLD}}$ pin. $\overline{\text{HOLD}}$ is held low for the entire ensuing bus transaction.

If CSR4 <00> BCON = 1
I/O Pin 17 (19) = $\overline{\text{BUSRQ}}$

$\overline{\text{BUSRQ}}$ is asserted by the MK5025 when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high. $\overline{\text{BUSRQ}}$ is held low for the entire ensuring bus transaction.

ALE, $\overline{\text{AS}}$. ***Address Latch Enable, Address Strobe*** (Output ; 3-State). The active level of Address Strobe is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by the MK5025 while it is the BUS MASTER. At all other times, the signal is tristated.

If CSR4 <00> ACON = 0
I/O PIN 18 (20) = ALE

Address Latch Enable is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion.

If CSR4 <00> ACON = 1,
I/O Pin 18 (20) = $\overline{\text{AS}}$

As $\overline{\text{AS}}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{\text{AS}}$ can be used by a slave device to strobe the address into a register.

HLDA. ***Hold Acknowledge*** (Input). Hold Acknowledge is the response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to MK5025's assertion of $\overline{\text{HOLD}}$, the MK5025 is the Bus Master. $\overline{\text{HLDA}}$ should be disasserted ONLY after $\overline{\text{HOLD}}$ has been released by MK5025.

$\overline{\text{CS}}$. ***Chip Select*** (Input). Chip Select indicates, when low, that the MK5025 is the slave device for the data transfer. $\overline{\text{CS}}$ must be valid throughout the entire transaction.

$\overline{\text{ADR}}$. ***Address*** (Input). Address selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when CS is low.

ADR	PORT
LOW	Register Data Port
HIGH	Register Address Port

$\overline{\text{READY}}$ (Input/Output ; Open Drain). When the MK5025 is a Bus Master, $\overline{\text{READY}}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle.

As a Bus Slave, the MK5025 asserts $\overline{\text{READY}}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{\text{READY}}$ is a response to $\overline{\text{DAS}}$ and it will be negated after $\overline{\text{DAS}}$ is negated.

PIN DESCRIPTIONS (continued)

RESET (Input). RESET is the Bus signal that will cause MK5025 to cease operation, clear its internal logic and enter an idle state with the STOP bit of CSR0 set.

TCLK. ***Transmit Clock*** (Input). A 1X clock input for transmitter timing. TD changes on the falling edge of TCLK. The frequency of TCLK may be up to 7Mbps.

DTR, RTS. Data Terminal Ready, Request to Send (Input/Output). Modem Control Pin. Pin 26 (29) is configurable through CSR5. This pin can be programmed to behave as output RTS or as programmable I/O in DTR. If configured as RTS, the MK5025 will assert this pin if it has data to send and throughout transmission of a frame.

RCLK. ***Receive Clock*** (Input). A 1X clock input for receiver timing. RD is sampled on the rising edge of RCLK. The frequency of RCLK may be up to 7MHz.

SYSCLK. ***System Clock*** (Input). Used for internal timing of the MK5025. SYSCLK should be a square wave, and be greater than 500KHz and less than 10MHz.

TD. ***Transmit Data*** (Output). Transmit serial data output.

DSR, CTS. ***Data Set Ready, Clear to Send*** (Input/Output). Modem Control Pin. Pin 30 (33) is configurable through CSR5. This pin can be programmed to behave as input CTS or as programmable I/O pin DSR. If configured as CTS, the MK5025 will transmit all 1's while CTS is high.

RD. ***Receive Data*** (Input). Received serial data input.

A<23 : 16> (Output ; 3-State). Address bits <23 : 16> used in conjunction with DAL <15 : 00> to produce a 24-bit address. MK5025 drives these lines only as a Bus Master.

DAL <15 : 08> (Input/Output ; 3-State). The time multiplexed Data/Address bus. For 16-bit operations, DAL <15 : 08> behaves similar to DAL <07 : 00> above for the high byte of data or the middle byte of the 24-bit address. For 8-bit operations,

DAL <15 : 08> behaves similar to A <23 : 16> for the middle byte of the 24-bit address only.

V_{SS}. Digital circuit ground pins.

V_{CC}. Main power supply pin (5V ± 5%).

OPERATIONAL DESCRIPTION

The SGS-THOMSON X.25 Link Controller (MK5025) device is a VLSI product intended for data communication applications requiring X.25 link level control (LAPB). The MK5025 will perform all frame formating, such as frame delimiting with flags, FCS generation and detection, as well as zero-bit insertion and delection for transparency. The MK5025 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple packets. Contained in the buffer management is an on-chip dual channel DMA : one channel for receive and one channel for transmit. The MK5025 handles all supervisory (S) and unnumbered (U) frames as shown in table 2 and table 3.

The MK5025 is intended to be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK5025 is shown in Figure 3.

The MK5025 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. An I/O acceleration processor can be used to off-load Network Level software from the Host. The I/O acceleration processor in Figure 3 is recommended, but not required.

All signal pins on the MK5025 independent of the physical interface. As shown in Figure 3, line drivers and receivers are used for electrical connection to the physical layer.

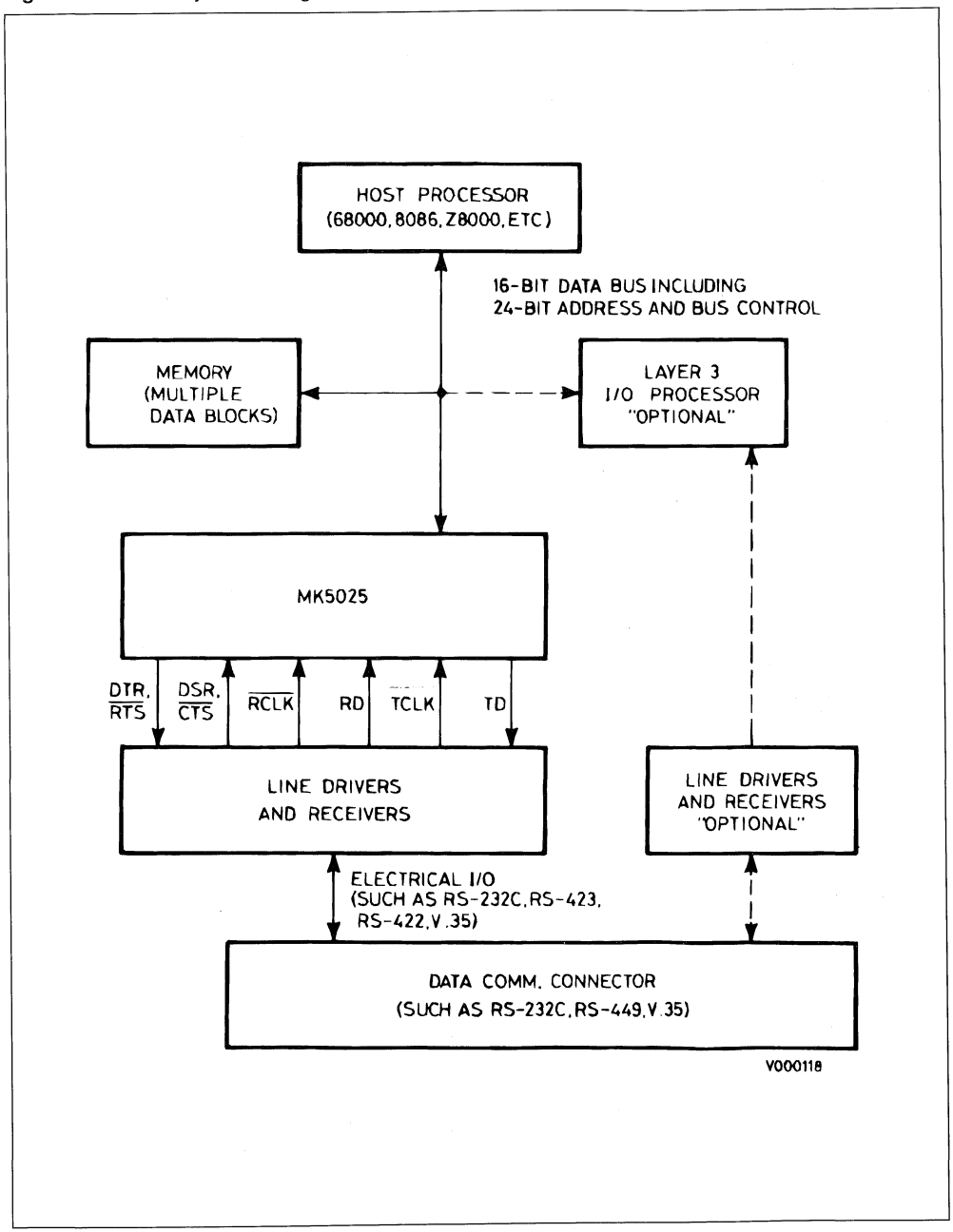
The MK5025 is mode up of functional blocks shown in Figure 4 and the MK5025 is made up of functional blocks shown in Figure 4 and described in the following paragraphs.

Microcontroller.

The microcontroller is the brain of the MK5025. It controls all of the other blocks and contains most of the protocol processing. All frame content processing as well as S and U frame processing and generation is performed by the microcontroller. All primitive processing and generation is also done here. The microcode ROM contains the control program for the microcontroller.

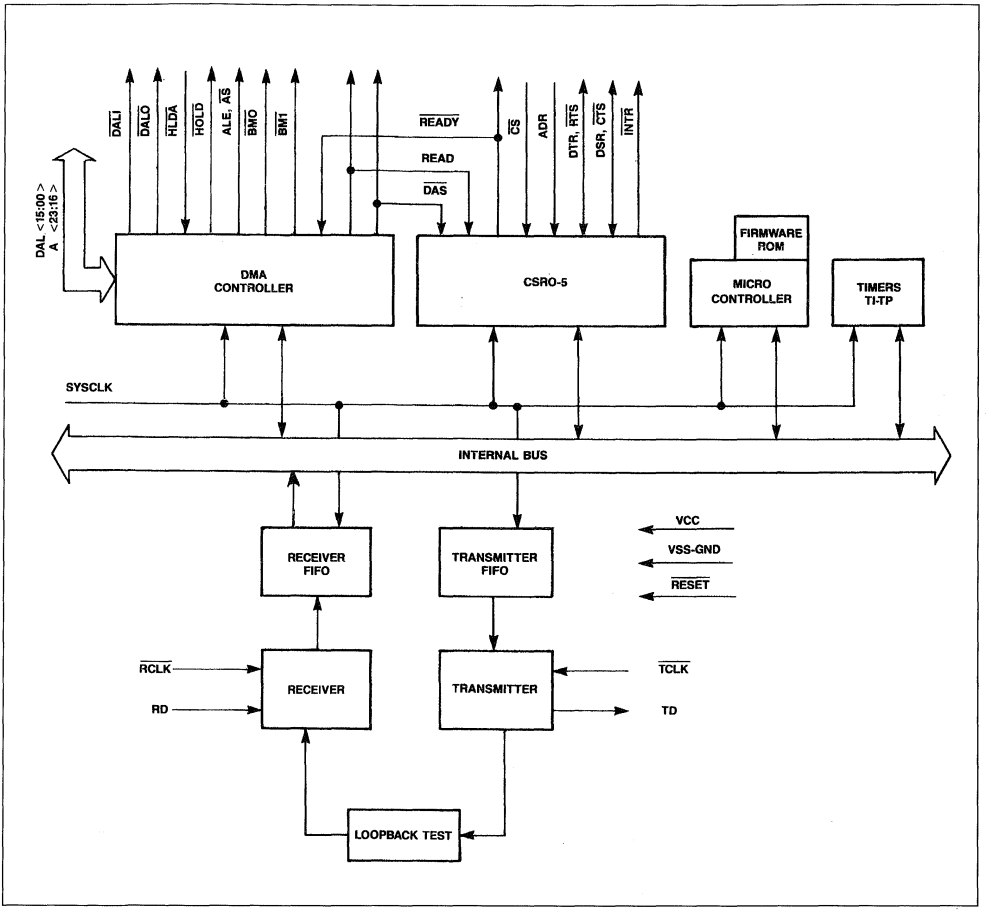
OPERATIONAL DESCRIPTION (continued)

Figure 3 : Possible System Configuration for the MK5025.



OPERATIONAL DESCRIPTION (continued)

Figure 4 : Simplified Block Diagram.



The MK5025 can interface with the host bus in two ways : either as bus master or as a bus peripheral. The MK5025 contains a dual channel DMA on chip to handle data transfers to and from the host memory. All access to the initialization block and descriptor rings is handled in this way. The address but is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations, this allows easy interfacing with both 8 and 16 bit processors. DMA transfers can be up to 1, 8 or an unlimited number of words per-transfer under program control. In bus slave mode the MK5025 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status, and more. Bus slave mode also allows both 8 and 16-bit accesses.

DMA Controller.

The MK5025 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK5025 requires access to the host memory it will negotiate

OPERATIONAL DESCRIPTION (continued)

for mastership of the bus. Upon gaining control of the bus the MK5025 will begin transferring data to or from memory. The MK5025 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case it will complete all bus transfers before releasing bus mastership back to the host. If, during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK5025 will release ownership of the bus immediately and the MERR bit will be set in CSRO. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode th limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode, it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed seperately for data and control information. Data information is defined as all contents of data buffers ; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see "Control and Status Register 4" description.

Serial Interface.

The MK5025 provides two seperate serial channels ; one for received data and one for transmitted data. These serial channels are completely seperate and may be run at different clock frequencies up to 7MHz. The receiver is responsible for recognizing frame boundaries, removal of inserted zeroes (for transparency), and checking the incoming FCS. Frames with incorrect FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring. The receiver also recognizes link idle and frame abort sequences. The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data. The transmitter generates flag sequences for interframe fill, at least two flags are transmitted between adjacent frames. The FCS calculations for both directions of serial data optionally follow either the 16-bit CRC-CCITT or the 32-bit CRC-32 algorithms. FCS generation and checking can also be optionally disabled if defined.

Receiver. Serial receive data comes into the Receiver (figure 4). The Receiver is responsible for :

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (Frame Check Sequence).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver-Over-Run.
7. Odd byte detection. If frames are received that have an odd number of bytes in the information field, the last byte of the frame is said to be an odd byte.
8. Detection of non-octet aligned frames, such frames are treated as invalid frames.

Transmitter. The Transmitter is responsible for :

1. Serialization of outgoing data.
2. Generating and appending the FCS.
3. Generation of interframe time-fill as either flags or idle.
4. Zero bit insertion for transparency.
5. Transmitter-Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS Control.

Frame Check Sequence. The FCS on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are :

- Transmitted Polarity : inverted
- Transmitted Order : High Order Bit First
- Pre-set Value : All 1's
- Polynominal 16 bit : X16 + X12 + X5 + 1
- Remainder 16 bit (if received correctly) : high order bit → 0001 1101 0000 1111
- Polynominal 32 bit : X32 + X26 + X23 + X22 + X16 + X12 + X11 + X10 + X8 + X7 + X5 + X4 + X2 + X + 1
- Remainder 32 bit (if received correctly) : high order bit → 1100 0111 0000 0100 1101 1101 0111 1011

OPERATIONAL DESCRIPTION (continued)

Receive FIFO. The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 2 bytes ; 18 or more bytes ; 34 or more bytes ; or 50 or more bytes. This programmability, along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK5025 must use the host bus. For more information, see Control and Status Register 4 description.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK5025 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

Transmit FIFO. The Transmit FIFO buffers the data to be transmitted by the MK5025. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to read data from the host's memory buffers in bursts ; making both the MK5025 and the host bus more efficient.

The transmit FIFO has a watermark scheme similar to the one described for the receive FIFO above. The transmit FIFO will not interrupt the microcontroller for service until it empties enough to reach the watermark level. The watermark can be programmed in CSR4 as: any space available, 18 bytes of space available, 34 bytes of space available, or 50 bytes of space available. The transmission of data however, will begin as soon as the FIFO has at least word of data

Bus Slave Circuitry

The MK5025 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in the Control and Status Registers section and the bus signal timing is described in figures 9 and 10.

Buffer Management

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in words (16 bits).

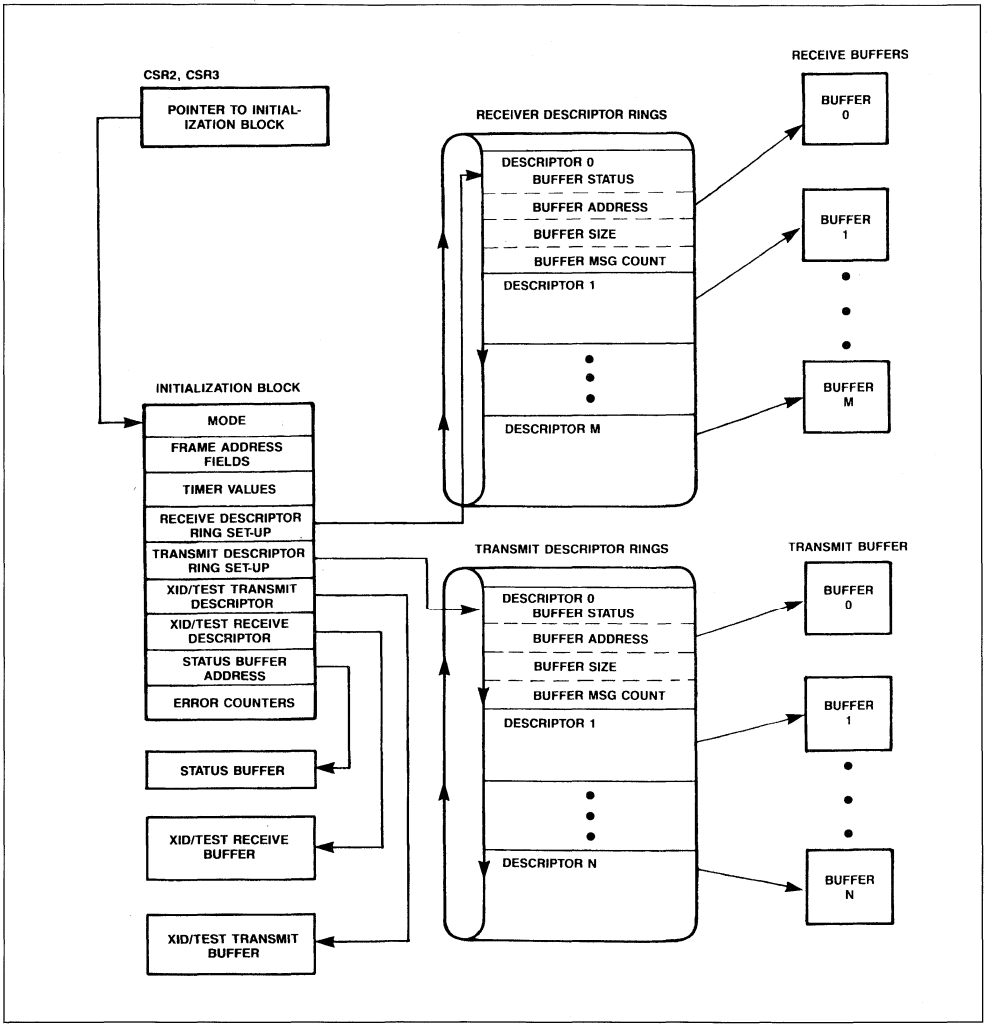
Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION Processor (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the .buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the Mk5025 does not own a receive buffer, it will not place received data in that buffer.

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the packet is too long for one buffer, the next buffer will be used after filling the first buffer ; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc.

OPERATIONAL DESCRIPTION (continued)

Figure 5 : Buffer Management Organization.



The Initialization Block. Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 28 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST or I/O acceleration processor, and is accessed by MK5025 during initialization. The Initialization Block is comprised of :

A. Mode of Operation.

B. Frame Address Values.

C. Timer Preset Values.

D. Location and size of Receive and Transmit Descriptor Rings.

E. Location and size of XID/TEST Buffers.

F. Location of status buffer.

G. Error Counters.

OPERATIONAL DESCRIPTION (continued)

The Circular Queue. The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5025. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5025, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5025 owns the buffer, the MK5025 is allowed and commanded to transmit the buffer. When the MK5025 does not own the buffer, it will not transmit that buffer. For receive, when the MK5025 owns a buffer, it may place received data into that buffer. Conversely, when the MK5025 does not own a receive buffer, it will not place received data in that buffer.

The MK5025 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5025 tests the next segment in the descriptor ring in a "look ahead" manner. If the frames are too long for one buffer, the next buffer will be used after filling (or transmitting) the first buffer ; that is, "chained". The MK5025 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, frame Address field, and etc. The starting address for the Initialization, IADR, is defined in the CSR2 and CSR3 registers inside the MK5025.

Frame Format. The frame format used by the MK5025 is shown below. Each frame consists of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field (not in all frames), an FCS of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags is programmable through the Mode Register in the Initialization Block. Received frames may have only one flag between adjacent frames.



Transmitted First

The Command/Response Repertoire. The command/response repertoire of the MK5025 is shown in tables 2 and 3. This set conforms to the ISDN LAPD, which is a super-set of X.25 Link Level. The MK5025 will process the S and U frames shown in table 1 and will handle the A and C fields for all I and UI frames.

Table 1 : Frame Types Symbols Definitions.

Name	Definition
I	Information frame
UI	Unnumbered Information
RR	Receiver Ready
DISC	Disconnect
RNR	Receiver Not Ready
UA	Unnumbered Acknoledge
REJ	Reject
FRMR	Frame Reject
SABM	Set Asynchronous Balance Mode
DM	Disconnect Mode
XID	Exchange Identification
TEST	Link Test frame

OPERATIONAL DESCRIPTION (continued)

Table 2 : Command/Response Repertoire - Module 8 Operation.

Format	Command	Resp	Encoding							
			1	2	3	4	5	6	7	8
Information Transfer	I		0	←	N(S)	→	P	←	N(R)	→
Supervisory	RR	RR	1	0	0	0	P/F	←	N(R)	→
	RNR	RNR	1	0	1	0	P/F	←	N(R)	→
	REJ	REJ	1	0	0	1	P/F	←	N(R)	→
Unnumbered	SABM		1	1	1	1	PF	1	0	0
		DM	1	1	1	1	F	0	0	0
	XID (1)	XID (1)	1	1	1	1	P/F	1	0	1
	UI (1)	UI (1)	1	1	0	0	P/F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
	TEST (2)	TEST (2)	1	1	0	0	P/F	1	1	1

Table 3 : Command/Response Repertoire - Modulo 128 Operation.

Format	Command	Resp	Encoding									
			1	2	3	4	5	6	7	8	9	10-1
Information Trasfer	I		0	N(S)							P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SABME		1	1	1	1	P/F	1	1	0		
		DM	1	1	1	1	F	0	0	0		
	XID (1)	XID (1)	1	1	1	1	P/F	1	0	1		
	UI (1)	UI (1)	1	1	0	0	P/F	0	0	0		
	DISC		1	1	0	0	P	0	1	0		
		UA	1	1	0	0	F	1	1	0		
		FRMR	1	1	1	0	F	0	0	1		
	TEST (2)	TEST (2)	1	1	0	0	P/F	1	1	1		

Notes :
1. XID and UI frames can be individually enabled for compatibility with X.32 and LAPD respectively.
2. TEST frames are enabled with XID frames.
3. N(S) = Transmitter Send sequence number.
4. N(R) = Transmitter Receive sequence number.
5. P/F = Poll bit when issued as a command, Final bit when issued as a response.

Protocol. The MK5025 contains a full implementation of the 1984 CCITT X.25 data link layer. It allows both basic and extended control fields, variable window sizes, and user-defined counter and timer values. Extended addressing and UI frames are optionally available for use in ISDN LAPD applications. XID and TEST frames are available for use in X.32. The interface between the MK5025 and the host (layer 3) conforms to both the ISO data link services standard and the ISDN LAPD data link services standard.

PROGRAMMING SPECIFICATIONS

This section defines the Control and Status Registers and the memory data structures required to program the MK5025.

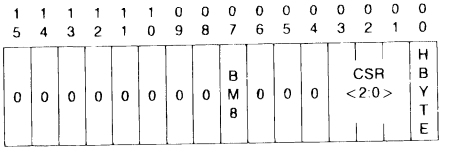
Control and Status Registers.

There are six Control and Status Registers (CSR's) resident within MK5025. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP). Thus the MK5025 needs only two address locations in the system memory or I/O map.

Accessing the Control and Status Registers. The CSR's are read (or written) in a two-step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction. During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

ADR	PORT
HIGH	Register Address Port (RAP)
LOW	Register Data Port (RDP)

Register Address Port (RAP)



Bit <15 : 08>. They are reserved and must be written as zeroes.

Bit 07, BM8. When set, places chip into 8-bit mode. CSR's, Init Block and data transfers are all 8-bit transfers, this provides compatibility with 8-bit microprocessors. When clear, all transfers are 16-bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is Read/Write and cleared on Bus Reset.

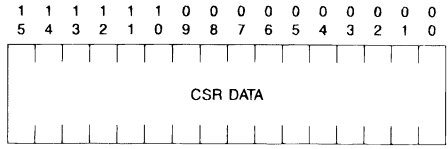
Bit <06 : 04>. They are reserved and must be written as zeroes.

Bit <03 : 01>, CSR <2 : 0>. CSR address select bits is Read/Write. Selects the CSR to be accessed through the RDP RAP is cleared by Bus Reset.

CSR<2 : 0>	CSR Selected
0	CSR0
1	CSR1
2	CSR2
3	CSR3
4	CSR4
5	CSR5

Bit 00, HBYTE. Determines which byte is addressed for 8-bit operation. If set, the high byte of the register referred to by CSR <2 : 0> is addressed, otherwise the low byte is addressed. This bit is only meaningful for 8-bit operation and must be written as zero if BM8 = 0. HBYTE is Read/Write and cleared on Bus Reset.

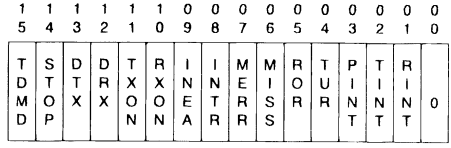
Register Data Port (RDP)



Bit <15 : 00>, CSR DATA. Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

Control and Status Register 0 (CSR0)

RAP <3 : 1> = 0



PROGRAMMING SPECIFICATIONS (continued)

Bit 15, TDMD. TRANSMIT DEMAND, when set, causes MK5025 to access the Transmit Descriptor Ring without waiting for the transmit polltime interval to elapse. TDMD need not be set to transmit a frame, it merely hastens MK5025's response to a Transmit Descriptor Ring entry insertion by the host. TDMD is WRITE WITH ONE ONLY and cleared by the MK5025 after it is used. It may read as a "1" for a short time after it is written because the MK5025 may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.

Bit 14, STOP. STOP, when set, indicates that MK5025 is operating in the STOPPED phase of operation. All external activity is disabled and internal logic is reset. MK5025 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.

Bit 13, DTX. Transmitter Ring Disable prevents the MK5025 from further access to the Transmitter Descriptor Ring. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. DTX is READ/WRITE. TXON acknowledges changes to DTX, see below.

Bit 12, DRX. Receiver Ring Disable prevents the MK5025 from further access to the Receiver Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. If DRX is set while a data link is established the MK5025 will go into the local busy condition and will send a RNR response frame to the remote station. Upon clearing DRX the MK5025 will send a RR response frame. DRX is READ/WRITE. RXON acknowledges changes to DRX, see below.

Bit 11, TXON. TRANSMITTER ON indicates that the transmitter ring access is enabled. TXON is set as the START primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by issuing a STOP primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY ; writing this bit has no effect.

Bit 10, RXON. RECEIVER ON indicates that the receiver ring access is enabled. RXON is set as the START primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a STOP primitive in CSR1, or by a Bus RESET. If RXON is clear, the host may modify the Receive Descriptor Ring entries regardless of the state of the OWNA bits. RXON is READ ONLY ; writing this bit has no effect.

Bit 09, INEA. INTERRUPT ENABLE allows the INTR I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 the INTR I/O pin will be low if CSR0 <08> INTR is set. If INEA = 0 the INTR I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE, set by writing a "1" into this bit and is cleared by writing a "0" into this bit or by Bus RESET or by issuing a STOP primitive.

Bit 08, INTR. INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occured ; MISS, MERR, RINT, TINT, PINT, TUR or ROR. If INEA = 1 and INTR = 1 the INTR I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a STOP primitive.

PROGRAMMING SPECIFICATIONS (continued)

Bit 07, MERR. MEMORY ERROR sets when MK5025 is the Bus Master and has not received READY within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the receiver and transmitter are turned off and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.

Bit 06, MISS. MISSED PACKET is set when the receiver loses a packet because it does not own a receive buffer, indicating loss of a frame. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by the MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 05, ROR. RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. The frame being received is lost but is recoverable according to the Link Level protocol. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 04, TUR. TRANSMITTER UNDERRUN indicates that the MK5025 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by the MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 03, PINT. PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive or to indicate a User Primitive Error Condition. See CSR1<15> UERR. When PINT is set, an interrupt is generated if INEA = 1. PINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

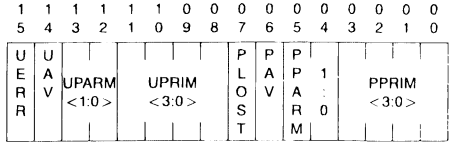
Bit 02, TINT. TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit descriptor Ring. This occurs when a transmitted frame has been acknowledged by the remote station. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a STOP primitive.

Bit 01, RINT. RECEIVER INTERRUPT is set after MK5025 updates an entry in the Receive Descriptor Ring. This occurs when the MK5025 has received a correct frame from the remote station. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by MK5025 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a STOP primitive.

Bit 00. Reserved. This bit is READ ONLY.

Control and Status Register 1 (CSR1)

RAP <3 : 1> = 1



PROGRAMMING SPECIFICATIONS (Continued)

Bit 15, UERR. USER PRIMITIVE ERROR is set by the MK5025 when a primitive issued by the user is in conflict with the current status of the link. UERR is READ/CLEAR ONLY and is set by MK5025 and cleared bywritig a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.

Bit 14, UAV. USER PRIMITIVE AVAILABLE is set by the user after a primitive has been placed in UPRIM. It is cleared by the MK5025 after the primitive has been processed. This bit is also cleared by a Bus RESET.

Bit < 13 : 12>, UPARM. UPARM is written by the host in conjunction with the user primitives in UPRIM. This user parameter field provides for the information to the MK5025 concerning the corresponding user primitive. For connect and reset primitives this field determines what the MK5025 will do with frames in the transmit descriptor ring that have been previously sent but not aknowledged. If UPARM = 0, these frames will be resent when the new link is established. If UPARM = 1, these frames are discarded by the MK5025 and their OWNA bits are cleared, releasing ownership back to the host. For all other primitives this field should be written with zeroes, unless otherwise indicated.

Bit < 11 : 08>, UPRIM. USER PRIMITIVE is written by the user to control the MK5025 link procedures. The following values are valid:

0 Stop - Instructs MK5025 to go into STPPED Mode. All link activity is terminated and the STOP bit is set. Transmitter outputs all "1"s. All DMA activity ceases.

1 Start-Instructs MK5025 to exit STOPPED Mode and enter the Disconnected Phase. Descriptor Rings are reset. Transmitter begins outputting flags. Issuring a Start primitive with UPARM = 1 will put the MK5025 directly into the Information Transfer phase, just as if it had received UA in response to SABM. Valid only in STOPPED Mode, or Transparent Mode.

2 Init Request - Instructs MK5025 to read the initialization block. Valid only in STOPPED Mode and Disconnected Phase. This should be performed prior to the start primitive after a bus reset or powerup.

3 Trans - Instructs MK5025 to enter the Transparent phase of operation. Data frames are transmitted and received out of the descriptor rings but no protocol processing is done. Address and Control Fields are not prepended to the frames, but FCS processing works normally. If the PROM bit is set in CSR2 then no address filtering is performed on received frames. Transparent Mode may be exited only with a stop primitive or by bus reset.

4 Status Request - Instructs MK5025 to write the current link status into the STATUS buffer. Valid only if INIT primitive has previously been issued.

5 Self - Test Request - Instructs MK5025 to perform a self test. Valid only in STOPPED Mode. See page 31/40 for self-test procedure.

6 Connect request - Instructs MK5025 to attempt to establish a logical link with the remote site. Valid only in Disconnected Phase.

7 Connect Response - Indicates willingness to establish a logical link with the remote site. Valid only in Disconnected Phase after receiving a Connect indication primitive.

PROGRAMMING SPECIFICATIONS (continued)

8 Reset Request - If a logical link has been established, instructs MK5025 to attempt to reset the current logical link with the remote site (sends SABM/E). In Transparent Mode or Disconnected Phase, instructs MK5025 to start the T1 timer.

9 Reset Response - If a logical link has been established, indicates willingness to reset current logical link with remote site (valid only after receiving a Reset Indication primitive.) In Transparent Mode or Disconnected Phase, instructs MK5025 to stop the T1 timer.

10 XID Request - Requests MK5025 to send an XID command to the remote site. Data in the XID/TEST Transmit buffer is used for the Data Field. Invalid in STOPPED Mode.

11 XID Response - Requests MK5025 to send an XID response to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Valid only after receiving an XID Indication primitive.

12 TEST Request - Requests MK5025 to send a TEST command to the remote site. Data in the XID/TEST Transmit Buffer is used for the Data Field. Invalid in STOPPED Mode.

13 TEST Response - Requests MK5025 to send a TEST response to the remote site. Data in the XID/TEST transmit buffer is used for the data field. Valid only after receiving a TEST indication primitive.

14 Disconnect Request - Requests MK5025 to disconnect the current logical link. Invalid in STOPPED Mode. A DM response with the F bit clear will be sent if the link is currently disconnected.

Bit 07, PLOST. PROVIDER PRIMITIVE LOST is set by MK5025 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared and by a Bus RESET. Writing to this bit has no effect.

Bit 06, PAV. PROVIDER PRIMITIVE AVAILABLE is set by the MK5025 when a new provider primitive has been placed in PPRIM. PPRIM is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET.

Bit <05 : 04>, PPARM. PROVIDER PARAMETER provides additional information about the reason for the receipt of a disconnect, reset or error indication primitive. This field is undefined for other provider primitives. Parameters are as follows :

PPARM	Disconnect Indication	Disconnect Confirmation	Reset Indication	Error Indication
0	Remotely Initiated	UA or DM F = 1 Recvd	Remotely Initiated	Unsolicited DM/F = 0 Recvd
1	SABM Timeout	DISC Timeout		Timer Recovery Timeout
2	FRMR Sent then DISC or DM Received T3 Timeout		FRMR Sent then SABM/E Recvd	FRMR Received
3		T3 Timeout		Unsolicited UA or F bit Received

PROGRAMMING SPECIFICATIONS (continued)

Bit <03 : 00>, PPRIM. PROVIDER PRIMITIVE is written by MK5025 to inform the user of link control conditions. Valid Provider Primitives are as follows :

2 Init Confirmation - Indicates that the initialization has completed.

4 Error Indication - Indicates an error condition has occurred during the Information Transfer phase of operation that requires instruction by the Host for recovery. See PPARM for specific error conditions. Either a Reset Request or Disconnect Request primitive should be issued in UPRIM after receiving an Error Indication primitive.

5 Remote Busy Indication - Indicates change in Remote Busy status. PPARM = 0 indicates receipt of RNR - Remote Busy. PPARM = 1 indicates Remote no longer busy - RR received. This primitive is only issued if RBSY = 1. RBSY (bit 15 of IADR + 16) is set by the Host in the Init block.

6 Connect Indication - Indicates an attempt by the remote site to establish a logical link. Appropriate user responses are Connect Response or Disconnect Request.

7 Connect Confirmation - Indicates the success of a previous Connect Request by the user. A logical link is now established.

8 Reset Indication - If a logical link has been established, indicates an attempt by the remote site to reset the current logical link. Appropriate user responses are Reset Response or Disconnect Request. In Transparent Mode, or Disconnected Phase, indicates expiry of timer T1.

9 Reset Confirmation - Indicates the success of a previous Reset Request by the user. The current logical link has now been reset.

10 XID Indication - Indicates the receipt of an XID command. The Data Field of the XID command is located in the XID/TEST Receive Buffer.

11 XID Confirmation - Indicates the receipt of an XID response. The Data field of the XID response is located in the XID/TEST Receive Buffer.

12 TEST Indication - Indicates the receipt of a TEST command. The Data Field of the TEST command is located in the XID/TEST Receive buffer.

13 TEST Confirmation - Indicates the receipt of a TEST response. The Data field of the TEST response is located in the XID/TEST Receive Buffer.

14 Disconnect Indication - Indicates a request by the remote site to disconnect the current logical link or the refusal of a previous Connect or Reset Request. The chip is now in the Disconnected Phase.

15 Disconnect Confirmation - Indicates the completion of a previously requested link disconnection.

Control and Status Register 2 (CSR2)

RAP <3 : 1> = 2

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	FRMRD	T203E	X75E	PROM	UIE	XIDE	IADR<23:16>							

Bit <15 : 14>. Reserved, must be written as zeroes.

Bit 13, FRMRD. Setting this bit disables the sending of FRMR frames (used for LAPD applications) ; otherwise the MK5025 behaves as specified for X.25. This bit is READ/WRITE.

Bit 12, T203E. If this bit is set, the T3 timer is reconfigured to behave as specified for LAPD T203 timer ; otherwise it behaves as specified for X.25. This bit is READ/WRITE.

PROGRAMMING SPECIFICATIONS (continued)

Bit 11, X75E. X.75 mode is enabled if this bit is set to 1 ; otherwise X.25 mode is enabled. This bit is READ/WRITE.

Bit 10, PROM. Address filtering is disabled for transparent mode, if this bit is set. All uncorrupted incoming frames are placed in the Receive Descriptor Ring. This bit is READ/WRITE. Should be set only in Trans Mode.

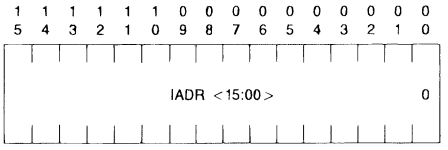
Bit 09, UIE. UI frames are recognized only if this bit is set. If UIE = 0 all received UI frames will not be recognized. This bit is READ/WRITE.

Bit 08, XIDE. XID frames are recognized only if this bit is set. If XIDE = 0 all received XID frames will not be recognized. This bit is READ/WRITE.

Bit <07 : 00>, IADR. The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

Control and Status Register 3 (CSR3)

RAP <3 : 1> = 3



BIT <15 : 00>, IADR. The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization Block must be on an even byte boundary.

Control and Status Register 4 (CRS4). CRS4 allows redefinition of the bus master interface.

RAP <3 : 1> = 4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	FWM <1:0>		BAEN	BUSR	BSWPC	BURST	1 : 0	BSWPD	ACON	BCON

Bit <15 : 10> Reserved, must be written as zeroes.

Bit <09 : 08>, FWM. These bits define the FIFO watermarks. FIFO watermarks prevent the MK5025 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive data, data will only be transferred to the data buffers after the FIFO has at least N 16-bit words or an end of frame has been reached. Conversely, for transmit data, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows :

FWM :0	N
11	1word
10*	9 words
01	17 words
00	25 words

* Suggested Setting

Bit 07, BAEN. This bit should be written as "0" for standard operation as described in the timing diagrams in figures 7 and 8 of this manual. If this bit is set, the upper 4 address bits (A <23 : 20>) will be available at the time HOLD is asserted, and are never tristated. This facilitates use in multiple bus systems to identify which bus is being requested.

Bit 06, BUSR. If this bit is set, pin 15 becomes input BUSREL. If this bit is clear pin 15 is either BM0 or BYTE depending on bit 00. For more information see the description for pin 15 earlier in this document. BUSR is READ/WRITE and cleared on Bus Reset.

Bit 05, BSWPC. This bit determines the byte ordering of all "non-data" DMA transfers. "Non-data" DMA transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows MK5025 to operate with

memory organizations that have bits <07 : 00> ar even addresses with bits <15 : 08> at odd addresses or vice versa.
With BSWPC = 1 :
Address
XX0 | 0 ••• 7 |
XX1 | 8 ••• 15 |
This memory organization is used with the LSI 11 and the 8086 microprocessors.
With BYTE SWAP = 0 :
Address
XX0 | 8 ••• 15 |
XX1 | 0 ••• 7 |
This memory organization is used with the 68000 and Z8000 microprocessors. BSWP is Read/Write and cleared by BUS RESET.

Bit <04 : 03>, BURST. This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on Bus RESET.

BURST <1 : 0>	8 bit Mode	16 bit Mode
00	2 bytes	1 word
10*	16 bytes	8 words
01	unlimited	unlimited

* Suggested Setting

Bit 02, BSWPD. This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.

Bit 01, ACON. ALE CONTROL defines the assertive state of Pin 18 when MK5025 is a Bus Master. ACON is READ/WRITE and cleared by Bus RESET.

ACON	Pin 18	Asserted
0	ALE	High
1	AS	Low

Bit 00, BCON. BYTE CONTROL redefines the Byte Mask and Hold I/O pins. BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN 16	PIN 15	PIN 17
0	BM 1	BM 0	HOLD
1	BUSAKO	BYTE	BUSRQ

Control and Status Register 5 (CSR5).CSR5 facilitates control and monitoring of modem controls.

RAP <3 : 1> = 5

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	RTSEN	DTRD	DSRD	DTR	DSR

Bit <15 : 05>. Reserved, must be written as zeroes.

Bit 4, RTSEN. RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set pin 26 (DTR) becomes RTS and pin 30 (DSR) becomes CTS. RTS is driven low whenever the MK5025 has data to transmit and kept low during transmission. RTS will be driven high after the closing flag of a frame transmitted if either no other frames are in the FIFO or if the minimum frame spacing is higher than 2 (see Mode Register). The MK5025 will not begin transmission and TD will remain HIGH if CTS is high. Bit RTSEN should not be set when operating in Internal Loopback mode.

Bit 3, DTRD. DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR pin. If DTRD = 0, the DTR pin becomes an input pin and the DTR bit reflects the current value of the pin ; if DTRD = 1, the DTR pin is an output pin controlled by the DTR bit below.

Bit 2, DSRD. DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR pin. If DSRD = 0, the DSR pin becomes an input pin and the DSR bit reflects the current value of the pin ; if DSRD = 1, the DSR pin is an output pin controlled by the DSR bit below.

Bit 1, DTR. DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR pin.

Bit 0, DSR. DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR pin. If DSRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DSR pin.

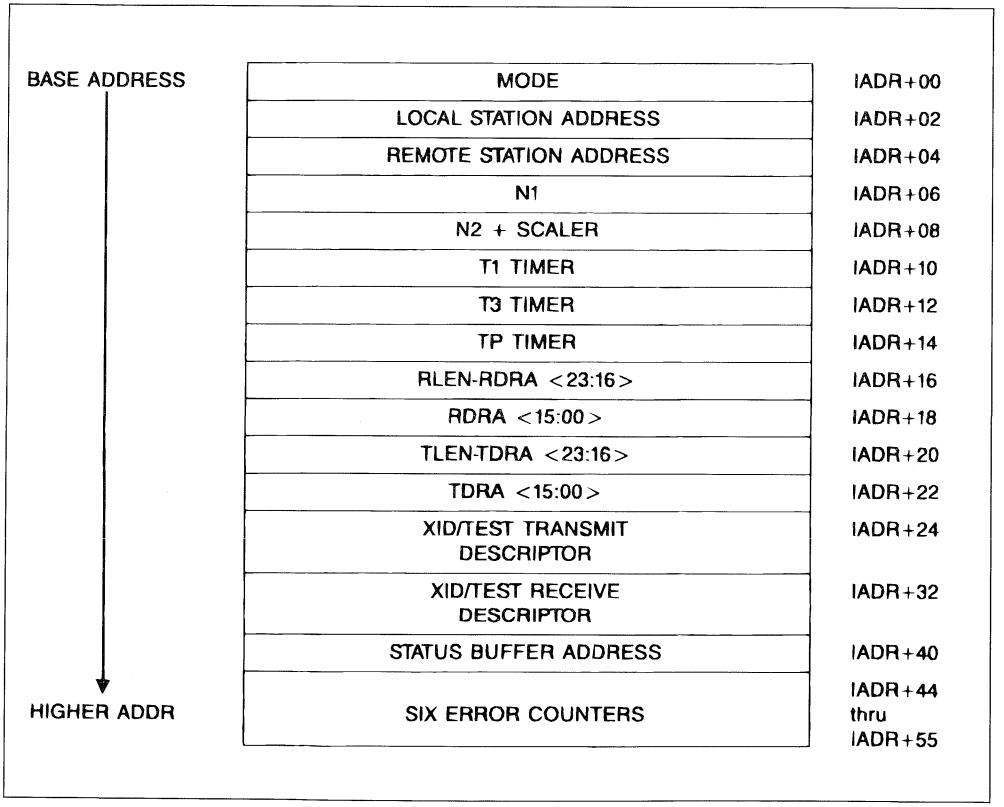
Initialization Block

MK5025 initialization includes the reading of the initialization block in memory to obtain the operating parameters.

The Initialization Block is read by MK5025 when receiving an INIT primitive. During normal initialization the INIT should be sent prior to sending a START primitive. The user may re-issue the INIT primitive after a START, but received frames may be lost if care is not taken. An INIT cannot be issued while a link is connected ; MK5025 will reject such an attempt.

Except for the Error Counters and XID/TEST Descriptor OWNA bits, the MK5025 will not write into the Initialization Block.

Figure 6 : Initialization Block.



Mode Register. The Mode Register allows alteration of the MK5025's operating parameters.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
MFS <4:0>					EXTCF	EXTAF	DACE	EXTC	EXTA	DRFCS	DTFCS	FCSS	LBACK <2:0>		

Bit <15 : 11>, MFS <4 :0>. Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK5025. This only affects frames transmitted by the MK5025 and does not restrict the spacing of frames received by the MK5025. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See following table for encoding of this field.

Number of Flags	MFS <4:0>
1	1
2	0
4	2
6	4
8	9
10	18
12	5
14	11
16	22
18	12
20	25
22	19
24	7
26	15
28	31
30	30
32	28
34	24
36	17
38	3
40	6
42	13
44	27
46	23
48	14
50	29
52	26
54	21
56	10
58	20
60	8
62	16

Bit 10, EXTCF. Extended Control Force is useful only in transparent mode operation. If set along with EXTC, the receiver will assume the control field to be two octets long regardless of the first two bits of the control field. See EXTC below.

Bit 09, EXTAF. Extended Address Force is useful only in transparent mode operation. If set along with EXTA, the receiver will assume the address field to be two octets long regardless of the first bit of the address. See EXTA below.

Bit 08, DACE. Address and control field extraction are disabled when DACE is set. Address and control fields are treated as normal data. DACE must be written as "0" for normal operation in non-transparent mode.

Bit 07, EXTC. Extended Control Field is enabled when EXTC = 1. The control fields of all S and I frames become two octets in length, instead of one. The numbering for I frames becomes modulo 128, instead of modulo 8. The control field of U frames remains one octet in length.

Bit 06, EXTA. Extended address is enabled when EXTA = 1. The length of address fields is determined by the first bit of the address. If the first bit is set then the address field is 1 octet long otherwise it is 2 octets.

Bit 05, DRFCS. Disable Receiver FCS. When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct.

Bit 04, DTFCS. Disable Transmitter FCS. When DTFCS = 0, the transmitter will generate and append the FCS to each frame. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames.

Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.

Bit 03, FCSS. FCS Select. When FCSS = 1, a 16 bit FCS is selected otherwise a 32-bit FCS is used.

Bit <02 : 00>, LBACK. Loopback Control puts the MK5025 into one of several loopback configurations.

LBACK0. Normal operation. No loopback.

LBACK4. Simple loopback. Receive data and clock are driven internally by transmit data and clock.

LBACK5. Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.

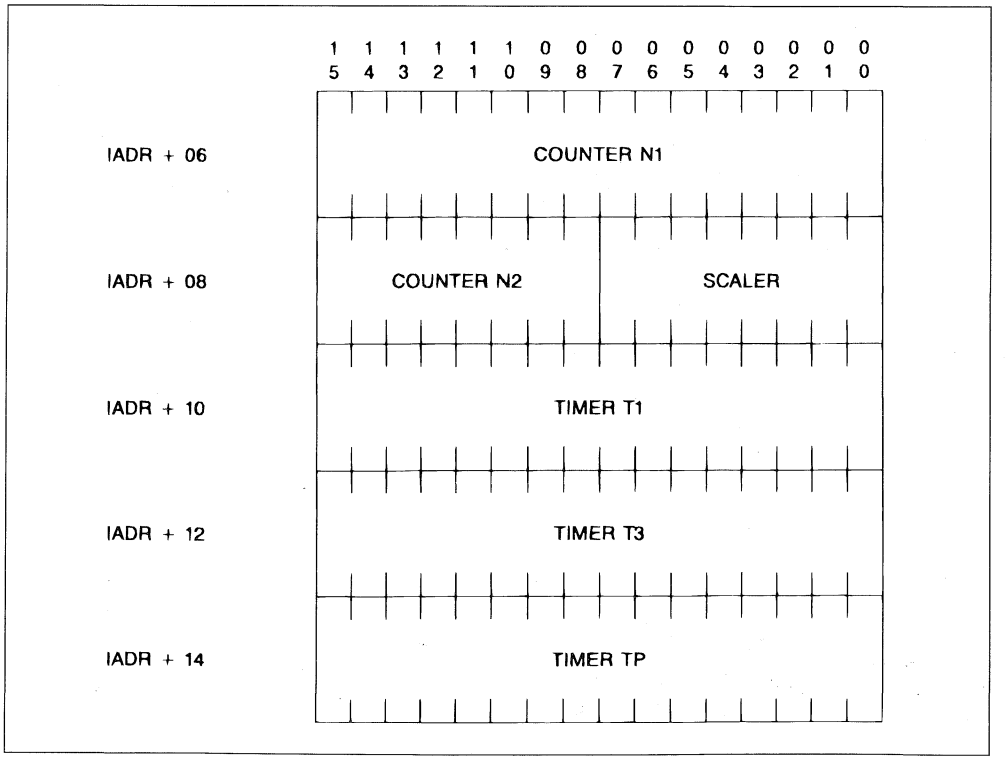
LBACK6. Silent loopback. Same as simple loopback with TD pin forced to all ones.

LBACK7. Silent Clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. TD pin is forced to all ones.

Station Addresses. The Local and Remote station addresses may be either one or two octets according to the EXTA control bit described in the MODE register. If extended address mode is selected bit 0 should be set to a zero for adherence to ADCCP/HDLC. If extended address mode is not selected, the command and response frame addresses should be located in the lower order byte of their respective fields. When operating in Loopback mode, Station addresses must be the same.

Timers. There are 5 independent counter-timers. The lower 8 bits of IADR + 08 are used as a scaler for T1, T3, and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is a 16 bit counter and is used to count the number of bytes in an I-frame. N2 is an 8 bit counter.

The Host will write the period of N1, N2, T1, T3, and TP into the Initialization Block.



N1. MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame received that exceeds this count will be discarded.

N2. MAXIMUM RETRANSMISSION COUNT. This field must contain the two's complement of one less than the maximum number of retransmissions that will be made following the expiration of T1.

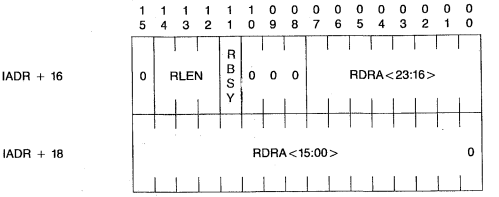
SCALER. TIMER PRESCALER. Timers T1, T3, and TP are scaled by this number. The prescaler incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field is interpreted as the two's complement of the prescaler period. Note : a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8224 clock pulses).

T1. RETRANSMISSION TIMER. Link control frames will be retransmitted upon the expiration of the T1 timer if the appropriate response is not received. These frames will be retransmitted up to N2 (see above) times, at which time the link will be disconnected or reset by MK5025 according to the X.25 protocol. This field must contain the two's complement of the period of timer T1. The scaled (see SCALER) value of T1 should be made large enough to allow the remote station to receive the control frame and send its response.

T3. LINK IDLE TIMER. The link idle timer determines the amount of link idle time necessary to consider the link disconnected. This field must contain the two's complement of the period of timer T3. T3 is disabled (but not T203) if CSR5 RTSEN = 1 or if the MK5025 is in transparent mode.

TP. TRANSMIT POLLING TIMER. This scaled timer determines the lenght of time between transmit frame polls. Unless TDMD (see CSR0) is set or a frame is received on the link, no attempt to transmit a frame in the transmit descriptor ring is made until TP expires. At TP expiration all transmit frames in the transmit descriptor ring will be sent. This field must contain the two's complement of the period of timer TP.

Receive Descriptor Ring Pointer



Bit 15. Reserved, must be written as a zero.

Bit <14 : 12>, RLEN. RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.

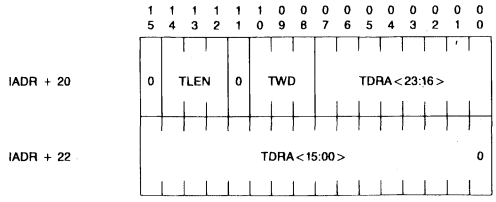
RLEN	Number of Entries
0	NA
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Bit 11 RBSY Setting this bit enables the generation of the Remote Busy Indication primitive (PPRIM = 5) whenever there is a change in the Remote Busy status.

Bit <10 : 08>. Reserved, must be written as zeroes.

Bit <07 : 00>/ <15 : 00>, RDRA. RECEIVE DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Receive Descriptor Ring. The Receive Ring must be aligned on a word boundary.

Transmit Descriptor Ring Pointer



Bit 15. Reserved, must be written as a zero.

Bit <14 : 12>, TLEN. TRANSIT RING LENGTH is the number of entires in the Transmit Ring expressed as a power of two.

Bit 11. Reserved, must be written as a zero.

Bit <10 : 08>, TWD. TRANSMIT WINDOW is the window size of the Transmitter as shown in the following table. TWD is the maximum number of I frames which may be transmitted without an acknowledgement. TWD is not allowed to be greater than 127.

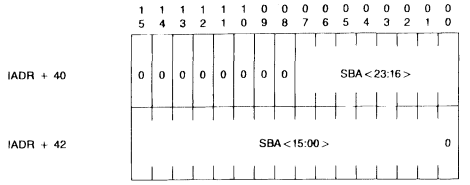
TLEN	Number of Entries
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

TWD	Window Size	
	EXTC = 0	EXTC = 1
0	NA	1
1	1	3
2	2	7
3	3	15
4	4	31
5	5	63
6	6	127
7	7	127

Bit <07 : 00>/ <15 : 00>, TDRA. TRANSMIT DESCRIPTOR RING ADDRESS is the base address of (lowest address) of the Transmit Descriptor Ring. The Transmit Ring must be aligned on a word boundary.

XID/TEST Descriptors. The XID/TEST Descriptors contain pointers to the buffers used to receive and transmit XID and TEST frames, as well as the buffer lengths. The exact format of these descriptors can be seen below under Receive and Transmit Message Descriptor Entry descriptions. They are used the same as other descriptors except that no data chaining is allowed.

Status Buffer Address



Bit <15 : 08>. Reserved, must be written as zeroes.

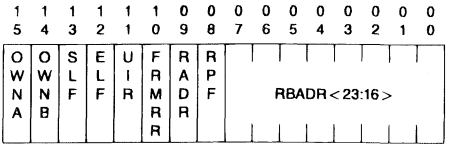
Bit <07 : 00>/ <15 : 00>, SBA. STATUS BUFFER ADDRESS points to a 7 word buffer into which link status information is placed upon the issuance of the STAT primitive by the HOST. The contents of the Status Buffer are described later in this document. The Status Buffer must begin on a word boundary.

Error Counters. Six locations in the initialization buffer are reserved for use as error counters which the MK5025 will increment. These are intended for use of the Host CPU for statistical analysis. The MK5025 will only increment the counters ; it is up to the user to clear and preset these counters. The error counters are :

MEMORY ADDRESS	ERROR COUNTER
IADR + 44	Bad frames received - Bad FCS - Non-Octet Aligned
IADR + 46	Number of FRMR frames received
IADR + 48	Number of T1 timeouts
IADR + 50	Number of REJ frames received
IADR + 52	Number of REJ frames transmitted
IADR + 54	Frames shorter than minimum length received

Receive and Transmit Descriptor Rings. Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

Receive Message Descriptor 0 (RMD0)



Bit 15, OWNA. When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided the received frame had a good FCS, N(r), and N(s). The Host sets the OWNA bit after emptying the buffer. Once the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

Bit 14, OWNB. This bit determines whether the HOST or the SLAVE PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.

Bit 13, SLF. Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the chip.
Note : *A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI or FRMR frame.*

Bit 12, ELF. End of Long Frame indicates that this the last buffer used by MK5025 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK5025.

Bit 11, UIR. UI Frame Received indicates that a UI frame has been received and is stored in this buffer.

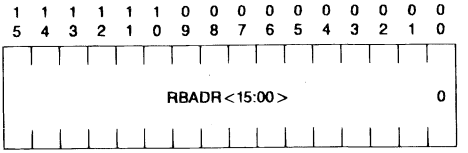
Bit 10, FRMRR. FRMR Received indicates that the I-field of a FRMR is stored in the buffer referenced by this Message Descriptor.

Bit 09, RADR. Valid only for frames received while in Transparent Mode with address filtering enabled. RADR indicates which of the 2 programmable addresses the frame matched. If set, the received address field matched the value in the Local Address field of the Initialization Block. Otherwise it matched the value in the Remote Address field.

Bit 08, RPF. Valid only for UI, XID and TEST frames. RPF equals the state of the P or F bit for the recvd frame.

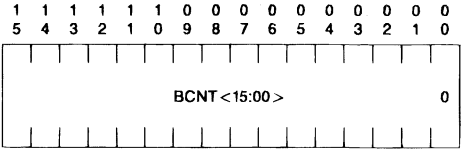
Bit <07 : 00>, RBADR. The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

Receive Message Descriptor 1 (RMD1)



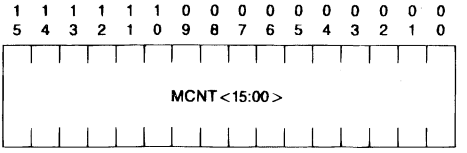
Bit <15 : 00>, RBADR. The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK5025. The receive buffers must be word aligned.

Receive Message Descriptor 2 (RMD2)



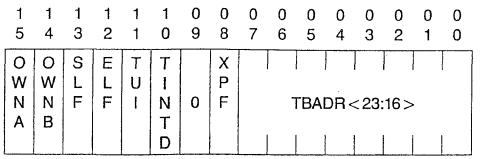
Bit <15 : 00>, BCNT. Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK5025. Buffer size must be even.

Receive Message Descriptor 3 (RMD3)



Bit <15 : 00>, MCNT. Message Byte Count is the length, in bytes, of the contents of the buffer expressed in two's complement. If ELF = 0, MCNT will equal the two's complement of BCNT since the MK5025 will fill a buffer before chaining to the next descriptor.

Transmit Message Descriptor 0 (TMD0)



Bit 15, OWNA. When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK5025 owns this descriptor. The host should set the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK5025 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the remote station. After the MK5025, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.

Bit 14, OWNB. This bit determines whether the HOST or the I/O ACCELERATION PROCESSOR owns the buffer when OWNA is a zero. The MK5025 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.

Bit 13, SLF. Start of Long Frame indicates that this is the first buffer used by MK5025 for this frame. It is used for data chaining buffers. SLF is set by the Host.
Note : A "Long Frame" is any frame which needs data chaining. Usually this will be an I frame, but it could also be a UI frame or others.

Bit 12, ELF. End of Long Frame indicates that this the last buffer used by MK5025 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host.

Bit 11, TUI. Transmit a UI frame indicates that a UI frame is to be transmitted from the transmit buffer instead of a normal I frame. This bit must also be set for anything transmitted while the MK5025 is in Transparent Mode.

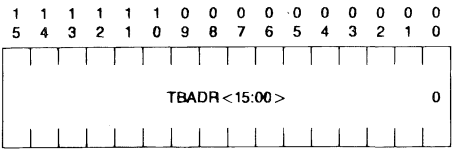
Bit 10, TINTD Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host. This allows users to limit the number of transmit interrupts.

Bit 09 Reserved, must be written as zeroes.

Bit 8, XPF. Transmit P/F bit instructs the MK5025 to send the corresponding frame with a particular value for the P/F bit. This bit should equal the desired value of the transmitted P/F bit. This bit is valid only for UI, XID and TEST frames and should be written with zero otherwise.

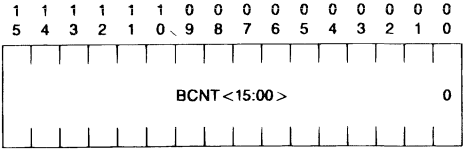
Bit <07 : 00>, TBADR. The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5025.

Transmit Message Descriptor 1 (TMD1)



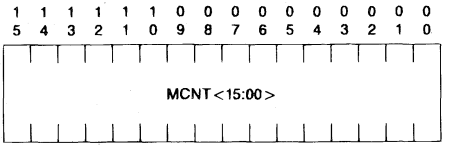
Bit <15 : 00>, TBADR. The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK5025. The least significant bit is zero since the descriptor must be word aligned.

Transmit Message Descriptor 2 (TMD2)



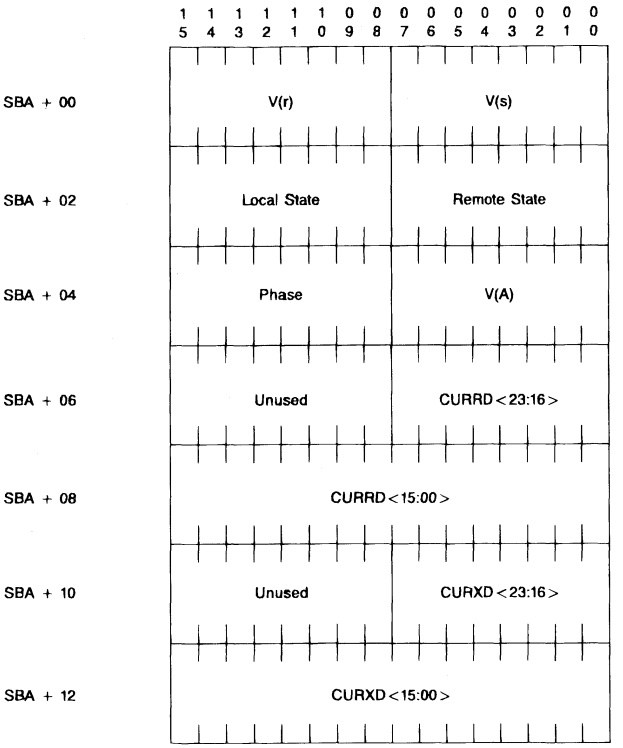
Bit <15 : 00>, BCNT. Buffer Byte Count is the usable length, in bytes, of the buffer pointed to by this descriptor in two's complement. This field is not used by the MK5025.

Transmit Message Descriptor 3 (TMD3)



Bit <15 : 00>, MCNT. Message byte count is the length, in bytes, of the contents of the buffer associated with this descriptor expressed as a two's complement.

Status Buffer



V(r). Current value of the Receive Count Variable. $0 \leq V(r) \leq 7$ for non-extended control ; $0 \leq V(r) \leq 127$ for extended control.

V(s). Current value of the Transmit Count Variable. $0 \Leftarrow V(s) \Leftarrow 7$ for non-extended control ; $0 \Leftarrow V(s) \Leftarrow 127$ for extended control.

Local State. Current state of local station.

Value	Description
0	Normal Data Transfer state
1	Local Busy state
2	REJ sent state
3	DISC sent state
4	Normal Disconnected state
5	SABM/E sent for link connection
6	FRMR sent state
7	SABM/E sent for link reset
8	Error Indication issued

Remote State. Current state of remote station.

Value	Description
0	Normal Data Transfer state
1	Remote Busy state

Phase. Current phase of operation.

Value	Description
– 1	Stopped Mode
0	Information Transfer phase
1	Disconnected phase
2	Resetting phase
3	Transparent Data Transfer phase

V(A). Current value of Transmit Acknowledge Count.. This field contains the value of the N(r) of the most recently received S or I frame. The modulo difference between V(A) and V(s) determines the number of outstanding I frames that have not been acknowledged by the remote station.

CURRD <23 : 00>. Current Receive Descriptor. This pointer indicates the position of the descriptor for the next receive buffer to be filled.

CURRXD <23 : 00>. Current Transmit Descriptor. This pointer indicates the position of the descriptor for the next transmit buffer to be transmitted.

Data Link Services

The MK5025 is consistent with the ISO Data Link Service Definition in providing services to the HOST. The following section is a brief description of this interface.

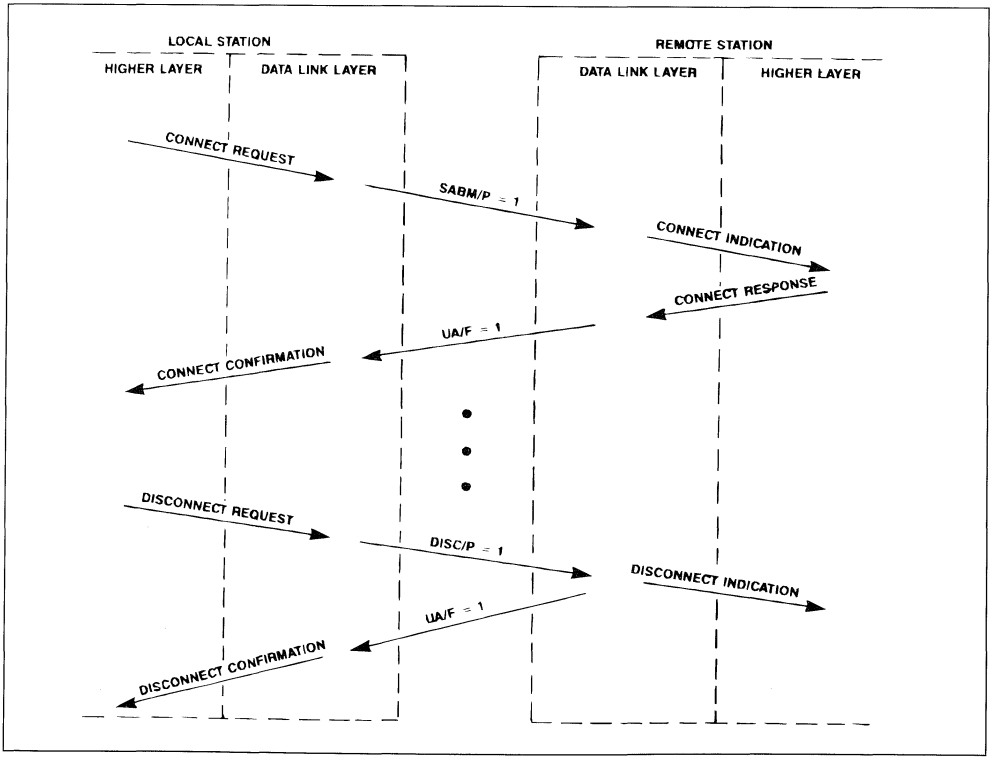
All link oriented services are provided through the exchange of Data Link Service Primitives. These primitives provide services to the HOST. Each primitive falls into one of the following categories :

1. Link Establishment (Connection)
2. Link Resetting
3. Link Disconnection
4. Data Transfer

A primitive is also one of the following types :

1. Request
2. Response
3. Indication
4. Confirmation

Figure 7 : Examples of Confirmed Data Link Services.



Requests and Responses are issued by the HOST and Indications and Confirmations are issued by the MK5025.

A Request will be issued by the HOST when a service is required. An Indication will be issued by the MK5025 when the remote system is attempting to change the data link status. A Response is issued by the HOST when receiving an indication for a confirmed service. A confirmation is issued by the MK5025 when the remote system has responded to a previously requested service.

In the MK5025, primitives are exchanged two ways : through the CSR1 and through the OWN bits in the descriptor rings. Connection, disconnection, and link reset primitives are exchanged through CSR1. Data transfer primitives are handled transparently by the OWN bit handshaking in the Descriptor Rings.

Nine additional primitives have been included in the MK5025 to handle services not mentioned in the ISO Data Link Service definition. These primitives include :

STOP - Disables the MK5025 from link operation. MK5025 transmits 1's.
INIT - Instructs the MK5025 to read the initialization block.
START - Enables the MK5025 for link operation. MK5025 starts sending flags.
TRANS - Enables the MK5025 for transparent operation. MK5025 starts sending flags.
STAT - Instructs the MK5025 to write chip status in the status buffer.
STEST - Instructs the MK5025 to perform an internal self test.
ERROR - Indicates the occurence of a link error requiring higher level action.
XID - Confirmed exchange of identification (optional).
TEST - Provides a full remote loopback test facility (optional).

For examples of the use of primitives, see the section on detailed programming procedures below.

Detailed Programming Procedures

Initialization. The following procedures should be followed to initialize the MK5025 :

1. Setup bus control information in CSR4.
2. Setup Initialization Block and Descriptor Rings and load the address of the initialization block in CSR's 2 and 3.
3. Issue the INIT primitive through CSR1 instructing the MK5025 to read the initialization block information.
4. Wait for INIT Confirmation primitive from the MK5025.
5. Issue the START Primitive through CSR1 to enable the MK5025 for link operation.
6. Enable interrupts in CSR0 if desired.

Active Link Setup. The following procedures should be followed to actively establish a link :

1. Issue the Connect Request primitive through CSR1. The MK5025 will attempt to establish a logical link.
2. Wait for a Connect Confirm primitive from the MK5025.
3. If a Connect Confirm primitive is received, a link has been established.
4. If a Disconnect Indication primitive is received, the MK5025 has been unable to establish a link. The reason will be in the PPARM field of CSR1.

Passive Link Setup. The following procedures should be followed to passively establish a link :

1. Issue a Disconnect Request primitive. A DM frame with F bit clear will be sent to the remote station requesting link setup. This step is optional.
2. Wait for a Connect Indication primitive from the MK5025.
3. If a Connect Indication primitive is received, issue a Connect Response primitive to indicate willingness to establish the link. The link is now established.
4. If no Connect Indication primitive is received, the remote site is not trying to actively setup a link.

Refusing Link Setup. The following procedure should be followed when refusing link establishment :

1. A Connect Indication will be received indicating a request by the remote station to establish a link.
2. Issue a Disconnect Request to refuse the link establishment request.

Sending Data. The following procedure should be followed to send a data frame :

1. Wait for OWNA bit of current transmit descriptor to be cleared, if not already.
2. Fill buffer associated with current transmit descriptor with data to be sent, or set descriptor buffer address to any already filled buffer.
3. Repeat steps 1 and 2 for next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.
5. Go on to next descriptor, these OWNA bits will be cleared when the data has been successfully sent and acknowledged. In Transparent Mode, OWNA bits are cleared immediately after frame transmission.

Receiving Data. The following procedure should be followed when receiving a data frame :

1. Make sure that the OWNA bit of the current receive descriptor is clear.
2. Read data out of buffer associated with current receive descriptor.
3. Set the OWNA bit of current descriptor.
4. If ELF bit of current descriptor is clear, go on to next descriptor and repeat above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

Link Disconnection. The following procedure should be followed to disconnect an established link :

1. Issue the Disconnect Request primitive to the MK5025. The MK5025 will disconnect the link.
2. A Disconnect Confirmation will be issued after successful disconnection.

Link Reset. The following procedure should be followed to reset an established link :

1. Issue a Reset Request primitive to the MK5025.
2. Wait for a Reset Confirm primitive from the MK5025.
3. If a Reset Confirm primitive is received, the link has been reset.
4. If a Disconnect Indication is received, the MK5025 was unable to reset and has disconnected. The reason for failure is in the PPARM field of CSR1. Link connection procedures must now be performed to re-establish the link.

Receiving Link Reset. The following procedure should be followed when receiving a request for link reset :

1. A Reset Indication will be received from the MK5025 indicating the remote station has requested a link resetting.
2. If able to reset, issue a reset response to indicate willingness to reset the link.
3. If unable to reset, issue a Disconnect Request to disconnect the link.

Receiving FRMR Frame. The following procedure should be followed when receiving a FRMR :

1. An Error Indication will be received from MK5025 indicating an error condition. PPARM will indicate a FRMR frame has been received. The I-field of the FRMR has been placed in the next Receive Descriptor.
2. If able to reset, issue a Reset Request to MK5025 and wait for either a Reset Indication or a Disconnect Indication as described above for Link Reset.
3. If unable to reset, issue a Disconnect Request to disconnect the current link. Link setup procedures should now be performed to re-establish a link.

Exchanging Identification. The following procedure should be followed to exchange identification with the remote :

1. XIDE in CSR3 must be set prior to any identification exchange.
2. Place identification information in the XID/TEST Transmit Buffer.
3. Issue an XID Request primitive.
4. If an XID Confirm primitive is received, the identication exchange has been performed and the remote response is located in the XID/TEST receive buffer.
5. If a Disconnect Indication is received, the identification exchange was unsuccessful.

Receiving an Identification Request. The following procedure should be performed when receiving a request for identification :

1. An XID Indication primitive will be received from the MK5025 to indicate the request for identification. The remote identification information will be located in the XID/TEST receive buffer.
2. To respond, place identification information in the XID/TEST send buffer and issue an XID Response primitive.
3. To refuse, issue a Disconnect Request primitive.

Note : *An XID Indication will only be issued if the XIDE bit in CSR3 has been set. Otherwise, all identification requests will automatically be refused and XID frames will not be recognized.*

Disabling the MK5025. The following procedure should be followed to disable the MK5025 :

1. Issue the STOP primitive. This will disable the MK5025 from receiving or transmitting. The TD pin will be held high while the MK5025 is in stopped mode. The STOP bit in CSR0 will be set and interrupts disabled. If a link is currently established, data may be lost.

Re-enabling the MK5025. The same procedure should be followed for re-enabling the MK5025 as was used to initialize upon power-up. If the Initialization Block and the hardware configuration have not changed then steps 1 and 2 may be omitted.

MK5025 Internal Self Test. The MK5025 contains an easy to use internal built-in self test designed to test, with a high fault coverage, all of the major blocks of the device except for the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute internal self test :

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK5025.
5. After the PAV bit is set, read CSR1. The success or failure of the test is indicated in the PPRIM and PPARM fields as follows :

PPARM	PPRIM	RESULT
0	0	Passed self test
1	1	Failed the reset test of the self test
1	2	Failed self test in the micro controller RAM
1	3	Failed self test in the ALU
1	4	Failed self test in the timers
1	5	Failed self test in the transmitter and/or receiver
1	6	Failed self test in the CSRs and/or bus master
Otherwise		failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHz), the MK5025 is unable to respond to the Self Test Request and will not complete it successfully.

If the self test passes, then it may be immediately re-executed by clearing the PAV bit in CSR1 and then proceding from step 3, otherwise re-execution should proceed from step 1.

MK5025 Software Identification. The MK502X family of devices provide a means of identifing the device type by using the following procedure.

After completing steps 1 and 2 of above listed procedure for Self Test, issue the Self Test Request primitive (UPRIM = 5) with UPARM = 3. The chip will then return a PPRIM of 5 (7 for the MK5027, 9 for the MK5029, etc.) to identify the device type.

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	Voltage on any Pin Relative to GND	− 0.5 to V_{CC} + 0.5	V
T_A	Ambient Operating Temperature Under Bias	− 25 to + 100	°C
T_{stg}	Ambient Storage Temperature	− 65 to + 150	°C
P_D	Total Device Power Dissipation	0.5	W

Note : Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified)

Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IL}		− 0.5		+ 0.8	V
V_{IH}		+ 2.0		V_{CC}+0.5	V
V_{OL}	@ I_{OL} = 3.2mA			+ 0.5	V
V_{OH}	@ I_{OH} = − 0.4mA	+ 2.4			V
I_{IL}	@ V_{in} = 0.4 to V_{CC}			± 10	µA
I_{CC}	T_{SCT} = 100ns		50		mA

CAPACITANCE (Frequency = 1MHz)

Symbol	Conditions	Min.	Max.	Unit
C_{IN}			10	pF
C_{OUT}			10	pF
C_{IO}			20	pF

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified).

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
1	SYSCLK	T_{SCT}	SYSCLK period		100		2000
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK	T_{SCR}	Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	$\overline{TCLK}$	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$		0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	C_L = 50pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$	C_L = 50pF	5		

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified)

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ Period		140		
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ High Time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ Low Time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise Time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall Time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD Data Rise Time		0		8
19	RD	T_{RDF}	RD Data Fall Time		0		8
20	RD	T_{RDH}	RD Hold Time after Rising Edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup Time Prior to Rising Edge of $\overline{RCLK}$		30		
22	A/ADL	T_{DOFF}	Bus Master Driver Disable after Rising Edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master Driver Enable after Falling Edge of $\overline{HLDA}$	T_{SCT} = 100nS	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to Falling Edge of $\overline{HLDA}$ from Falling Edge of $\overline{HOLD}$ (bus master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ Pulse Width		30		
26	A/DAL	T_{CYCLE}	Read/write, Address/data Cycle Time	T_{SCT} = 100nS	600		
27	A	T_{XAS}	Address Setup Time to Falling Edge of ALE		100		
28	A	T_{XAH}	Address Hold Time after the Rising Edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address Setup Time to the Falling Edge of ALE		75		
30	DAL	T_{AH}	Address Hold Time after the Falling Edge of ALE		20		
31	DAL	T_{RDAS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus maaster read)		55		
32	DAL	T_{RDAH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0		
33	DAL	T_{DDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master write)		0		
34	DAL	T_{WDS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus master write)		250		
35	DAL	TWDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus mater write)		35		
36	DAL	TSRDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave read)	T_{SCT} = 100nS	0		35
37	DAL	TSWDH	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave write)		0		
38	DAL	TSWDS	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave write)		0		
39	ALE	TALEW	ALE width high		110		

AC TIMING SPECIFICATIONS (T_A = 0°C to 70°C, V_{CC} = + 5V ± 5%, unless otherwise specified).

N°.	Signal	Symbol	Parameter	Test Conditions	Min. ns	Typ. ns	Max. ns
40	$\overline{ALE}$	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	DAS width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD} = 300nS T_{SCT} = 100nS	120		200
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of $\overline{ALE}$ (Bus master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus master read)		35		
51	$\overline{DALO}$	T_{WDIS}	Delay from rising edge of $\overline{DAS}$ to the rising edge of DALO (bus master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
54	ADR	T_{SAH}	$\overline{ADR}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle (600nS)	T_{SCT} = 100nS			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)	T_{SCT} = 100nS	0		35
60	READ	T_{SRH}	$\overline{READ}$ hold time after the rising edge of $\overline{DAS}$ (bus slave)		0		
61	$\overline{READ}$	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (bus slave read)	T_{SCT} = 100nS		200	

Figure 8 : Output Load Diagram.

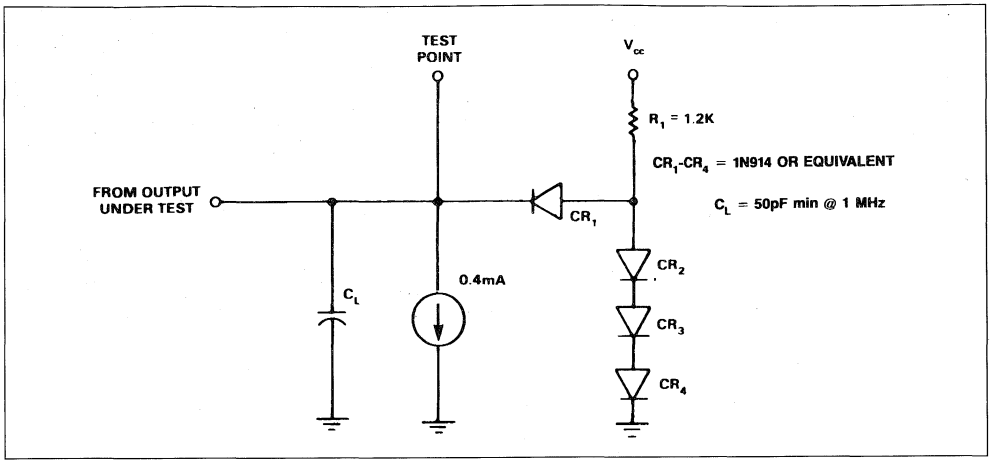
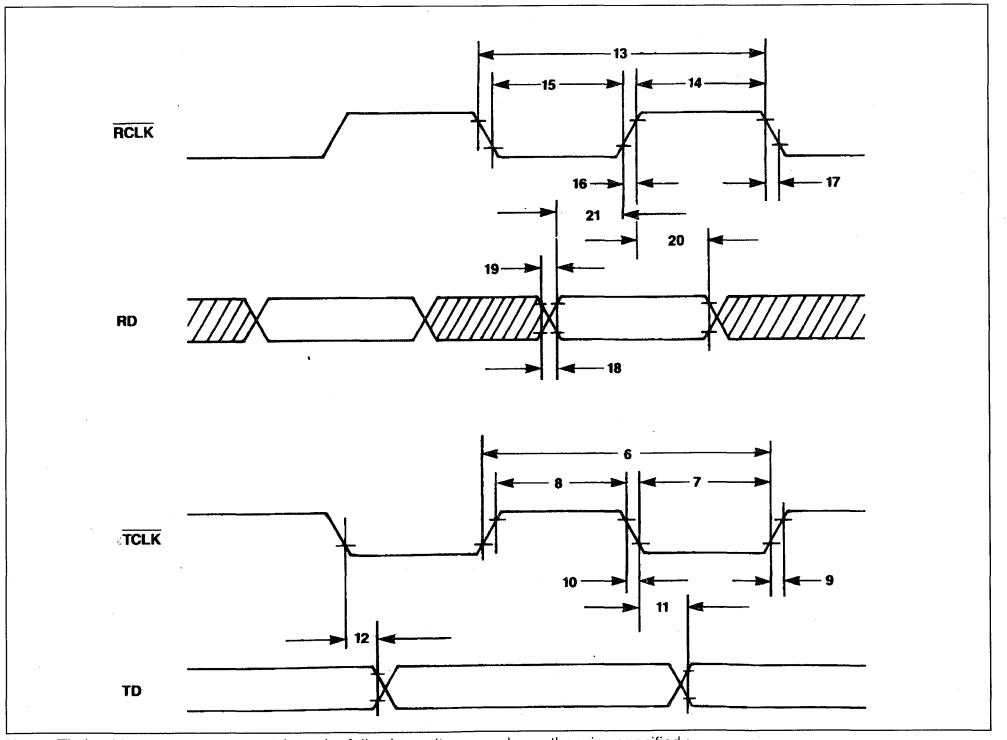


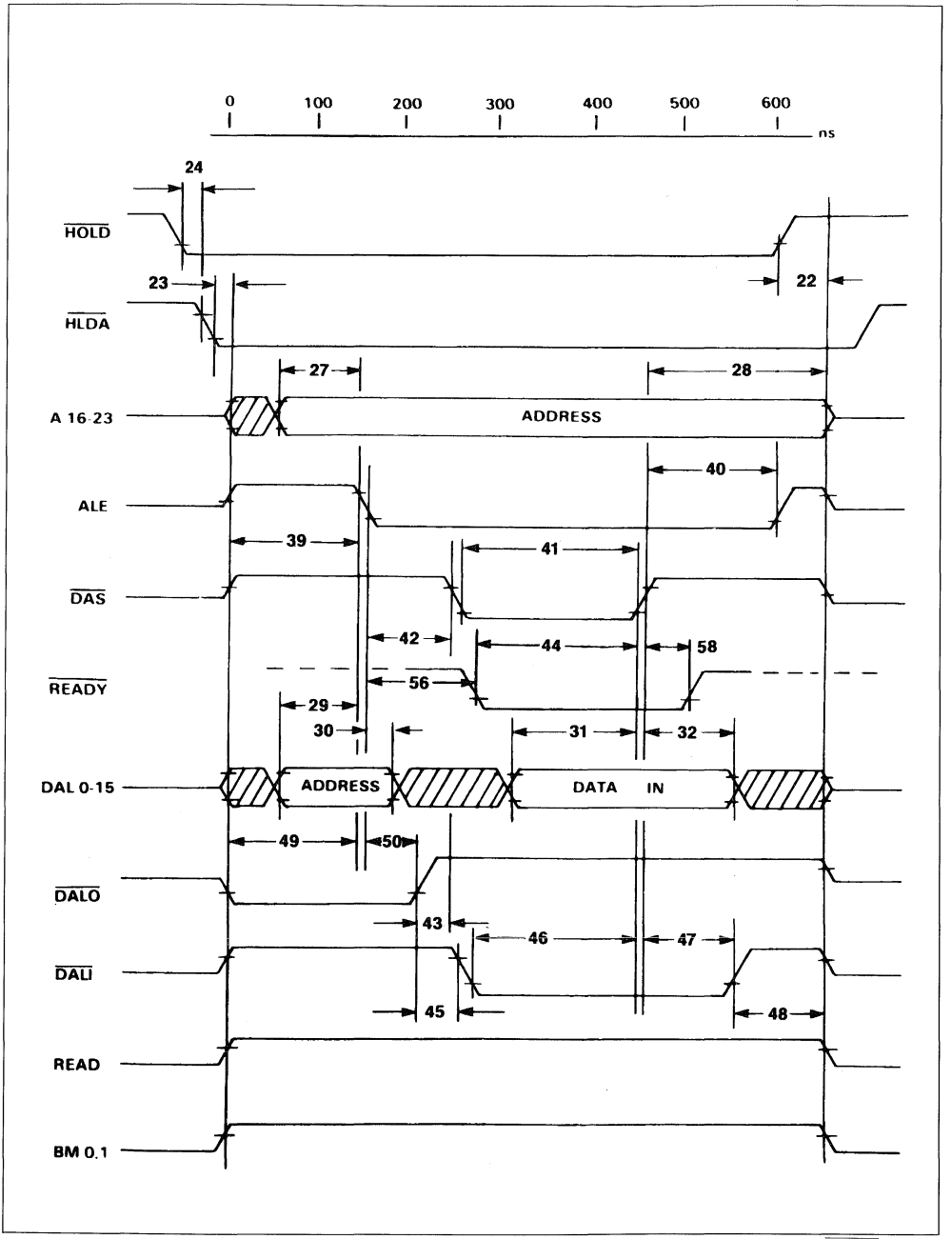
Figure 9 : Serial Link Timing Diagram.



Note : Timing Measurements are made at the following voltages, unless otherwise specified :

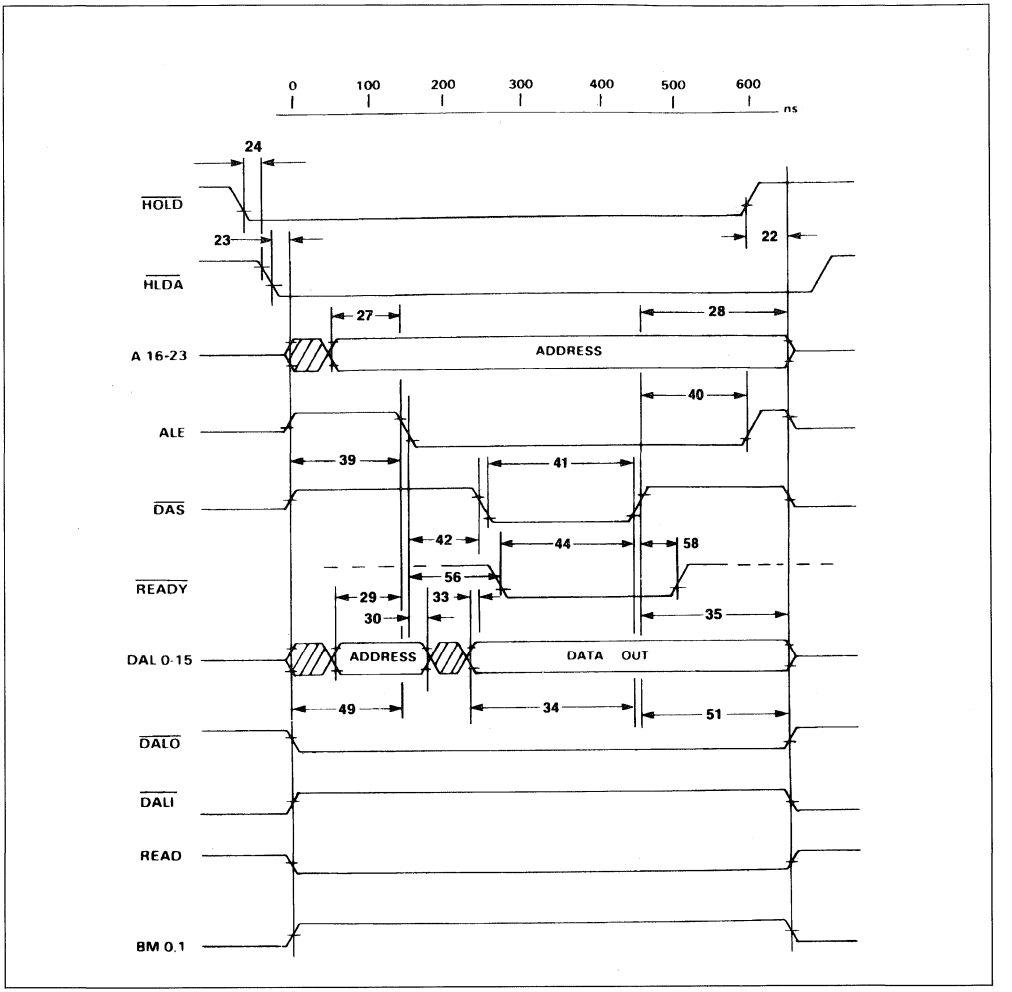
	"1"	"0"
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	90% V_{OH}	10% V_{OL}

Figure 10 : Bus Master Timing Diagram (Read).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 11 : Bus Master Timing Diagram (Write).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

Figure 12: MK5025 Bus Slave Timing Diagram (Read).

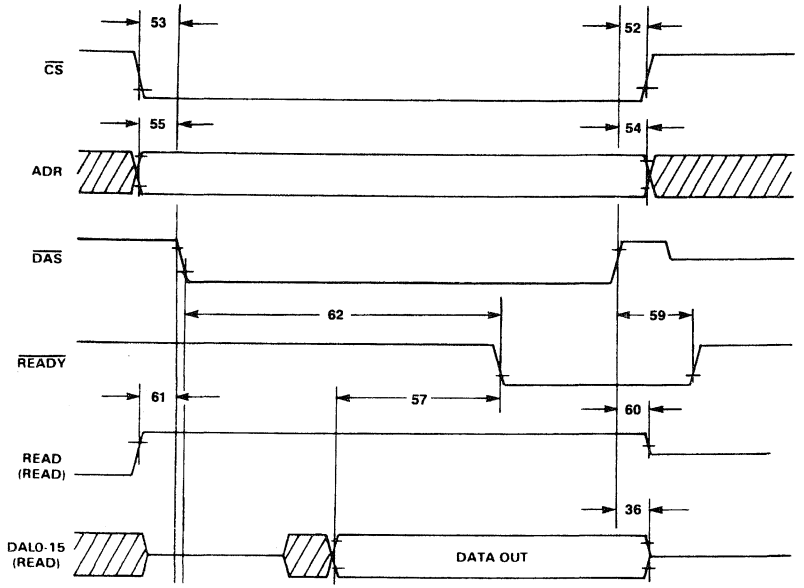
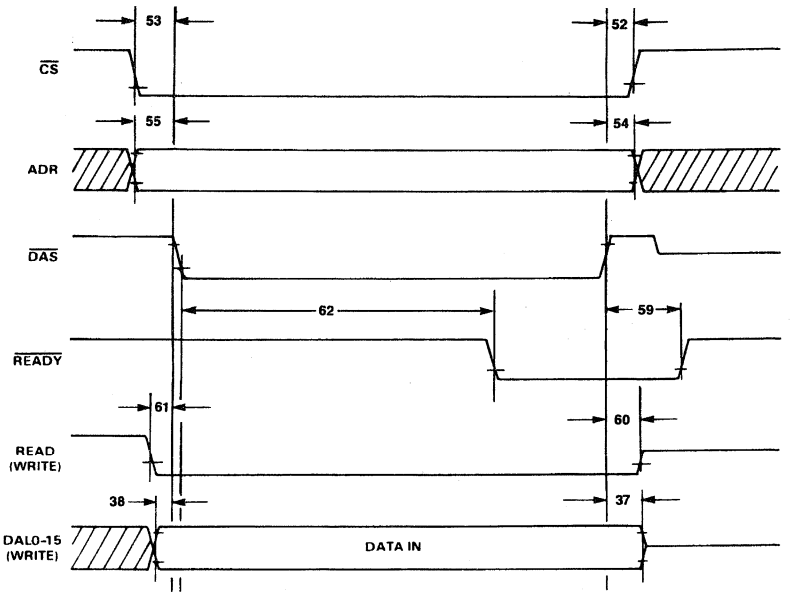


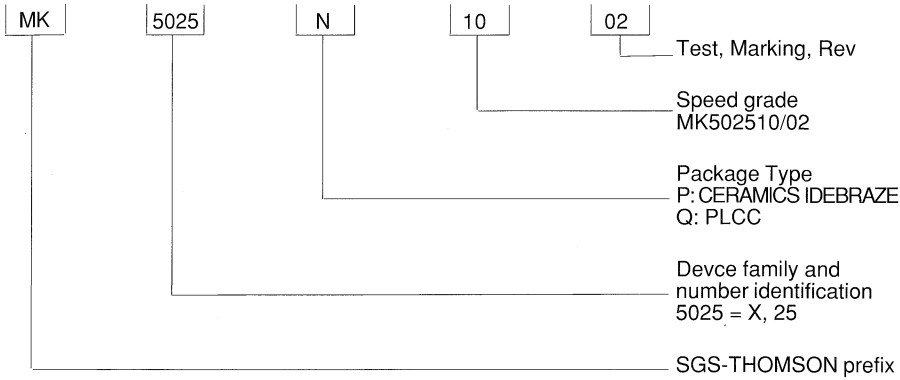
Figure 13: MK5025 Bus Slave Timing Diagram (Write).



ORDER CODES

Part Number	Description I/O	Data Rate	Clock Frequency	Temperature Range	Package Type
MK5025P-10/02	X, 25	7MB/s	10MHz	0°C to 70°C	CDIP48 600-MIL
MK5025Q-10/02		7MB/s	10MHz	0°C to 70°C	PLCC52

Note: CDIP = Ceramic Multilayer DIP, PLCC = Plastic leaded Chip carrier, PDIP = Plastic DIP.



MK5021Q10/0 Serial COM Controller, Frame Relay
MK5027P10/0 CCS#7
MK5027Q10/0 CCS#7

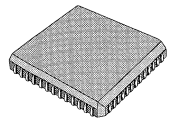
SGS-THOMSON MICROELECTRONICS

MK50H25

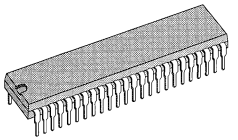
HIGH SPEED X.25 LINK LEVEL CONTROLLER

PRODUCT PREVIEW

- Fully compatible with both 8 or 16 bit systems.
- System clock rate up to 33 MHz.
- Data rate up to 20 Mbps continuous or up to 50 Mbps bursted
- Separate 64-byte Transmit and Receive FIFO.
- Complete Level 2 implementation compatible with X.25 LAPB, ISDN LAPD, X.32, and X.75 Protocols. Handles all error recovery, sequencing, and S and U frame control.
- Available in 52 pin PLCC or 48 pin DIP packages.
- Pin-for-pin and architecturally compatible with MK5025 (X.25/LAPD), MK5027 (CCS#7) and MK5029(SDLC).
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes
  - Data buffer chaining for Transmit & Receive
- On chip DMA with programmable burst length.
- Programmable Transmit FIFO hold-off watermark.
- Handles all HDLC frame formatting:
  - Zero bit insertion and deletion
  - FCS (CRC) generation and detection
  - Frame delimiting with flags
- Programmable Single or Extended Address and Control fields.
- Five programmable timer/counters: T1, T3, TP, N1, N2
- Programmable minimum frame spacing on transmission (number of flags between frames).
  - Programmable from 1 to 62 flags between frames - Selectable FCS (CRC) of 16 or 32 bits, and passing of entire FCS to buffer.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Extensive Self Test.
  - Part No. Identification & Revision Identification through software interrogation
- CMOS design with all inputs and outputs TTL compatible
- Programmable for full or half duplex operation
- Programmable Watchdog Timers for RCLK and TCLK (to detect absence of data clocks).

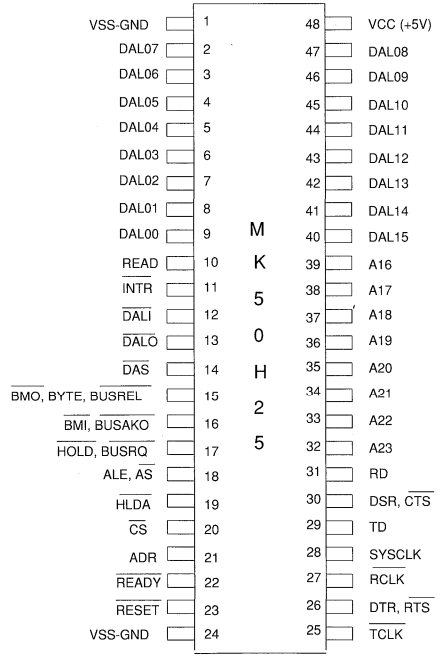


PLCC52



DIP48

DIP48 PIN CONNECTION (Top view)



This is advanced information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

SGS-THOMSON MICROELECTRONICS

MK5027

SS7 SIGNALLING LINK CONTROLLER

- CMOS
- FULLY COMPATIBLE WITH BOTH 8 OR 16 BIT SYSTEMS
- SYSTEM CLOCK RATE TO 10MHz
- DATA RATE UP TO 2.5Mbps FOR SS7 PROTOCOL PROCESSING , 7Mbps FOR TRANSPARENT HDLC MODE
- COMPLETE LEVEL 2 IMPLEMENTATION
- COMPATIBLE WITH 1988 CCITT, AT&T, ANSI, AND BELLCORE SIGNALLING SYSTEM NUMBER 7 LINK LEVEL PROTOCOLS
- 52 PIN PLCC AND 48-PIN DIP PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON X.25 CHIP (MK5025) AND NEARLY PIN-FOR-PIN COMPATIBLE WITH THE SGS-THOMSON VLANCE CHIP (MK5032)
- BUFFER MANAGEMENT INCLUDES :
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- ON CHIP DMA CONTROL WITH PROGRAMMABLE BURST LENGTH
- SELECTABLE BEC OR PCR RETRANSMISSION METHODS, INCLUDING FORCED RETRANSMISSION FOR PCR
- HANDLES ALL 7 SS7 TIMERS
- HANDLES ALL SS7 FRAME FORMATTING :
  - Zero bit insert and delete
  - FCS generation and detection
  - Frame delimiting with flags
- PROGRAMMABLE MINIMUM SIGNAL UNIT SPACING (number of flags between SU's)
- HANDLES ALL SEQUENCING AND LINK CONTROL.
- SELECTABLE FCS OF 16 OR 32 BITS
- TESTING FACILITIES :
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- ALL INPUTS AND OUTPUTS ARE TTL COMPATIBLE
- PROGRAMMABLE FOR FULL OR HALF DUPLEX OPERATION

DESCRIPTION

The SGS-Thomson Signalling System #7 Signalling Link Controller (MK5027) is a VLSI semiconductor device which provides a complete link control function conforming to the 1988 CCITT version of SS7. This includes frame formatting, transparency (so-called "bit-stuffing"), error recovery by two types of retransmission, error monitoring, sequence number control, link status control, and FISU generation. One of the outstanding features of the MK5027 is its buffer management which includes on-chip DMA. This feature allows users to handle multiple packets of receive and transmit data at a time. (A conventional data link control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK5027 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI-11, 8086, 8088, 8080, etc.

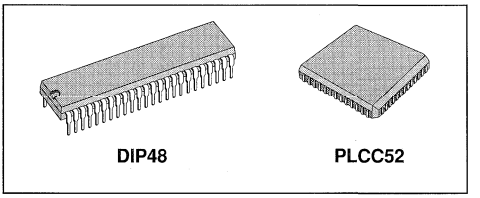


Figure 1 : Pin Connection.

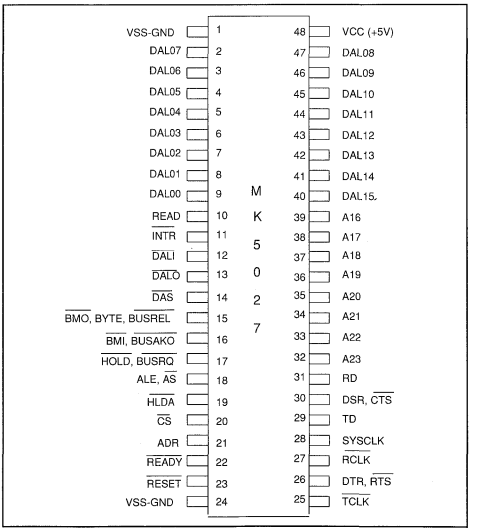


Table 1 : Pin Description.

LEGEND :

I	Input only	O	Output only
IO	Input/Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Signal Name	Pin(s)	Type	Description
DAL<15:00>	2-9 40-47	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	10	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5027 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK5027 as a Bus Slave : READ = HIGH - Data is placed on the DAL lines by the chip. READ = LOW - Data is taken off the DAL lines by the chip. MK5027 as a Bus Master : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
$\overline{\text{INTR}}$	11	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set : MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA = 1.
$\overline{\text{DALI}}$	12	O/3S	DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK5027 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.
$\overline{\text{DALO}}$	13	O/3S	DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5027 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by the MK5027 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.
$\overline{\text{DAS}}$	14	IO/3S	DATA STROBE defines the data portion of a transaction. By definition, data is stable and valid at the low to high transition of $\overline{\text{DAS}}$. This signal is driven by the MK5027 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
$\overline{\text{BMO}}$ BYTE $\overline{\text{BUSREL}}$	15	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input $\overline{\text{BUSREL}}$ and is used by the host to signal the MK5027 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear the pin 15 is an output and behaves as described below for pin 16.

Note : Pin out shown is for 48 pin dip.

Table 1 : Pin Description (continued).

Signal Name	Pin(s)	Type	Description
$\overline{BM1}$ / $\overline{BUSAKO}$	16	O/3S	Pins 15 and 16 are programmable though bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = BMO (O/3S) I/O PIN 16 = BM1 (O/3S) BYTE MASK<1:0> indicates the byte(s) on the DAL to be read or written during this bus transaction. MK5027 drives these lines only as a Bus Master. MK5027 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. $\overline{BM1}$ $\overline{BM0}$ TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE If CSR4<00> BCON = 1, I/O PIN 15 = $\overline{BYTE}$ (O/3S) I/O PIN 16 = $\overline{BUSAKO}$ (O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5027 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table. BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE $\overline{BUSAKO}$ is a bus request daisy chain output. If MK5027 is not requesting the bus and it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will be driven low. If MK5027 is requesting the bus when it receives $\overline{HLDA}$, $\overline{BUSAKO}$ will remain high. Note : All transfers are entire word unless the MK5027 is configured for 8 bit operation.

Table 1 : Pin Description (continued).

Signal Name	Pin(s)	Type	Description
$\overline{\text{HOLD}}$ $\overline{\text{BUSRQ}}$	17	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> $\overline{\text{BCON}}$ = 0, I/O PIN 17 = $\overline{\text{HOLD}}$ $\overline{\text{HOLD}}$ request is asserted by MK5027 when it requires a DMA cycle, if $\overline{\text{HLDA}}$ is inactive, regardless of the previous state of the $\overline{\text{HOLD}}$ pin. $\overline{\text{HOLD}}$ is held low for the entire ensuing bus transaction. If CSR4<00> $\overline{\text{BCON}}$ = 1, I/O PIN 17 = $\overline{\text{BUSRQ}}$ $\overline{\text{BUSRQ}}$ is asserted by MK5027 when it requires a DMA cycle if the prior state of the $\overline{\text{BUSRQ}}$ pin was high and $\overline{\text{HLDA}}$ is inactive. $\overline{\text{BUSRQ}}$ is held low for the entire ensuing bus transaction.
ALE $\overline{\text{AS}}$	18	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK5027 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = $\overline{\text{AS}}$ As $\overline{\text{AS}}$, the signal pulses low during the address portion of the bus transfer. The low to high transition of $\overline{\text{AS}}$ can be used by a slave device to strobe the address into a register. $\overline{\text{AS}}$ is effectively the inversion of ALE.
$\overline{\text{HLDA}}$	19	I	HOLD ACKNOWLEDGE is the response to $\overline{\text{HOLD}}$. When $\overline{\text{HLDA}}$ is low in response to MK5027's assertion of $\overline{\text{HOLD}}$, the MK5027 is the Bus Master. $\overline{\text{HLDA}}$ should be desasserted ONLY after $\overline{\text{HOLD}}$ has been released by the MK5027.

Table 1 : Pin Description (continued).

Signal	Pin(s)	Type	Description
$\overline{CS}$	20	I	CHIP SELECT indicates, when low, that the MK5027 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	21	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
$\overline{READY}$	22	IO/OD	When the MK5027 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a bus Slave, the MK5027 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be released after $\overline{DAS}$ or $\overline{CS}$ is negated.
$\overline{RESET}$	23	I	$\overline{RESET}$ is the Bus signal that will cause MK5027 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.
$\overline{TCLK}$	25	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may not be greater than the frequency of SYSCLK.
DTR $\overline{RTS}$	26	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5027 will assert this pin if it has data to send and throughout the transmission of a signal unit.
$\overline{RCLK}$	27	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may not be greater than the frequency of SYSCLK.
SYSCLK	28	I	SYSTEM CLOCK. System clock used for internal timing of the MK5027. SYSCLK should be a square wave, of frequency up to 10 MHz.
TD	29	O	TRANSMIT DATA. Transmit serial data output.
DSR $\overline{CTS}$	30	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input $\overline{CTS}$ or as programmable IO pin DSR. If configured as $\overline{CTS}$, the MK5027 will transmit all ones while $\overline{CTS}$ is high.
RD	31	I	RECEIVE DATA. Received serial data input.
A <23:16>	32-39	O/3S	Address bits <23:16> used in conjunction with DAL <15:00> to produce a 24 bit address. MK5027 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4 <7> BAEN bit.
VSS-GND	1, 24		Ground Pins
VCC	48		Power Supply Pin + 5.0 VDC ± 5%

Figure 2 : Possible System Configuration for the MK5027.

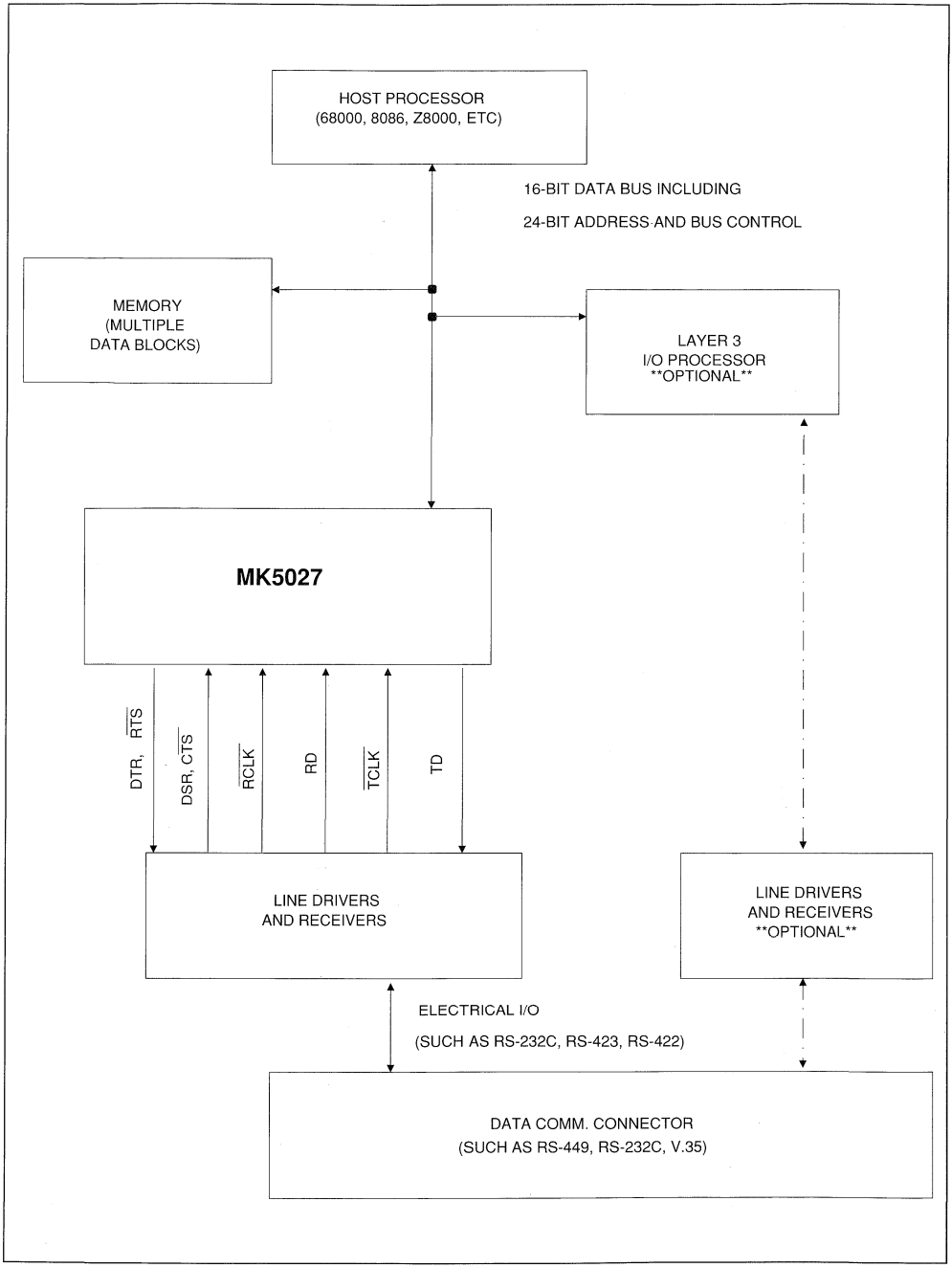
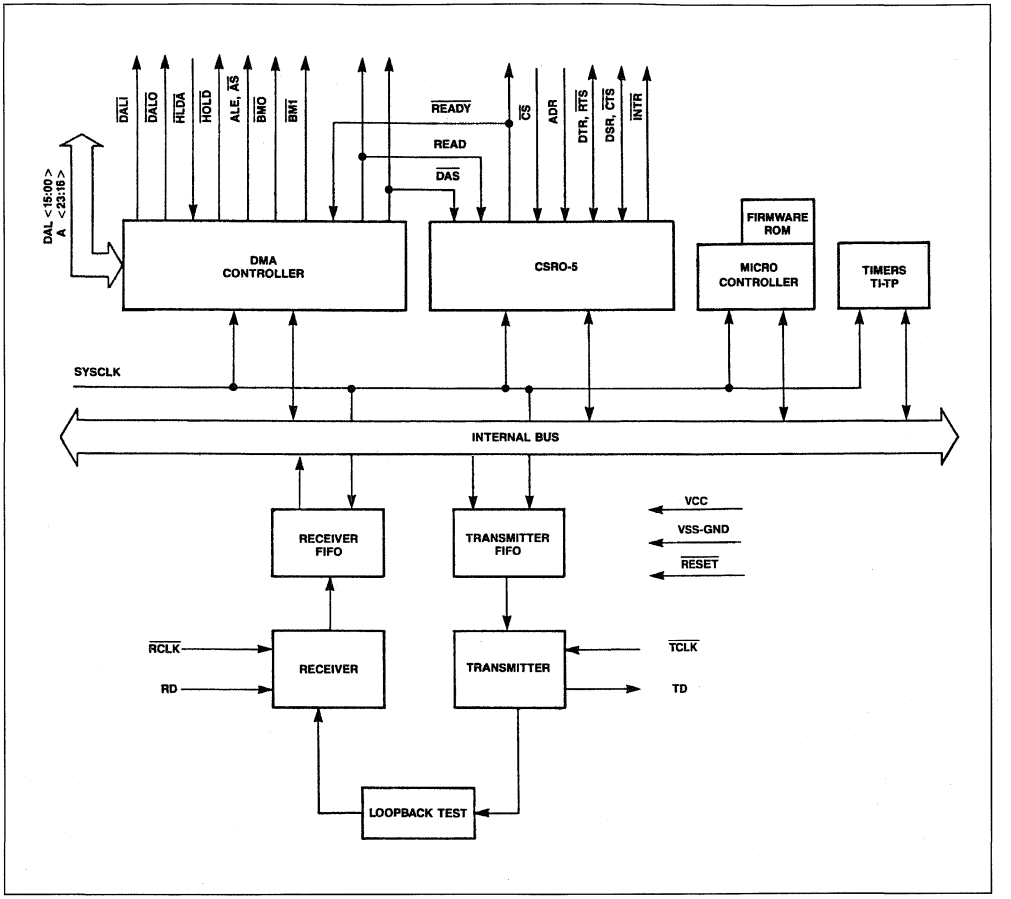


Figure 3 : MK5027 Simplified Block Diagram.



OPERATIONAL DESCRIPTION

The SGS-Thomson Signalling System #7 Signalling Link Controller (MK5027) device is a VLSI product intended for data communication applications requiring SS7 link level control. The MK5027 will perform all frame formatting, such as : frame delimiting with flags, FCS generation and detection. It will also perform all error recovery and link control. The MK5027 also includes a buffer management mechanism that allows the user to transmit and/or receive mutilple MSU's. Contained in the buffer management is an on-chip dual channel DMA : one channel for receive and one channel for transmit. The MK5027 handles error recovery and link status signalling.

The MK5027 is intended to be used with any popular 16 or 8 bit microprocessor. Possible system configuration for the MK5027 is shown in Figure 2. The MK5027 will move multiple blocks of receive and transmit data directly into and out of memory through the host's bus. An I/O acceleration processor could be used to off-load Higher Level software from the Host. The I/O acceleration processor in Figure 2 is recommended, but not required.

All signal pins on the MK5027 are TTL compatible. This has the advantage of making the MK5027 independent of the physical interface. As shown in Figure 2, line drivers and receivers are used for electrical connection to the physical layer.

SERIAL INTERFACE

The MK5027 provides two seperate serial channels; one for received data and one for transmitted data. These serial channels are completely seperate and may be run at different clock frequencies. The receiver is responsible for recognizing frame boundries, removal of inserted zeroes (for transparency), and checking the incoming FCS. Signal units with incorrect FCS values are discarded. The receiver also parallelizes the incoming data which is placed into the receive data buffers within the receive descriptor ring. The transmitter is responsible for framing and serializing the data frames placed in the transmit descriptor ring. The transmitter calculates the FCS of the outgoing data and appends it to the data. The transmitter generates flag sequences for inter-signal unit fill, at least two flags are transmitted between adjacent signal units. The FCS calculations for both directions of serial data optionally follow either the 16-bit CRC-CCITT or the 32-bit CRC-32 algorithms. FCS generation and checking can also be optionally disabled if necessary.

MICROPROCESSOR INTERFACE

The MK5027 contains a dual channel DMA on chip to handle data transfers to and from the host memory. All access to the initialization block and descriptor rings is handled in this way. The address bus is 24 bits wide and does not use any segmentation or paging methods. Data transfers can optionally be 8 and 16 bit operations, this allows easy interfacing with both 8 and 16 bit processors. DMA transfers can be up to 1, 8 or an unlimited number of words per transfer under program control. During bus slave operation the MK5027 allows access to its 6 control/status registers which are used to monitor and control the chip. These registers are used to control link procedures, configure interface options, control and monitor interrupt status, and more. Bus slave mode also allows both 8 and 16 bit accesses.

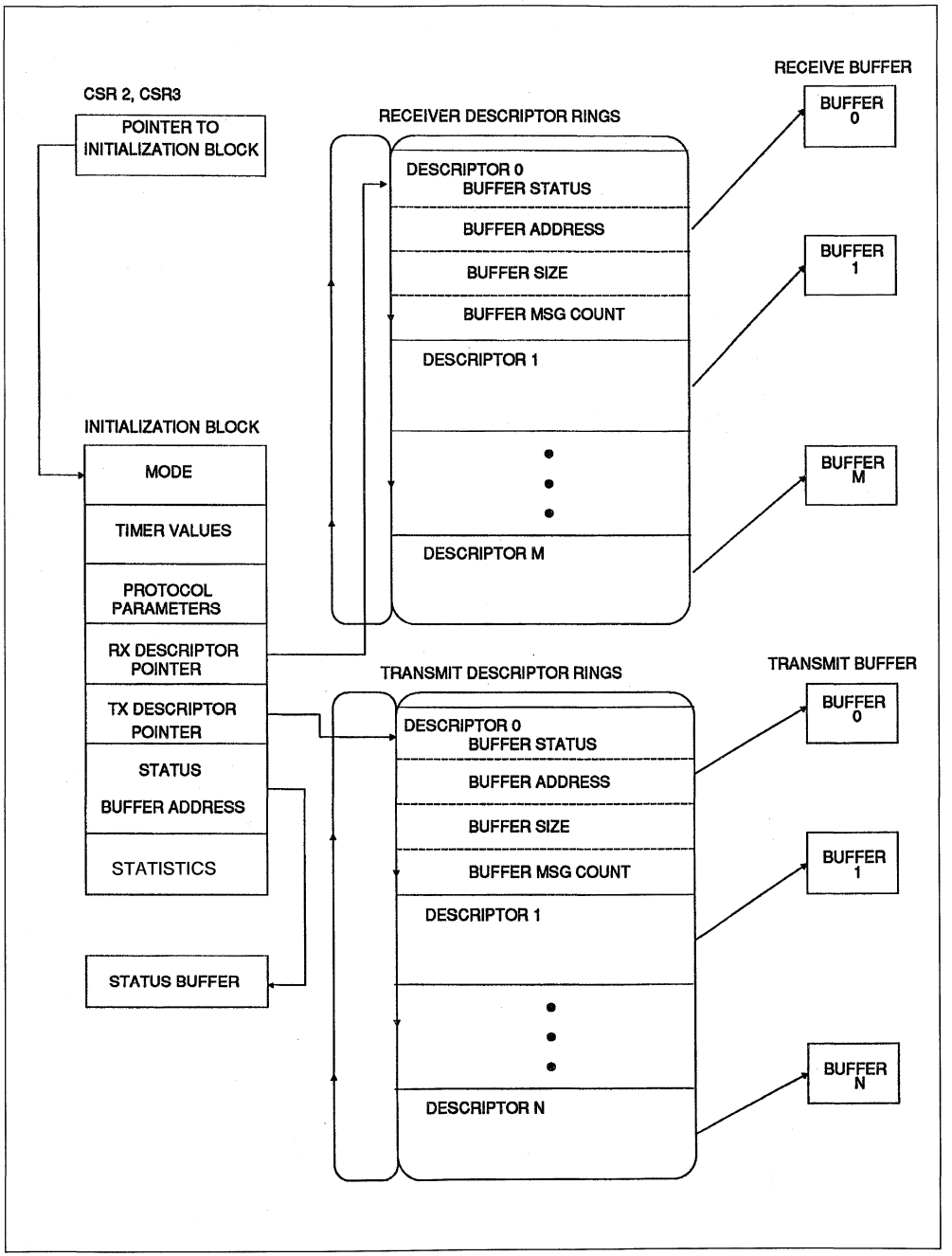
BUFFER MANAGEMENT

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are seperate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5027. The descriptor ring has a segment assigned to each buffer. Each segment holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each segment also contains two control bits called OWNA and OWNB, which denote whether the MK5027, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5027 owns the buffer, the MK5027 is allowed and commanded to transmit the buffer. When the MK5027 does not own the buffer, it will not transmit that buffer. For receive, when the MK5027 owns a buffer, it may place received data into that buffer. Conversely, when the MK5027 does not own a receive buffer, it will not place received data in that buffer.

The MK5027 buffer management mechanism will handle signal units which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers.The MK5027 tests the next segment in the descriptor ring in a "look ahead" manner.If the packet is too long for one buffer, the next buffer will be used after filling the first buffer ; that is, "chained". The MK5027 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on. The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, etc.

Figure 4 : MK5027 Buffer Management.



SIGNAL UNIT REPERTOIRE

The signal unit repertoire of the MK5027 is shown in Table 1. This set conforms to the 1988 CCITT specification for level 2 of Signalling System #7.

The definitions for the symbols for the frame types are :

Name	Definition
F	Flag Sequence
FSN	Forward Sequence Number
BSN	Backward Sequence Number
FIB	Forward Indicator Bit
BIB	Backward Indicator Bit
LI	Length Indicator
X	Programmed As Zeroes
SIO	Signalling Information Octet
SIF	Service Information Field
SF	Status Field
FCS	Frame Check Sequence

Table 1 : MK5027 Signal Unit Repertoire.

Message Signal Unit (MSU)

F	FCS	SIF	SIO	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8n,n>=2	8	2	6	1	7	1	7	8

Link Status Signal Unit (LSSU)

F	FCS	SF	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	8/16	2	6	1	7	1	7	8

Values for SF:

0 - SIO,	Out of alignment	3 - SIOS,	Out-of-service
1 - SIN,	Normal alignment	4 - SIPO,	Processor outage
2 - SIE,	Emergency	5 - SIB,	Congestion (Busy)

Fill-in Signal Unit (FISU)

F	FCS	X	LI	FIB	FSN	BIB	BSN	F
8	16/32	2	6	1	7	1	7	8

Right-most fields are transmitted first

MK5027 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Temperature under Bias ..... – 25°C to + 100°C

Storage Temperature ..... – 65°C to + 150°C

Voltage on Any Pin with Respect to Ground ..... – 0.5V to VCC + 0.5V

Power Dissipation..... 0.50W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect

DC CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = + 5V ± 5 percent unless otherwise specified.

Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{IL}		– 0.5		+ 0.8	V
V_{IH}		+ 2.0		V_{CC} +0.5	V
V_{OL}	@ I_{OL} = 3.2mA			+ 0.5	V
V_{OH}	@ I_{OH} = – 0.4mA	+ 2.4			V
I_{IL}	@ V_{IN} = 0.4 to V_{CC}			± 10	µA
I_{CC}	@ T_{SCT} = 100ns		50		mA

CAPACITANCE

F = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Capacitance on Input Pins		10	pf
C_{OUT}	Capacitance on Output Pins		10	pf
C_{IO}	Capacitance on I/O Pins		20	pf

AC TIMING SPECIFICATIONS

T_A = 0°C to 70°C, V_{CC} = + 5V ±5 percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
1	SYSCLK	T_{SCT}	SYSCLK Period		100		2000	ns
2	SYSCLK	T_{SCL}	SYSCLK Low Time		45			ns
3	SYSCLK	T_{SCH}	SYSCLK High Time		45			ns
4	SYSCLK	T_{SCR}	Rise Time of SYSCLK		0		8	ns
5	SYSCLK	T_{SCF}	Fall Time of SYSCLK		0		8	ns
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ Period		140			ns
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ Low Time		63			ns
8	TCLK	T_{TCH}	$\overline{TCLK}$ High Time		63			ns
9	$\overline{TCLK}$	T_{TCR}	Rise Time of $\overline{TCLK}$	CL = 50pF	0		8	ns
10	$\overline{TCLK}$	T_{TCF}	Fall Time of $\overline{TCLK}$		0		8	ns
11	TD	T_{TDP}	TD Data Propagation Delay after the Falling Edge of $\overline{TCLK}$	CL = 50pF			40	ns
12	TD	T_{TDH}	TD Data Hold Time after the Falling Edge of $\overline{TCLK}$		5			ns
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ Period		140			ns

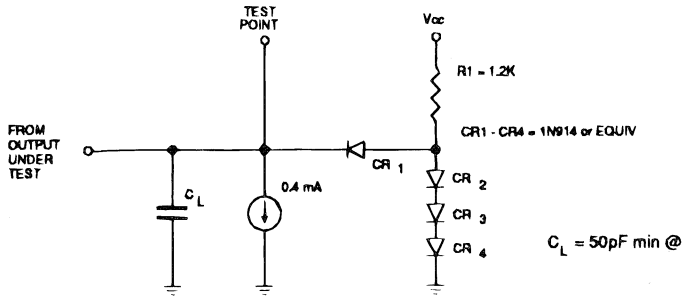
AC TIMING SPECIFICATIONS (continued)
T_A = 0°C to 70°C, V_{CC} = + 5V ±5 percent, unless otherwise specified.

N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ High Time		63			ns
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ Low Time		63			ns
16	$\overline{RCLK}$	T_{RCR}	Rise Time of $\overline{RCLK}$		0		8	ns
17	$\overline{RCLK}$	T_{RCF}	Fall Time of $\overline{RCLK}$		0		8	ns
18	RD	T_{RDR}	RD Data Rise Time		0		8	ns
19	RD	T_{RDF}	RD Data Fall Time		0		8	ns
20	RD	T_{RDH}	RD Hold Time after Rising Edge of $\overline{RCLK}$		5			ns
21	RD	T_{RDS}	RD Setup Time Prior to Rising Edge of $\overline{RCLK}$		30			ns
22	A/DAL	T_{DOFF}	Bus Master Driver Disable after Rising Edge of $\overline{HOLD}$		0		50	ns
23	A/DAL	T_{DON}	Bus Master Driver Enable after Falling Edge of $\overline{HLDA}$	TSCT=100nS	0		200	ns
24	$\overline{HLDA}$	T_{HHA}	Delay to Falling Edge of $\overline{HLDA}$ from Falling Edge of $\overline{HOLD}$ (bus master)		0			ns
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ Pulse Width		30			ns
26	A/DAL	T_{CYCLE}	Read/write, address/data Cycle Time	TSCT=100nS	600			ns
27	A	T_{XAS}	Address Setup Time to Falling Edge of ALE		100			ns
28	A	T_{XAH}	Address Hold Time after the Rising Edge of $\overline{DAS}$		50			ns
29	DAL	T_{AS}	Address Setup Time to the Falling Edge of ALE		75			ns
30	DAL	T_{AH}	Address Hold Time after the Falling Edge of ALE		20			ns
31	DAL	T_{RDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master read)		55			ns
32	DAL	T_{RDAH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0			ns
33	DAL	T_{DDAS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus master write)		0			ns
34	DAL	T_{WDS}	Data Setup Time to the Rising Edge of $\overline{DAS}$ (bus master write)		250			ns
35	DAL	$T\overline{WDH}$	Data Hold Time to the Rising Edge of $\overline{DAS}$ (bus master write)		35			ns
36	DAL	T_{SRDH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave read)	TSCT=100nS	0		35	ns
37	DAL	T_{SWDH}	Data Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave write)		0			ns
38	DAL	T_{SWDS}	Data Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave write)		0			ns
39	ALE	T_{ALEW}	ALE width High		110			ns
40	ALE	T_{DALE}	Delay from Rising Edge of $\overline{DAS}$ to the Rising Edge of ALE		70			ns
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width Low		200			ns

AC TIMING SPECIFICATIONS (continued)
T_A = 0°C to 70°C, V_{CC} = + 5V ±5 percent, unless otherwise specified.

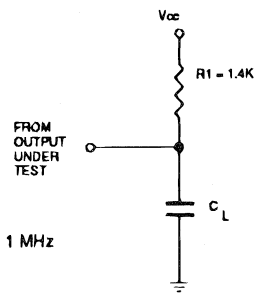
N°	Signal	Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
42	$\overline{DAS}$	T_{ADAS}	Delay from the Falling Edge of Ale to the Falling Edge of $\overline{DAS}$		80			ns
43	$\overline{DAS}$	T_{RIDF}	Delay from the Rising Edge of $\overline{DALO}$ to the Falling Edge of $\overline{DAS}$ (bus master read)		35			ns
44	$\overline{DAS}$	T_{RDYS}	Delay from the Falling Edge of $\overline{READY}$ to the Falling Edge of $\overline{DAS}$	T_{ARYD}=300ns T_{SCT}=100ns	120		200	ns
45	$\overline{DALI}$	T_{ROIF}	Delay from the Rising Edge of $\overline{DALO}$ to the Falling Edge of $\overline{DALI}$ (bus master read)		70			ns
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ Setup Time to the Rising Edge of $\overline{DAS}$ (bus master read)		150			ns
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus master read)		0			ns
48	$\overline{DALI}$	T_{RIOF}	Delay from the Rising Edge of $\overline{DALI}$ to the Falling Edge of $\overline{DALO}$ (bus master read)		70			ns
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ Setup Time to the Falling Edge of ALE (bus master read)		110			ns
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ Hold Time after the Falling Edge of ALE (bus master read)		35			ns
51	$\overline{DALO}$	T_{WDSI}	Delay from the Rising Edge of $\overline{DAS}$ to the Rising Edge of $\overline{DALO}$ (bus master write)		50			ns
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
54	$\overline{ADR}$	T_{SAH}	$\overline{ADR}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
55	$\overline{ADR}$	T_{SAS}	$\overline{ADR}$ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
56	$\overline{READY}$	T_{ARYD}	Delay from the Falling Edge of ALE to the Falling Edge of $\overline{READY}$ to Insure a Minimum Bus Cycle Time (600nS)	T_{SCT}=100nS			150	ns
57	$\overline{READY}$	T_{SRDS}	Data Setup Time to the Falling Edge of $\overline{READY}$ (bus slave read)		75			ns
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus master)		0			ns
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)	T_{SCT}=100nS	0		35	ns
60	$\overline{READY}$	T_{RSH}	$\overline{READ}$ Hold Time after the Rising Edge of $\overline{DAS}$ (bus slave)		0			ns
61	$\overline{READ}$	T_{SRS}	$\overline{READ}$ Setup Time to the Falling Edge of $\overline{DAS}$ (bus slave)		0			ns
62	$\overline{READY}$	T_{RDYD}	Delay from Falling Edge of $\overline{DAS}$ to Falling Edge of $\overline{READY}$ (bus slave)	T_{SCT}=100ns		200		ns

Figure 5A : TTL Output Load Diagram.



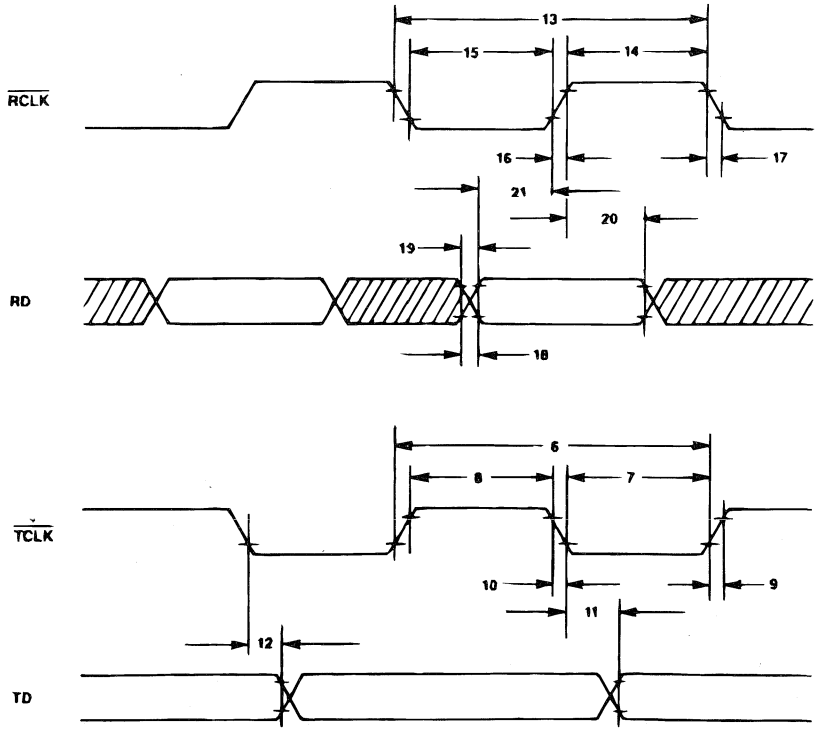
Note : This load is used on all outputs except $\overline{INTR}$, HOLD, READY.

Figure 5AB : Open Drain Output Load Diagram.



Note : This load is used on open drain outputs $\overline{INTR}$, $\overline{HOLD}$, READY.

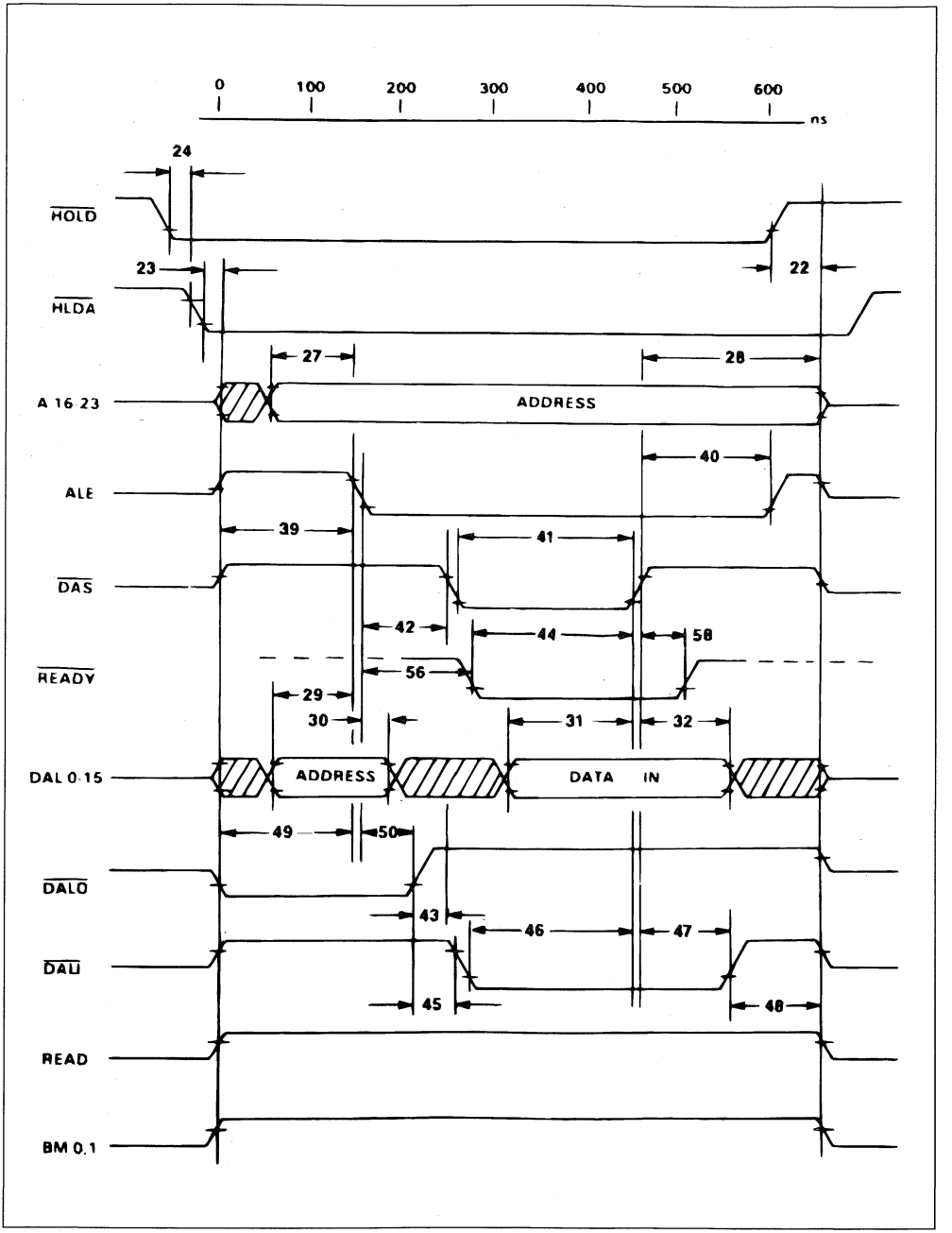
Figure 6 : MK5027 Serial Link Timing Diagram.



Timing measurements are made at the following voltages, unless otherwise specified :

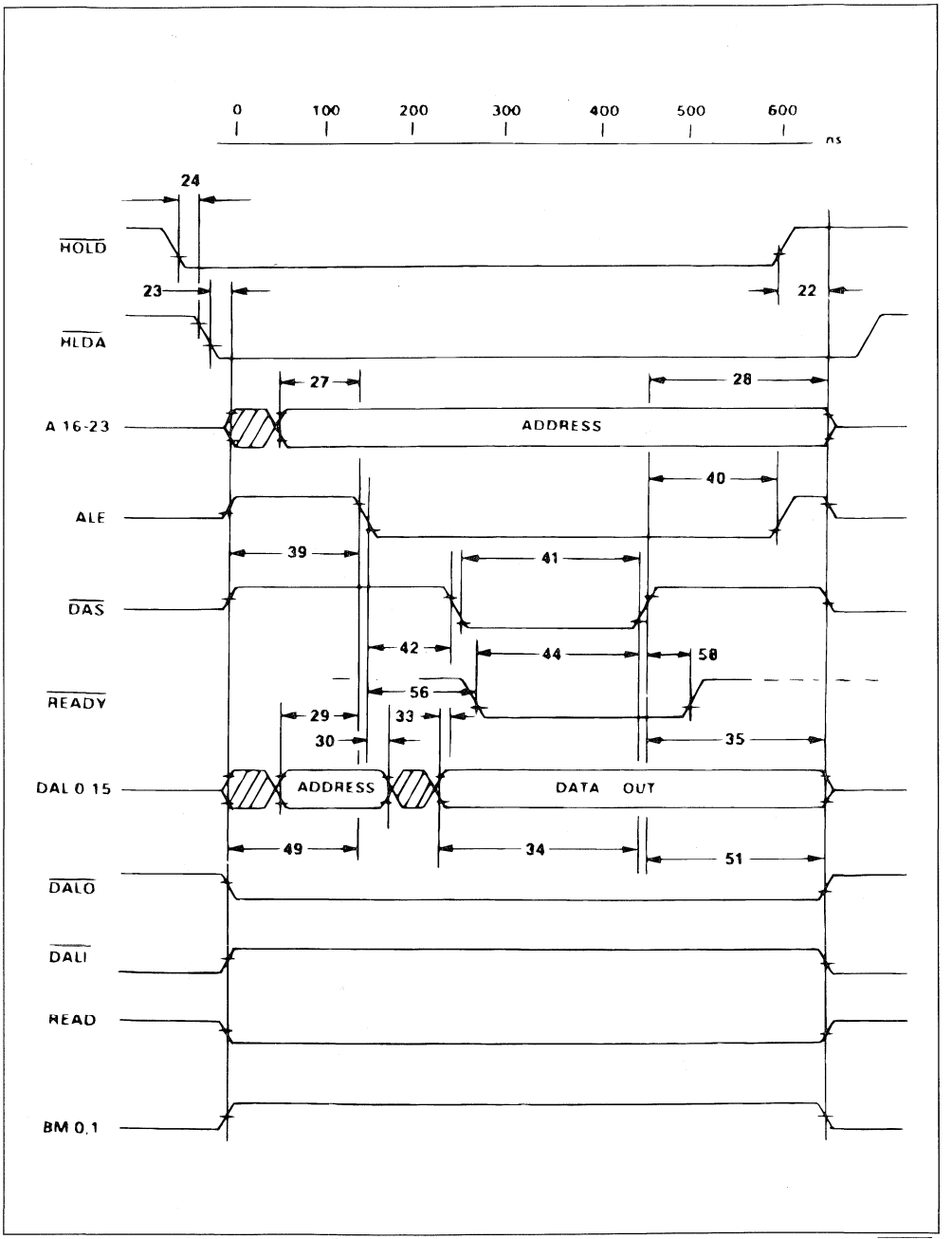
	"1"	"0"
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	10%	90%

Figure 7 : MK5027 Bus Master Timing Diagram (read).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 8 : MK5027 Bus Master Timing Diagram (write).



Note : The Bus Master cycle time will increase from a minimum of 600ns in 100ns steps until the slave device returns READY.

Figure 9: MK5027 Bus Slave Timing Diagram (read).

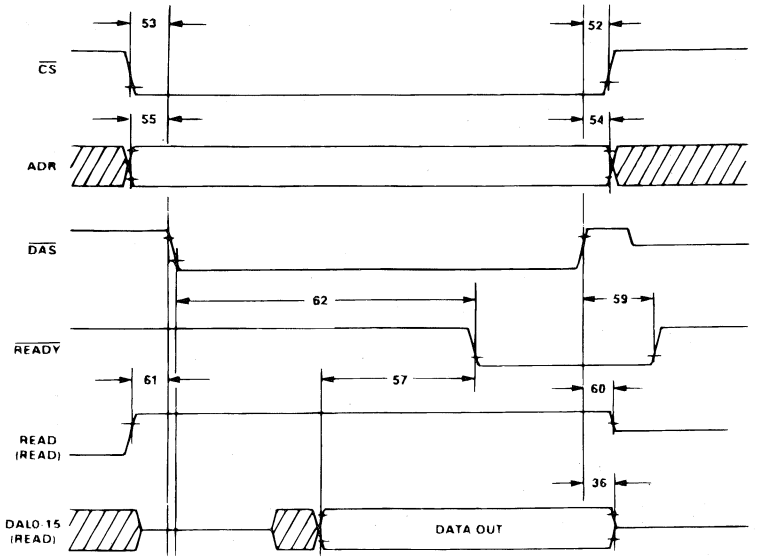
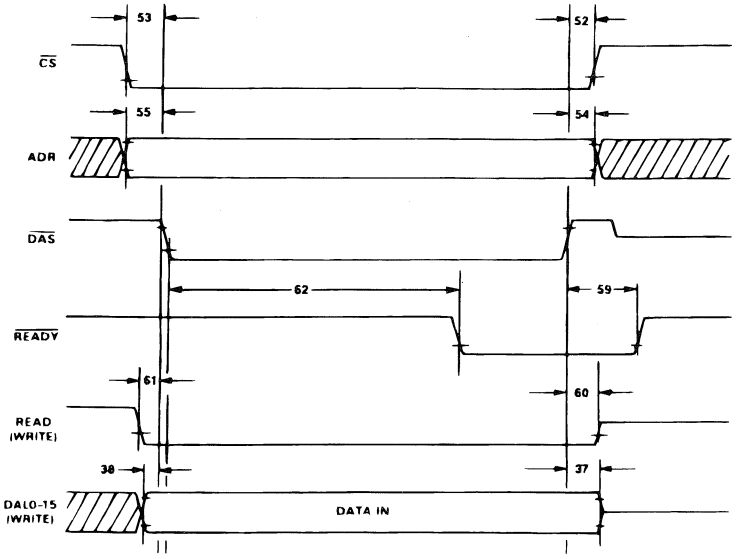


Figure 10: MK5027 Bus Slave Timing Diagram (write).



MK5029
SDLC LINK LEVEL CONTROLLER

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ELECTRICAL SPECIFICATIONS

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SECTION 1: INTRODUCTION

The SGS - Thomson MK5029 SDLC Communications Controller is a 7 Mbps CMOS device which provides link level data communications control for SDLC secondary stations. The MK5029 will perform frame formating including: frame delimiting with flags, transparency (so-called "bit-stuffing"), error recovery by retransmission, sequence number control, S (supervisory) and U (unnumbered) frame control, plus FCS (CRC) generation and detection. For added flexibility a transparent mode provides an HDLC transport mechanism without link layer support. This flexible transparent mode may be easily entered and exited without affecting the SDLC link status or the link state variables kept by the MK5029. The MK5029, in full transparent mode, can be used for implementing SDLC Master stations. In this mode no protocol processing is done and it is up to the user to take care of the upper level software.

One of the outstanding features of the MK5029 is its buffer management which includes on-chip dual channel DMA. This feature allows users to receive and transmit multiple data frames at a time. (A conventional serial communications control chip plus a separate DMA chip would handle data for only a single block at a time.) The MK5029 will move multiple blocks of receive and transmit data directly into and out of memory through the Host's bus. Moreover, the memory management capability includes the chaining of long frames. A possible system configuration for the MK5029 is shown in figure 1.

The MK5029 may be used with any of several popular 16 and 8 bit microprocessors, such as 68000, 6800, Z8000, Z80, LSI- 11, 8086, 8088, 8080, etc.

The MK5029 may be operated in either full or half duplex mode. In half duplex mode, the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins. All signal pins on the MK5029 are TTL compatible. This has the advantage of making the MK5029 independent of the physical interface. As shown in figure 1, line drivers and receivers are used for electrical connection to the physical layer.

SECTION 2: FEATURES

- CMOS
- Fully compatible with both 8 and 16 bit systems.
- System clock rate up to 10 MHz.
- Data rate up to 7 Mbps, with a 64-byte FIFO in each direction.
- Implements SDLC/HDLC (ADCCP) type frame formating.
- Available in 52 pin PLCC or 48 pin DIP packages.
- Pin compatible and architecturally the same as MK5025 (X.25/LAPD), MK5027 (CCS#7) and MK5021(SCC).
- Buffer Management includes:
  - Initialization Block
  - Separate Receive and Transmit Rings
  - Variable Descriptor Ring and Window Sizes.
- On chip DMA control with programmable burst length.
- Handles all SDLC/HDLC frame formatting:
  - Zero bit insertion and deletion
  - FCS (CRC) generation and detection
  - Frame delimiting with flags
- Programmable Address and Control fields.
- Programmable (N1) Maximum Frame Length counter.
- Handles all error recovery, sequencing, and S and U frame control.
- Programmable minimum frame spacing on transmission (number of flags between frames).
- Selectable FCS (CRC) of 16 or 32 bits.
- Testing Facilities:
  - Internal Loopback
  - Silent Loopback
  - Optional Internal Data Clock Generation
  - Self Test.
- All inputs and outputs are TTL compatible
- Programmable for full or half duplex operation

SECTION 3: OPERATIONAL DESCRIPTION

The SGS - Thomson MK5029 SDLC Communications Controller device is a VLSI product intended for high performance data communication applications requiring SDLC link level control. The MK5029 will perform all frame formatting, such as: frame delimiting with flags, FCS (CRC) generation and detection, and zero bit insertion and deletion for transparency. The MK5029 also includes a buffer management mechanism that allows the user to transmit and/or receive multiple frames. Contained in the buffer management is an on-chip dual channel DMA: one channel for receive and one channel for transmit.

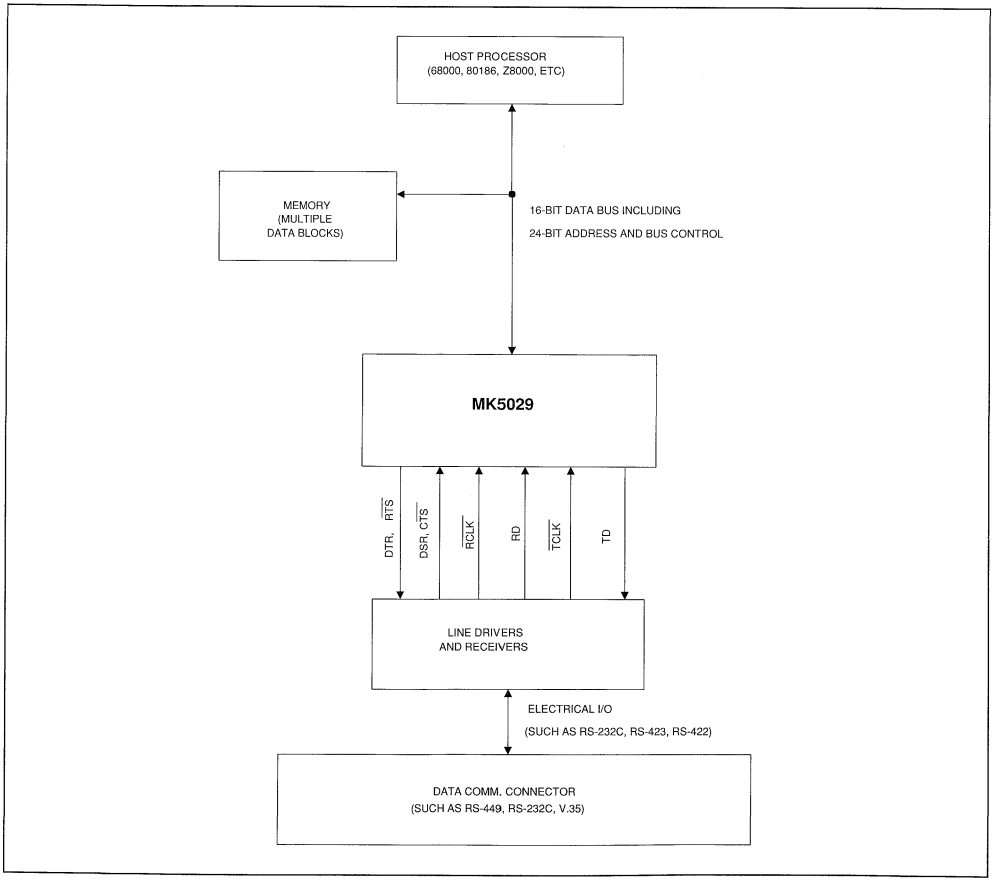
The MK5029 can be used with any popular 16 or 8 bit microprocessor. A possible system configuration for the MK5029 is shown in Figure 1. This document assumes that the processor has a byte addressable memory organization.

The MK5029 will move multiple blocks of receive and transmit data directly in and out of memory through the Host's bus. An I/O acceleration processor, could be used to off-load Network Level software from the Host.

The MK5029 may be operated in full or half duplex mode. In half duplex mode the RTS and CTS modem control pins are provided. In full duplex mode, these pins become user programmable I/O pins.

All signal pins on the MK5029 are TTL compatible. This has the advantage of making the MK5029 independent of the physical interface. As shown in Fig. 1, line drivers and receivers are used for electrical connection to the physical layer.

Figure 1: Possible System Configuration For The MK5029



3.1 Functional Blocks

Refer to the block diagram in Figure 2.

The MK5029 is primarily initialized and controlled through six 16-bit Control and Status Registers (CSR0 thru CSR5). The CSR's are accessed through two bus addressable ports, the Register Address Port (RAP), and the Register Data Port (RDP). The MK5029 may also generate an interrupt(s) to the Host. These interrupts are enabled and disabled through CSR0.

The on-chip microcontroller is used to control the movement of parallel receive and transmit data, and to handle the Address and Control field filtering.

3.1.1 Microcontroller

The microcontroller controls all of the other blocks of the MK5029. The microcontroller performs frame processing and protocol processing. All frame content processing as well as S and U frame

3.1.2 Receiver

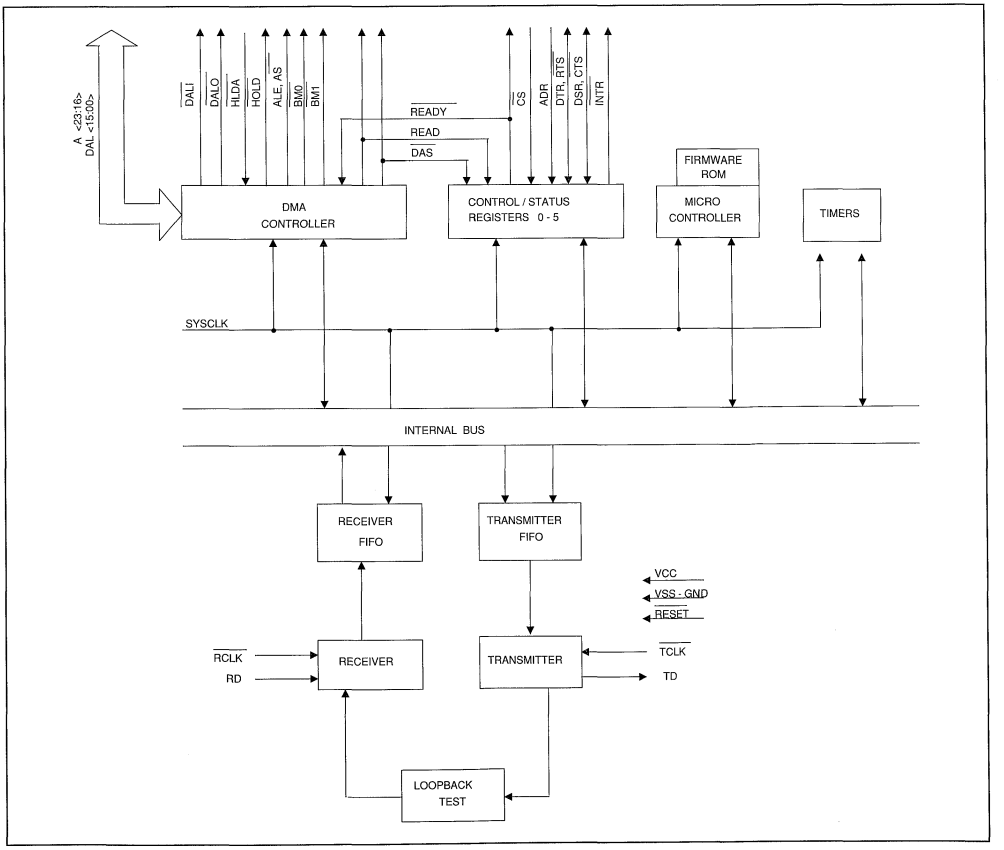
Serial receive data comes into the Receiver (Figure 2). The Receiver is responsible for:

1. Leading and trailing flag detection.
2. Deletion of zeroes inserted for transparency.
3. Detection of idle and abort sequences.
4. Detection of good and bad FCS (CRC).
5. Monitoring Receiver FIFO status.
6. Detection of Receiver Over-Run.
7. Odd byte detection.

NOTE: If frames are received that have an odd number of bytes
then the last byte of the frame is said to be an odd byte.

8. Detection of non-octet aligned frames. Such frames are treated as invalid frames.

Figure 2 : MK5029 Simplified Block Diagram



3.1.3 Transmitter

The Transmitter is responsible for:

1. Serialization of outgoing data.
2. Generating and appending the FCS (CRC).
3. Framing outgoing frame with flags.
4. Zero bit insertion for transparency.
5. Transmitter Under-Run detection.
6. Transmission of odd byte.
7. RTS/CTS control.

3.1.4 Frame Check Sequence or Cyclic Redundancy Check

The FCS (CRC) on the transmitter or receiver may be either 16 bit or 32 bit, and is user selectable. For full duplex operation, both the receiver and transmitter have individual FCS computation circuits. The characteristics of the FCS are:

Transmitted Polarity: Inverted

Transmitted Order: High Order Bit First

Pre-set Value: All 1's

Polynomial 16 bit:
$X^{16} + X^{12} + X^5 + 1$

Remainder 16 bit (if received correctly):
High order bit—>0001 1101 0000 1111

Polynomial 32 bit:
$X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$

Remainder 32 bit (if received correctly):
high order bit—>1100 0111 0000 0100
1101 1101 0111 1011

3.1.5 Receive FIFO

The Receive FIFO buffers the data received by the receiver. This performs two major functions. First, it resynchronizes the data from the receive clock to the system clock. Second, it allows the microcontroller time to finish whatever it may be doing before it has to process the received data.

The receive FIFO holds the data from the receiver without interrupting the microcontroller until it contains enough data to reach the watermark level. This watermark level can be programmed in CSR4 to occur when the FIFO contains at least 2 bytes; 18 or more bytes; 34 or more bytes; or 50 or more bytes. This programmability , along with the programmable burst length of the DMA controller, enables the user to define how often and for how long the MK5029 must use the host bus. For more information, see Control/Status Register 4.

For example, if the watermark level is set at 34 bytes and the burst length is limited to 8 word transfers at a time, the MK5029 will request control of the host bus as soon as 34 bytes are received and again after every 16 subsequent bytes.

3.1.6 Transmit FIFO

The Transmit FIFO buffers the data to be transmitted by the MK5029. This also performs two major functions. First, it resynchronizes the data from the system clock to the transmit clock. Second, it allows the microcontroller and DMA controller to burst read data from the host's memory buffers; making both the MK5029 and the host bus more efficient.

3.1.7 DMA Controller

The MK5029 has an on-chip DMA Controller circuit. This allows it to access memory without requiring host software intervention. Whenever the MK5029 requires access to the host memory it will negotiate for mastership of the bus. Upon gaining control of the bus the MK5029 will begin transferring data to or from memory. The MK5029 will perform memory transfers until either it has nothing more to transfer, it has reached its DMA burst limit (user programmable), or the BUSREL pin is driven low. In any case, it will complete all bus transfers before releasing bus mastership back to the host. If during a memory transfer, the memory does not respond within 256 SCLK cycles, the MK5029 will release ownership of the bus immediately and the MERR bit will be set in CSR0. The DMA burst limit can be programmed by the user through CSR4. In 16 bit mode the limit can be set to 1 word, 8 words, or unlimited word transfers. In 8 bit mode,it can be set to 2 bytes, 16 bytes, or unlimited byte transfers. For high speed data lines (i.e. > 1 Mbps) a burst limit of 8 words, 16 bytes or unlimited is suggested to allow maximum throughput.

The byte ordering of the DMA transfers can be programmed to account for differences in processor architectures or host programming languages. Byte ordering can be programmed separately for data and control information. Data information is defined as all contents of data buffers; control information is defined as anything else in the shared memory space (i.e. initialization block, descriptors, etc). For more information see section 4.1.2.5 on control status register 4.

3.1.8 Bus Slave Circuitry

The MK5029 contains a bank of internal control/status registers (CSR0-5) which can be accessed by the host as a peripheral. The host can read or write to these registers like any other bus slave. The contents of these registers are listed in Section 4 and bus signal timing is described in Figures 9 and 10.

3.2 Buffer Management Overview

Refer to Fig. 3.

3.2.1 Initialization Block

Chip initialization information is located in a block of memory called the Initialization Block. The Initialization Block consists of 28 contiguous words of memory starting on a word boundary. This memory is assembled by the HOST, and is accessed by the MK5029 during initialization. The Initialization Block is comprised of:

A. Mode of Operation.

B. Frame Address Values.

C. N1 Counter (Max Frame Length) and Timer Values.

D. Protocol Parameters.

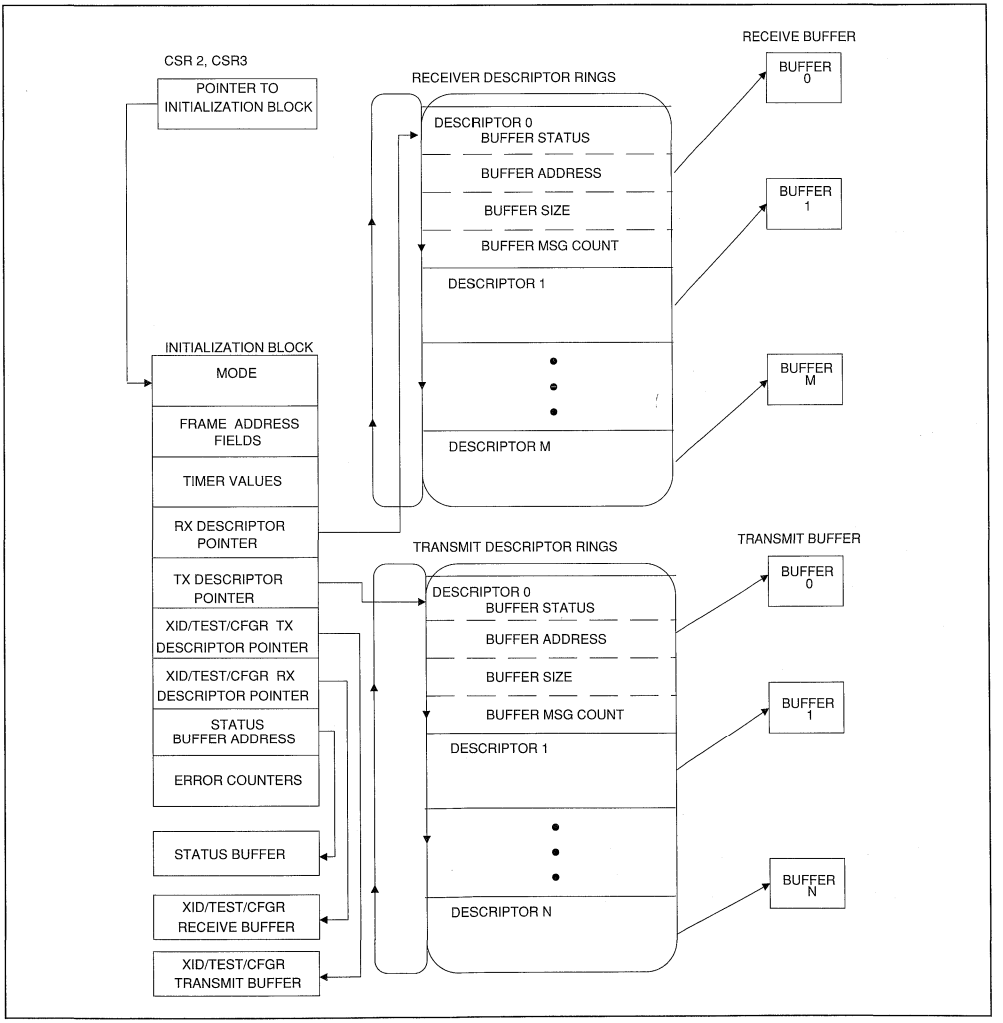
E. Location and size of Receive and Transmit Descriptor Rings.

F. Location and size of XID/TEST/CFGR Buffers.

G. Location of Status Buffer.

H. Error Counters.

Figure 3 : MK5029 Buffer Management



3.2.2 The Circular Queue

The basic organization of the buffer management is a circular queue of tasks in memory called descriptor rings. There are separate rings to describe the transmit and receive operations. Up to 128 buffers may be queued-up on a descriptor ring awaiting execution by the MK5029. The descriptor ring has a descriptor assigned to each buffer. Each descriptor holds a pointer for the starting address of the buffer, and holds a value for the length of the buffer in bytes.

Each descriptor also contains two control bits called OWNA and OWNB, which denote whether the MK5029, the HOST, or the I/O ACCELERATION PROCESSOR (if present) "owns" the buffer. For transmit, when the MK5029 owns the buffer, the MK5029 is allowed and commanded to transmit the buffer at its next poll opportunity. When the MK5029 does not own the buffer, it will not transmit that buffer. For receive, when the MK5029 owns a buffer, it may place received data into that buffer. Conversely, when the MK5029 does not own a receive buffer, it will not place received data into that buffer.

The MK5029 buffer management mechanism will handle frames which are longer than the length of an individual buffer. This is done by a chaining method which utilizes multiple buffers. The MK5029 tests the next descriptor in the descriptor ring in a "look ahead" manner. If the frame is too long for one buffer, the next buffer will be used after filling the first buffer; that is, "chained". The MK5029 will then "look ahead" to the next buffer, and chain that buffer if necessary, and so on.

The operational parameters for the buffer management are defined by the user in the initialization block. The parameters defined include the basic mode of operation, the number of entries for the transmitter and receiver descriptor rings, protocol parameters, etc. The starting address for the Initialization block, IADR, is defined in the CSR2 and CSR3 registers inside the MK5029.

3.2.3 Frame Format

The frame format supported by the MK5029 is shown below. Each frame may consist of a programmable number of leading flag patterns (01111110), an address field, a control field, an information field, an FCS (CRC) of either 16 or 32 bits, and a trailing flag pattern. The number of leading flags transmitted is programmable through the Mode Register in the Initialization Block. Received frames may have only one flag between adjacent frames.

F	A	C	INFO	FCS	F
8	8/16	8/16	8*n	16/32	8

TRANSMITTED FIRST

3.2.4 The Command/Response Repertoire

The command/response repertoire of the MK5029 is shown in Tables A and B. This set conforms to the IBM SDLC manual GA27-3093-2. The MK5029 will process the Information, Supervisory, and Unnumbered frames shown in Tables A and B, and will handle the A and C fields for all the frames mentioned below.

The definitions for the frame types are:

Name	Definition	Name	Definition
I	Information frame	SIM	Set Initialization Mode
UI	Unnumbered Information frame	RIM	Request Initialization Mode
RR	Receiver Ready	DM	Disconnect Mode
RNR	Receiver Not Ready	FRMR	Frame Reject
REJ	Reject	TEST	Link Test Frame
SNRM	Set Normal Response Mode	XID	Exchange Station Identification
DISC	Disconnect	UP	Unnumbered Poll
RD	Request Disconnect	BCN *	Beacon (Loop response)
UA	Unnumbered Acknowledge	CFGR	Configure

* BCN may be sent by the user by switching to the transparent mode.

Table A: MK5029 Command/Response Repertoire Modulo 8 Operation

Format	Command	Response	Encoding LSB							MSB
			1	2	3	4	5	6	7	8
Information Transfer	I	I	0	←	N(S)	→	P	←	N(R)	→
Supervisory	RR	RR	1	0	0	0	P/F	←	N(R)	→
	RNR	RNR	1	0	1	0	P/F	←	N(R)	→
	REJ	REJ	1	0	0	1	P/F	←	N(R)	→
Unnumbered	*UI	*UI	1	1	0	0	P/F	0	0	0
		RIM	1	1	1	0	F	0	0	0
	*SIM		1	1	1	0	P	0	0	0
	SNRM		1	1	0	0	P	0	0	1
		DM	1	1	1	1	F	0	0	0
	DISC		1	1	0	0	P	0	1	0
		UA	1	1	0	0	F	1	1	0
		FRMR	1	1	1	0	F	0	0	1
		RD	1	1	0	0	F	0	1	0
	*XID	*XID	1	1	1	1	P/F	1	0	1
	*UP		1	1	0	0	P	1	0	0
	*TEST	*TEST	1	1	0	0	P/F	1	1	1
		**BCN	1	1	1	1	F	1	1	1
	*CFGR	*CFGR	1	1	1	0	P/F	0	1	1

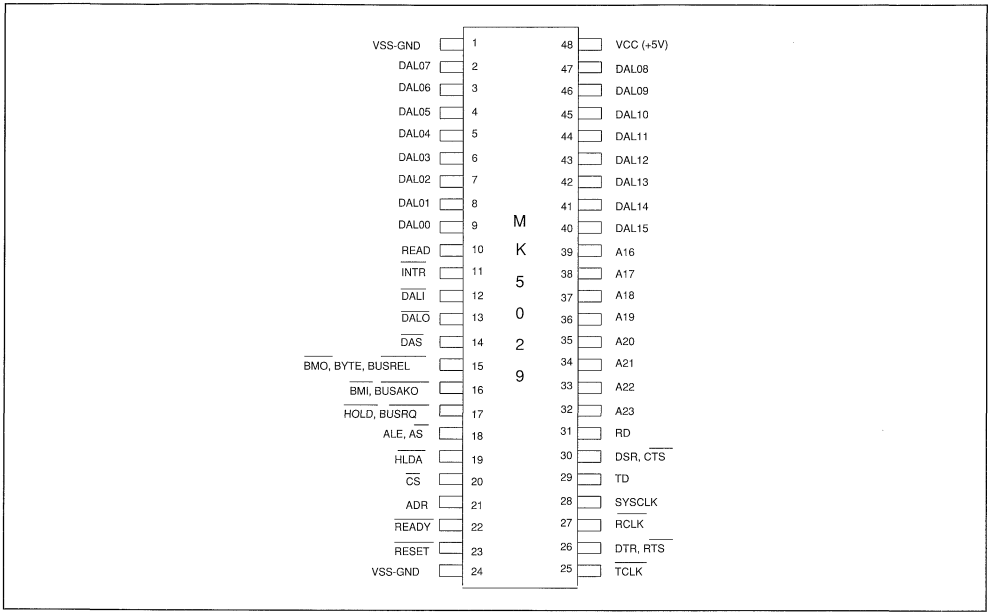
Table B: MK5029 Command/Response Repertoire Modulo 128 Operation

Format	Command	Response	Encoding									
			1	2	3	4	5	6	7	8	9	10-16
Information Transfer	I	I	0 ← N(S) →								P	N(R)
Supervisory	RR	RR	1	0	0	0	0	0	0	0	P/F	N(R)
	RNR	RNR	1	0	1	0	0	0	0	0	P/F	N(R)
	REJ	REJ	1	0	0	1	0	0	0	0	P/F	N(R)
Unnumbered	SNRME		1	1	0	0	P	0	1	1		
	All others		Same Repertoire and Encoding as for Modulo 8 Operation									

N(S) = Transmitter send sequence number
N(R) = Transmitter receive sequence number
XID and UI frames can be individually enabled through CSR2.
P/F = Poll bit when issued as a command, Final bit when issued as a response
* TEST, CFGR, SIM and UP frames can be enabled individually by setting the appropriate bits in the Protocol Parameters Register
** BCN frame can be sent by temporarily switching to the flexible Transparent Mode

3.3 PIN DESCRIPTION

DIP48



PLCC52

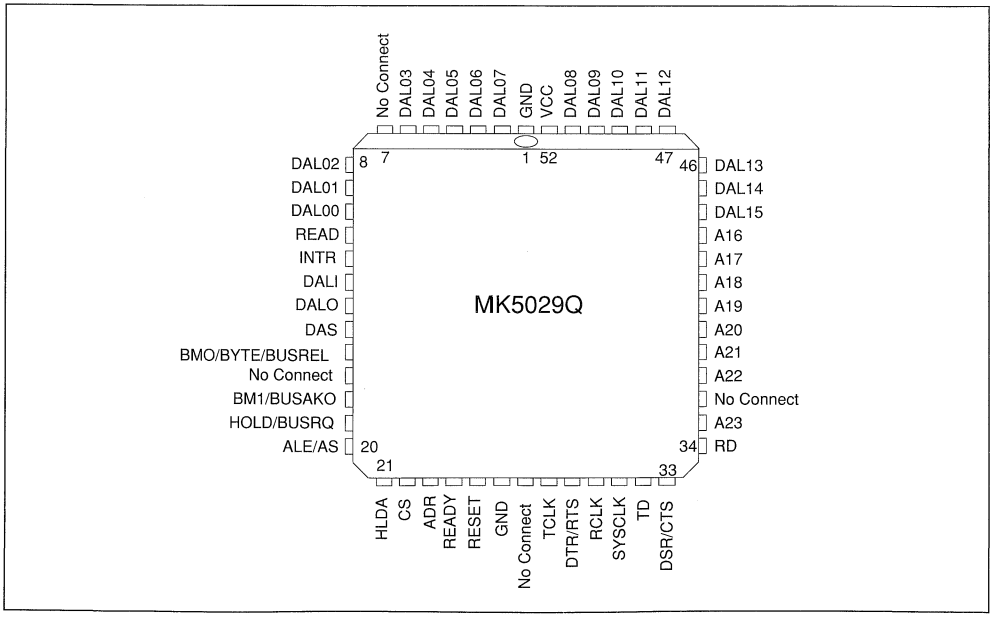


Table 1 : PIN DESCRIPTION

LEGEND:

I	Input only	O	Output only
IO	Input / Output	3S	3-State
OD	Open Drain (no internal pull-up)		

Note: Pin out for 52 pin PLCC is shown in brackets.

Signal Name	Pin(S)	Type	Description
DAL<15:00>	2-9 40-47 [2-10 44-51]	IO/3S	The time multiplexed Data/Address bus. During the address portion of a memory transfer, DAL<15:00> contains the lower 16 bits of the memory address. During the data portion of a memory transfer, DAL<15:00> contains the read or write data, depending on the type of transfer.
READ	10 [11]	IO/3S	READ indicates the type of operation that the bus controller is performing during a bus transaction. READ is driven by the MK5029 only while it is the BUS MASTER. READ is valid during the entire bus transaction and is tristated at all other times. MK5029 as a Bus Slave : READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip. MK5029 as a Bus Master READ = HIGH - Data is taken off the DAL lines by the chip. READ = LOW - Data is placed on the DAL lines by the chip.
$\overline{\text{INTR}}$	11 [12]	O/OD	INTERRUPT is an attention interrupt line that indicates that one or more of the following CSR0 status flags is set: MISS, MERR, RINT, TINT or PINT. INTERRUPT is enabled by CSR0<09>, INEA=1.
$\overline{\text{DALI}}$	12 [13]	O/3S	DAL IN is an external bus transceiver control line. $\overline{\text{DALI}}$ is driven by the MK5029 only while it is the BUS MASTER. $\overline{\text{DALI}}$ is asserted by the MK5029 when it reads from the DAL lines during the data portion of a READ transfer. $\overline{\text{DALI}}$ is not asserted during a WRITE transfer.
$\overline{\text{DALO}}$	13 [14]	O/3S	DAL OUT is an external bus transceiver control line. $\overline{\text{DALO}}$ is driven by the MK5029 only while it is the BUS MASTER. $\overline{\text{DALO}}$ is asserted by the MK5029 when it drives the DAL lines during the address portion of a READ transfer or for the duration of a WRITE transfer.

Table 1 : PIN DESCRIPTION (Continued)

Signal Name	Pin(S)	Type	Description
$\overline{DAS}$	14 [15]	IO/3S	DATA STROBE defines the data portion of a bus transaction. By definition, data is stable and valid at the low to high transition of DAS. This signal is driven by the MK5029 while it is the BUS MASTER. During the BUS SLAVE operation, this pin is used as an input. At all other times the signal is tristated.
$\overline{BMO}$ BYTE BUSREL	15 [16]	IO/3S	I/O pins 15 and 16 are programmable through CSR4. If bit 06 of CSR4 is set to a one, pin 15 becomes input BUSREL and is used by the host to signal the MK5029 to terminate a DMA burst after the current bus transfer has completed. If bit 06 is clear then pin 15 is an output and behaves as described below for pin 16.
$\overline{BM1}$ BUSAKO	16 [18]	O/3S	Pins 15 and 16 are programmable through bit 00 of CSR4 (BCON). If CSR4<00> BCON = 0, I/O PIN 15 = $\overline{BMO}$ (O/3S) I/O PIN 16 = $\overline{BM1}$ (O/3S) BYTE MASK<1:0> Indicates the byte(s) on the DAL to be read or written during this bus transaction. MK5029 drives these lines only as a Bus Master. MK5029 ignores the BM lines when it is a Bus Slave. Byte selection is done as outlined in the following table. $\overline{BM1}$ $\overline{BM0}$ TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH UPPER BYTE (DAL<15:08>) HIGH LOW LOWER BYTE (DAL<07:00>) HIGH HIGH NONE If CSR4<00> BCON = 1, I/O PIN 15 = BYTE (O/3S) I/O PIN 16 = BUSAKO (O) Byte selection is done using the BYTE line and DAL<00> latched during the address portion of the bus transaction. MK5029 drives BYTE only as a Bus Master and ignores it when a Bus Slave. Byte selection is done as outlined in the following table BYTE DAL<00> TYPE OF TRANSFER LOW LOW ENTIRE WORD LOW HIGH ILLEGAL CONDITION HIGH LOW LOWER BYTE HIGH HIGH UPPER BYTE

Table 1 : PIN DESCRIPTION (Continued)

Signal Name	Pin(S)	Type	Description
			BUSAKO is a bus request daisy chain output. If MK5029 is not requesting the bus and it receives HLDA, BUSAKO will be driven low. If MK5029 is requesting the bus when it receives HLDA, BUSAKO will remain high. Note: All transfers are entire word unless the MK5029 is configured for 8 bit operation.
HOLD BUSRQ	17 [19]	IO/OD	Pin 17 is configured through bit 0 of CSR4. If CSR4<00> BCON = 0, I/O PIN 17 = HOLD HOLD request is asserted by MK5029 when it requires a DMA cycle, if HLDA is inactive, regardless of the previous state of the HOLD pin. HOLD is held low for the entire ensuing bus transaction. If CSR4<00> BCON = 1, I/O PIN 17 = BUSRQ BUSRQ is asserted by MK5029 when it requires a DMA cycle if the prior state of the BUSRQ pin was high and HLDA is inactive. BUSRQ is held low for the entire ensuing bus transaction.
ALE AS	18 [20]	O/3S	The active level of ADDRESS STROBE is programmable through CSR4. The address portion of a bus transfer occurs while this signal is at its asserted level. This signal is driven by MK5029 while it is the BUS MASTER. At all other times, the signal is tristated. If CSR4<01> ACON = 0, I/O PIN 18 = ALE ADDRESS LATCH ENABLE is used to demultiplex the DAL lines and define the address portion of the transfer. As ALE, the signal transitions from high to low during the address portion of the transfer and remains low during the data portion. If CSR4<01> ACON = 1, I/O PIN 18 = AS As AS, the signal pulses low during the address portion of the bus transfer. The low to high transition of AS can be used by a slave device to strobe the address into a register. AS is effectively the inversion of ALE.
HLDA	19 [21]	I	HOLD ACKNOWLEDGE is the response to HOLD. When HLDA is low in response to MK5029's assertion of HOLD, the MK5029 is the Bus Master. HLDA should be deasserted ONLY after HOLD has been released by the MK5029.

Table 1 : PIN DESCRIPTION (Continued)

Signal	Pin(S)	Type	Description
$\overline{CS}$	20 [22]	I	CHIP SELECT indicates, when low, that the MK5029 is the slave device for the data transfer. $\overline{CS}$ must be valid throughout the entire transaction.
ADR	21 [23]	I	ADDRESS selects the Register Address Port or the Register Data Port. It must be valid throughout the data portion of the transfer and is only used by the chip when $\overline{CS}$ is low. ADR PORT LOW REGISTER DATA PORT HIGH REGISTER ADDRESS PORT
$\overline{READY}$	22 [24]	IO/OD	When the MK5029 is a Bus Master, $\overline{READY}$ is an asynchronous acknowledgement from the bus memory that memory will accept data in a WRITE cycle or that memory has put data on the DAL lines in a READ cycle. As a Bus Slave, the MK5029 asserts $\overline{READY}$ when it has put data on the DAL lines during a READ cycle or is about to take data from the DAL lines during a WRITE cycle. $\overline{READY}$ is a response to $\overline{DAS}$ and it will be released after $\overline{DAS}$ or $\overline{CS}$ is negated.
$\overline{RESET}$	23 [25]	I	$\overline{RESET}$ is the Bus signal that will cause MK5029 to cease operation, clear its internal logic and enter an idle state with the Power Off bit of CSR0 set.
$\overline{TCLK}$	25 [28]	I	TRANSMIT CLOCK. A 1x clock input for transmitter timing. TD changes on the falling edge of $\overline{TCLK}$. The frequency of $\overline{TCLK}$ may not be greater than the frequency of SYSCLK.
$\overline{DTR}$ $\overline{RTS}$	26 [29]	IO	DATA TERMINAL READY, REQUEST TO SEND. Modem control pin. Pin 26 is configurable through CSR5. This pin can be programmed to behave as output $\overline{RTS}$ or as programmable IO pin DTR. If configured as $\overline{RTS}$, the MK5029 will assert this pin if it has data to send and throughout the transmission of a signal unit.
$\overline{RCLK}$	27 [30]	I	RECEIVE CLOCK. A 1x clock input for receiver timing. RD is sampled on the rising edge of $\overline{RCLK}$. The frequency of $\overline{RCLK}$ may not be greater than the frequency of SYSCLK.
SYSCLK	28 [31]	I	SYSTEM CLOCK. System clock used for internal timing of the MK5029. SYSCLK should be a square wave, of frequency up to 10 MHz.
TD	29 [32]	O	TRANSMIT DATA. Transmit serial data output.

Table 1 : PIN DESCRIPTION (Continued)

Signal	Pin(S)	Type	DescriptioN
DSR CTS	30 [33]	IO	DATA SET READY, CLEAR TO SEND. Modem Control Pin. Pin 30 is configurable through CSR5. This pin can be programmed to behave as input CTS or as programmable IO pin DSR. If configured as CTS, the MK5029 will transmit all ones while CTS is high.
RD	31 [34]	I	RECEIVE DATA. Received serial data input.
A<23:16>	32-39 [37-43]	O/3S	Address bits <23:16> used in conjunction with DAL<15:00> to produce a 24 bit address. MK5029 drives these lines only as a Bus Master. A23-A20 may be driven continuously as described in the CSR4<7> BAE bit.
VSS-GND	1, 24 [1, 26]		Ground Pins
VCC	52		Power Supply Pin +5.0 VDC + - 5%

SECTION 4: PROGRAMMING SPECIFICATION

This section defines the Control and Status Registers and the memory data structures required to program the MK5029.

4.1 Control and Status Registers

There are six Control and Status Registers (CSR's) resident within the MK5029. The CSR's are accessed through two bus addressable ports, an address port (RAP), and a data port (RDP), thus requiring only two locations in the system memory or I/O map.

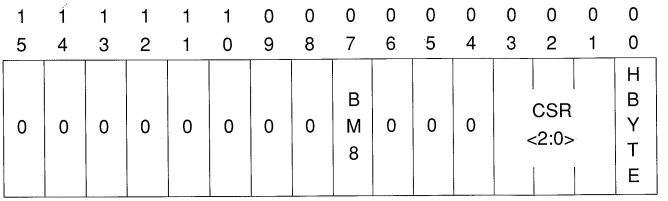
4.1.1 Accessing the Control and Status Registers

The CSR's are read (or written) in a two step operation. The address of the CSR is written into the address port (RAP) during a bus slave transaction.

During a subsequent bus slave transaction, the data being read from (or written into) the data port (RDP) is read from (or written into) the CSR selected in the RAP. Once written, the address in RAP remains unchanged until rewritten or upon a bus reset. A control I/O pin (ADR) is provided to distinguish the address port from the data port.

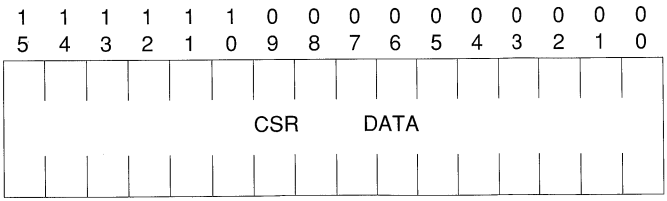
ADR	Port
L	Register Data Port (RDP)
H	Register Address Port (RAP)

4.1.1.1 Register Address Port (RAP)



BIT	NAME	DESCRIPTION
15:08	RESERVED	Must be written as zeroes.
07	BM8	When set, places chip into 8 bit mode. CSR's, Init Block, and data transfers are all 8 bit trans fers; this providescompatibility with 8 bitmicroprocessors. When clear, all transfers are 16 bit transfers. This bit must be set to the same value each time it is written, changing this bit during normal operation will achieve unexpected results. BM8 is READ/WRITE and cleared on Bus RESET.
06:04	RESERVED	Must be written as zeroes.
03:01	CSR DATA	CSR address select bits. READ/WRITE. Selects the CSR to be accessed through the RDP. RAP is cleared by Bus RESET. CSR<2:0> CSR0 1 CSR1 2 CSR2 3 CSR3 4 CSR4 5 CSR5
00	HBYTE	Determines which byte is addressed for 8 bit mode. If set, the high byte of the register referred to by CSR<2:0> is addressed, otherwise the low byte is addressed. This bit is only meaningful in 8 bit mode and must be written as zero if BM8=0. HBYTE is READ/WRITE and cleared on bus reset.

4.1.1.2 Registers Data Port (RDP)



BIT	NAME	DESCRIPTION
15:00	CSR DATA	Writing data to the RDP loads data into the CSR selected by RAP. Reading the data from RDP reads the data from the CSR selected in RAP.

4.1.2 Control and Status Register Definition

4.1.2.1 Control and Status Register 0 (CSR0)

RAP<3:1> = 0

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TDMD	STOP	DTX	DRX	TXON	RXON	INEA	INTR	MERR	MISS	ROR	TUR	PINT	TINT	RINT	0

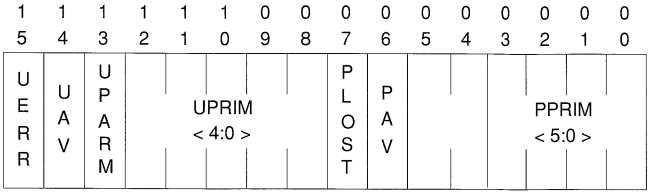
BIT	NAME	DESCRIPTION
15	TDMD	TRANSMIT DEMAND, when set in Transparent Mode, causes MK5029 to access the Transmit Descriptor Ring. TDMD should not be set to transmit a frame in protocol mode, it should only be used in Transparent mode to cause the MK5029 to transmit a frame in response to a Transmit Descriptor Ring entry insertion by the host. TDMD is written with ONE ONLY and cleared by the microcode after it is used. It may read as a "1" for a short time after it is written because the microcode may have been busy when TDMD was set. It is also cleared by Bus RESET. Writing a "0" in this bit has no effect.
14	STOP	STOP, when set, indicates that MK5029 is operating in the Stopped phase of operation. All external activity is disabled and internal logic is reset. MK5029 remains inactive except for primitive processing until a START primitive is issued. STOP IS READ ONLY and set by Bus RESET or a STOP primitive. Writing to this bit has no effect.
13	DTX	Disable Transmitter ring prevents the MK5029 from further access to the Transmitter Descriptor Ring. No transmissions are attempted after finishing transmission of any frame in transmission at the time of DTX being set. TXON acknowledges changes to DTX, see below. DTX is READ/WRITE.
12	DRX	Disable the Receiver prevents the MK5029 from further access to the Receiver Descriptor Ring. No received frames are accepted after finishing reception of any frame in reception at the time of DRX being set. RXON acknowledges changes to DRX, see description of RXON. DRX is READ/WRITE.
11	TXON	TRANSMITTER ON indicates that the transmit ring access is enabled. TXON is set as the Start primitive is issued if the DTX bit is "0" or afterward as DTX is cleared. TXON is cleared upon recognition of DTX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. If TXON is clear, the host may modify the Transmit Descriptor Ring entries regardless of the state of the OWNA bits. TXON is READ ONLY; writing to this bit has no effect.

10	RXON	RECEIVER ON indicates that the receive ring access is enabled. RXON is set as the Start primitive is issued if the DRX bit is "0" or afterward as DRX is cleared. RXON is cleared upon recognition of DRX being set, by sending a Stop primitive in CSR1, or by a Bus RESET. RXON is READ ONLY; writing to this bit has no effect.
09	INEA	INTERRUPT ENABLE allows the $\overline{\text{INTR}}$ I/O pin to be driven low when the Interrupt Flag is set. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. If INEA = 0 the $\overline{\text{INTR}}$ I/O pin will be high, regardless of the state of the Interrupt Flag. INEA is READ/WRITE set by writing a "1" into this bit and is cleared by writing a "0" into this bit, by Bus RESET, or by issuing a Stop primitive. INEA may not be set while in the Stopped phase.
08	INTR	INTERRUPT FLAG indicates that one or more of the following interrupt causing conditions has occurred: MISS, MERR, RINT, TINT, PINT. If INEA = 1 and INTR = 1 the $\overline{\text{INTR}}$ I/O pin will be low. INTR is READ ONLY, writing this bit has no effect. INTR is cleared as the specific interrupting condition bits are cleared. INTR is also cleared by Bus RESET or by issuing a Stop primitive.
07	MERR	MEMORY ERROR is set when the MK5029 is the Bus Master and $\overline{\text{READY}}$ has not been asserted within 256 SYSCLKs (25.6 usec @ 10MHz) after asserting the address on the DAL lines. When a Memory Error is detected, the MK5029 releases the bus, the receiver and transmitter are turned off, and an interrupt is generated if INEA = 1. MERR is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
06	MISS	MISSED frame is set when the receiver loses a frame because it does not own a receive buffer indicating loss of data. When MISS is set, an interrupt will be generated if INEA = 1. MISS is READ/CLEAR ONLY and is set by MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
05	ROR	RECEIVER OVERRUN indicates that the Receiver FIFO was full when the receiver was ready to input data to the Receiver FIFO. The frame being received is lost, but is probably recoverable if an upper level protocol is used. When ROR is set, an interrupt is generated if INEA = 1. ROR is READ/CLEAR ONLY and is set by MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
04	TUR	TRANSMITTER UNDERRUN indicates that the MK5029 has aborted a frame since data was late from memory. This condition is reached when the transmitter and transmitter FIFO both become empty while transmitting a frame. When TUR is set, an interrupt is generated if INEA = 1. TUR is READ/CLEAR ONLY and is set by MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.

03	PINT	PRIMITIVE INTERRUPT is set after the chip updates the primitive register to issue a provider primitive. When PINT is set, an interrupt is generated if INEA =1. PINT is READ/CLEAR ONLY and is set by MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
02	TINT	TRANSMITTER INTERRUPT is set after the chip updates an entry in the Transmit Descriptor Ring. When TINT is set, an interrupt is generated if INEA = 1. TINT is READ/CLEAR ONLY and is set by the MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is also cleared by Bus RESET or by issuing a Stop primitive.
01	RINT	RECEIVER INTERRUPT is set after the MK5029 updates an entry in the Receive Descriptor Ring. When RINT is set, an interrupt is generated if INEA = 1. RINT is READ/CLEAR ONLY and is set by the MK5029 and cleared by writing a "1" into the bit. Writing a "0" has no effect. It is cleared by Bus RESET or by issuing a Stop primitive.
00	0	This bit is READ ONLY and will always read as a zero.

4.1.2.2 Control and Status Register 1 (CSR1)

RAP <3:1> = 1



15 UERR

USER PRIMITIVE ERROR is set by the MK5029 when a primitive is issued by the user which is in conflict with the current status of the chip. UERR is READ/CLEAR ONLY and is set by MK5029 and cleared by writing a "1" into the bit. Writing a "0" in this bit has no effect. It is also cleared by Bus RESET.

14 UAV

USER PRIMITIVE AVAILABLE is set by the user when a primitive is written into UPRIM. It is cleared by the MK5029 after the primitive has been processed. This bit is also cleared by a Bus RESET.

13 UPARN

USER PARAMETER is written by the host in conjunction with the user primitives in UPRIM. This User Parameter field provides information to the MK5029 concerning the corresponding user primitive. For connect and reset primitives this field determines what the MK5029 will do with frames in the transmit descriptor ring which have previously been sent but not acknowledged. If UPARM = 0, these frames will be resent when the new link is established. If UPARM = 1, these frames will be discarded and their OWNA bits cleared, releasing ownership back to the host. For other primitives UPARM = 0 unless otherwise indicated.

12 UPRIM

USER PRIMITIVE is written by the user, in conjunction with setting UAV, to control the MK5029 link procedures. The following primitives are available:

0 Stop: Causes MK5029 to enter the Stopped mode or phase. All DMA activity ceases, the transmitter transmits all ones, and all received data is ignored.

1 Start: Instructs the MK5029 to exit the Stopped phase and enter the Disconnected phase, if UPARM = 0. The descriptor Rings are reset. The transmitter begis to output flags. If issued with UPARM = 1 the MK5029 will directly enter the Information Transfer phase (link connected). Valid only in Stopped Mode or Transparent Mode.

2 Init: Instructs the MK5029 to read the Initialization Block from memory. Valid only in the Stopped mode or phase. This should be performed prior to the Start primitive after a bus reset or power-up.

3 Trans: Instructs MK5029 to enter the Transparent phase of operation. Data frames are transmitted and received out of the descriptor rings with no Address and Control fields prepended to the frames. If the PROM bit is set in the Protocol Parameters register, then no address filtering is performed on received frames. Transparent Mode may be exited with a Stop primitive or by a bus reset. Exiting from Transparent Mode to the information transfer phase (link connected) is possible by issuing a Start primitive with UPARM = 1, or to the Disconnected phase by issuing Start with UPARM = 0.

4 Status Request: Instructs the MK5029 to write the current chip status into the STATUS BUFFER. Valid in all states, but only after the Init primitive has been previously issued.

5 Self-Test Request: Instructs the MK5029 to perform the built in internal self test. Valid only in the Stopped phase. See section 4.4.12 for the self test procedure.

7 Connect Response: Indicates willingness to establish a logical link with the primary station. Valid only in Disconnected phase after receiving a Connect Indication primitive.

8 SIM Response: Indicates willingness to initialize the secondary station (sends UA in response to SIM). Valid only after receiving a IM Indication primitive. In Transparent mode instructs the MK5029 to start the timer T1.

9 Reset Response: If a logical link has been established, indicates willingness to reset current logical link with remote site (sends UA in response to SNRM). Valid only after receiving Reset Indication primitive. In Transparent mode instructs the MK5029 to stop the T1 timer.

10 RIM Response: Instructs the MK5029 to send a RIM frame at its next. poll opportunity. If UPARM = 1, then RIM/F=1 will be sent, otherwisise, RIM/F=0 will be sent.

11 XID Response: Instructs the MK5029 to send an XID response frame at its next poll opportunity. Data in the XID/TEST/CFGR transmit buffer is used for the data field. Valid only after receiving an XID Indication primitive.

12 CFGR Response: Instructs MK5029 to send CFGR response frame at its next poll opportunity. Data in the XID/TEST/CFGR transmit buffer is used for the data field. Valid only after receiving a CFGR Indication primitive.

13 TEST Response: Instructs MK5029 to send a TEST response frame at its next poll opportunity. Data in XID/TEST/CFGR transmit buffer is used for the data field. Valid only after receiving TEST Indication primitive.

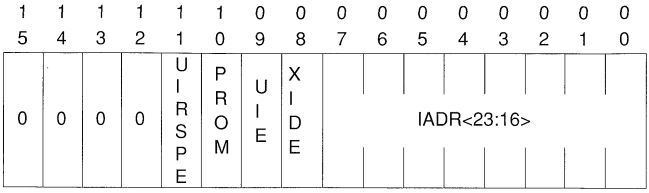
14 Disconnect Request: Instructs the MK5029 to send a DM frame at its next poll opportunity, and enter the Normal Disconnected phase.

15 RD Response: Instructs MK5029 to request to disconnect by sending a RD response frame at its next poll opportunity. If UPARM= 1, then RD/F = 1 will be sent. Otherwise, RD/F = 0 will be sent.

07	PLOST		PROVIDER PRIMITIVE LOST is set by the MK5029 when a provider primitive cannot be issued because the PAV bit is still set from the previous provider primitive. PLOST is cleared when PAV is cleared or by a Bus RESET. Writing to this bit has no effect.
06	PAV		PAV PROVIDER PRIMITIVE AVAILABLE is set by the MK5029 when a new provider primitive has been placed in PPRIM. PAV is READ/CLEAR ONLY and is set by the chip and cleared by writing a "1" to the bit or by Bus RESET. Under normal operation the host should clear the PAV bit after PPRIM is read.
05:00	PPRIM		PROVIDER PRIMITIVE is written by the MK5029, in conjunction with with setting the PAV bit, to inform the user of link control conditions. Valid Provider Primitives are as follows:
		0	IM Indication: Indicates that the MK5029 received a SIM command. Valid only if SIME bit in Protocol Parameters register is set..
		1	IM Confirmation: Indicates the success of the initialization of the local station. All MK5029 link state variables are reset to zero.
		2	Init Confirmation: Indicates MK5029 Init Block reading has completed.
		6	Connect Indication: Indicates an attempt by the Primary station to establish a logical link (SNRM received). Appropriate user responses are Connect Response or Disconnect Request.
		8	Reset Indication: If a logical link has been established, indicates an attempt by the Primary station to reset the current logical link (SNRM received). Appropriate user responses are Reset Response or Disconnect Request. In the Transparent Mode, indicates the expiration of the T1 timer.
		9	Reset Confirmation: Indicates the Secondary is in reset state. (ie; UA is sent in response to SNRM)
		10	XID Indication: Indicates the receipt of an XID command. The data field of the XID command is located in the XID/TEST/CFGR receive buffer. Valid only if XIDE bit in CSR2 is set.
		11	UI Indication: Indicates receipt of UI command. UI data field in receive buffer. Valid only if UIRSPE bit in CSR2 is set.
		12	TEST Indication: Indicates the receipt of TEST command. The data field of the TEST command is located in the XID/TEST/CFGR receive buffer. Valid only if TESTE bit in Protocol Parameters register is set.
		13	CFGR Indication: Indicates receipt of a CFGR command. The data field of the CFGR command is located in the XID/TEST/CFGR receive buffer. Valid only if CFGRE bit in Protocol Parameters register is set.
		14	Disconnect Indication: Indicates request by the primary to disconnect the current logical link (DISC received). The chip is now in the Disconnected phase.

4.1.2.3 Control and Status Register 2 (CSR2)

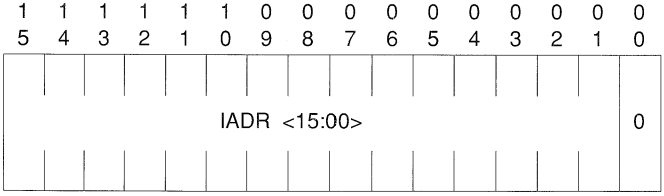
RAP<3:1> = 2



BIT	NAME	DESCRIPTION
15:12	0	Reserved, must be written as zeroes.
11	UIRSPE	UIRSPE Should be set only if a UI frame needs to be transmitted in response to a received UI command. Otherwise a UA frame will be automatically transmitted in response to a received UI command.
10	PROM	PROM Promiscuous mode. Address filtering is disabled in Transparent Mode if this bit is set. All uncorrupted incoming frames are placed in the Received Descriptor Ring. Should be set only in Transparent Mode.
09	UIE	UI frames are recognized only if this bit is set.
08	XIDE	Bit. XID frames are recognized only if this bit is set.
07:00	IADR	The high order 8 bits of the address of the first word (lowest address) in the Initialization Block. IADR must be written by the Host prior to issuing an INIT primitive.

4.1.2.4 Control and Status Register 3 (CSR3)

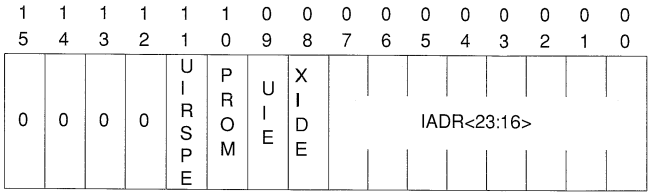
RAP<3:1> = 3



BIT	NAME	DESCRIPTION
15:00	IADR	The low order 16 bits of the address of the first word (lowest address) in the Initialization Block. Must be written by the Host prior to issuing an INIT primitive. The Initialization block must begin on a word boundary.

4.1.2.5 Control and Status Register 4 (CSR4)

CSR4 allows redefinition of the bus master interface.
RAP<3:1> = 4

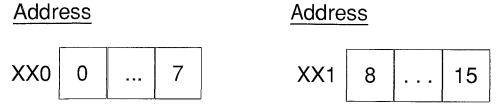


BIT	NAME	DESCRIPTION
15:10	0	Reserved, must be written as zeroes.
09:08	FWM	These bits define the FIFO watermarks. FIFO watermarks prevent the MK5029 from performing DMA transfers to/from the data buffers until the FIFOs contain a minimum amount of data or space for data. For receive, data will only be transferred to the buffers after the FIFO has at least N 16-bit words or end of frame has been reached. Conversely, for transmit, data will only be transferred from the data buffers when the transmit FIFO has room for at least N words of data. N is defined as follows:

FWM<1:0>	N
1 word10*	9 words
01	17 words
00	25 words

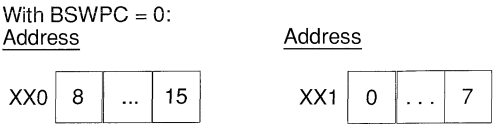
* Suggested setting

07	BAE	Bus Address Enable: if BAE is set then the A23-A20 pins are driven by the MK5029 constantly providing the ability to use A23-A20 for memory bus selection. If clear, A23-A20 behave identically to A19- A16.
06	BUSR	If this bit is set, pin 15 becomes input $\overline{\text{BUSREL}}$. If this bit is clear then pin 15 is either $\overline{\text{BM0}}$ or BYTE depending on bit 00. For more information see the description for pin 15 in this document. BUSR is READ/WRITE and cleared on bus Reset.
05	BSWPC	This bit determines the byte ordering of all "non-data" DMA transfers. This transfers refers to any DMA transfers that access memory other than the data buffers themselves. This includes the Initialization Block, Descriptors, and Status Buffer. It has no effect on data DMA transfers. BSWPC allows the MK5029 to operate with memory organizations that have bits 07:00 at even addresses and with bits 15:08 at odd addressses or vice versa. BSWPC is Read/Write and cleared by BUS RESET. With BSWPC = 1:



This memory organization is used with the LSI 11 microprocessor and the 8086 microprocessor.

With BSWPC = 0:



This memory organization is used with the 68000 and the Z8000 microprocessors.

04:03 BURST

This field determines the maximum number of data transfers performed each time control of the host bus is obtained. BURST is READ/WRITE and cleared on bus Reset.

BURST<1:0>	8 bit mode	16 bit mode
00	21	1
10*	16	8
01	unlimited	unlimited

* Suggested setting

02 BSWPD

This bit determines the byte ordering of all data DMA transfers. Data transfers are those to or from a data buffer. BSWPD has no effect on non-data transfers. The effect of BSWPD on data transfers is the same as that of BSWPC on non-data transfers (see above). For most applications, including most 68000 based systems, this bit should be set.

01 ACON

ALE CONTROL defines the assertive state of pin 18 when the MK5029 is a Bus Master. ACON is READ/ WRITE and cleared by Bus RESET.

ACON	PIN18	NAME
0	ASSERTED HIGH	ALE
1	ASSERTED LOW	$\overline{AS}$

00 BCON

BYTE CONTROL redefines the Byte Mask and Hold I/O pins BCON is READ/WRITE and cleared by Bus RESET.

BCON	PIN16	PIN15	PIN17
0	BM 1	BM 0	HOLD
1	$\overline{BUSAKO}$	BYTE	$\overline{BUSRQ}$

4.1.2.6 Control and Status Register 5 (CSR5)

CSR5 facilitates control and monitoring of modem controls.
RAP<3:1> = 5

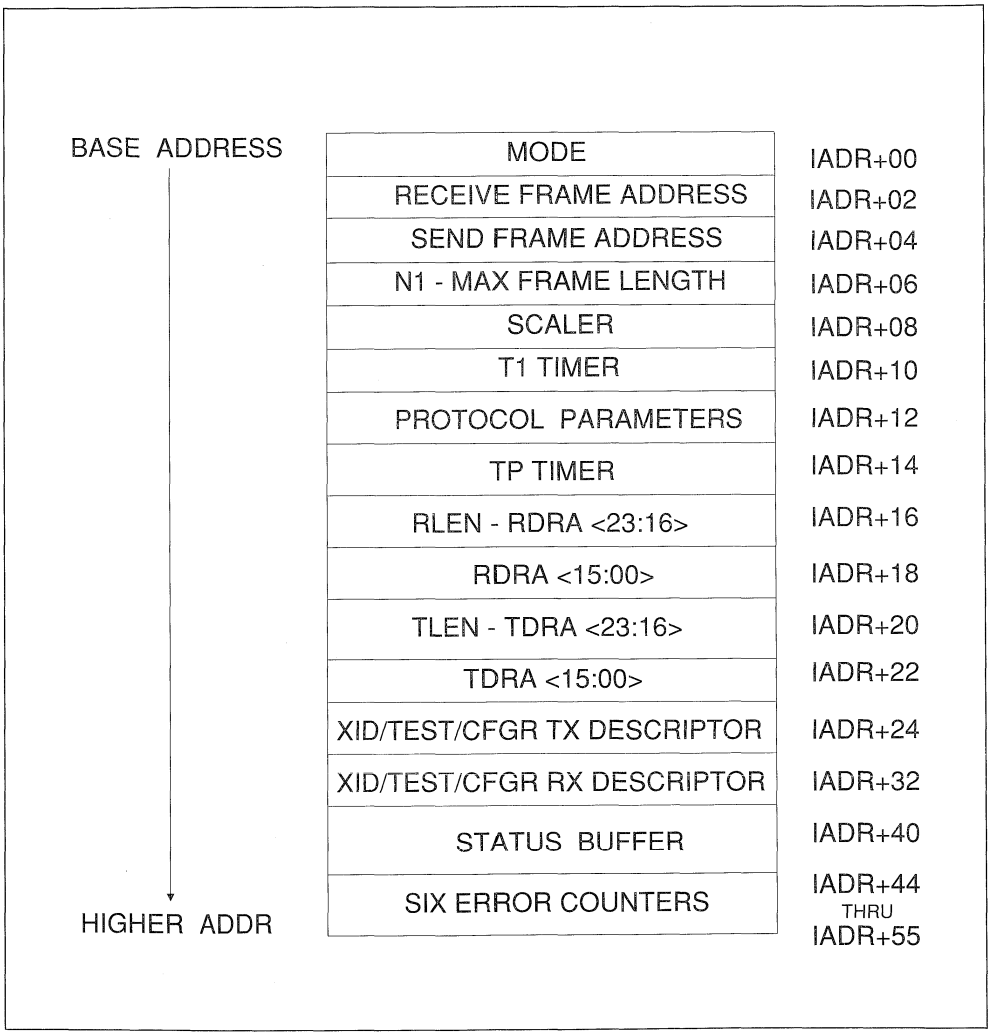
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	0	0	0	RTSEN	DTRD	DSRD	DTR	DSR

BIT	NAME	DESCRIPTION
15:05	0	Reserved, must be written as zeroes.
4	RTSEN	RTS/CTS ENABLE is a READ/WRITE bit used to configure pins 26 and 30. If this bit is set, pin 26 becomes $\overline{RTS}$ and pin 30 becomes $\overline{CTS}$. $\overline{RTS}$ is driven low whenever the MK5029 has data to transmit and is kept low during transmission. $\overline{RTS}$ will be driven high after the closing flag of a signal unit is transmited if either no other frames are in the FIFO or if the minimum signal unit spacing is higher than 2 (see Mode Register). The MK5029 will not begin transmission and TD will remain HIGH if $\overline{CTS}$ is high. If RTSEN = 0 then pins 26 and 30 become programmable I/O pins DTR and DSR. The direction and behavior of DSR and DTR are controlled by the following bits.
3	DTRD	DTR DIRECTION is a READ/WRITE bit used to control the direction of the DTR/RTS pin. If DTRD = 0, the DTR/RTS pin becomes an input pin and the DTR bit reflects the current value of the pin; if DTRD = 1, the DTR/RTS pin is an output pin controlled by the DTR bit below.
2	DSRD	DSR DIRECTION is a READ/WRITE bit used to control the direction of the DSR/CTS pin. If DSRD = 0, the DSR/CTS pin becomes an input pin and the DSR bit reflects the current value of the pin; if DSRD = 1, the DSR/CTS pin is an output pin controlled by the DSR bit below.
1	DTR	DATA TERMINAL READY is used to control or observe the DTR I/O pin depending on the value of DTRD. If DTRD = 0, this bit becomes READ ONLY and always equals the current value of the DTR/RTS pin. If DTRD = 1, this bit becomes READ/WRITE and any value written to this bit appears on the DTR/RTS pin.
0	DSR	DATA SET READY is used to control or observe the DSR I/O pin depending on the value of DSRD. If DSRD = 0, this bit becomes READ ONLY and always equals the current value of the DSR/CTS pin. If DSRD = 1 this bit becomes READ/WRITE and any value written to this bit appears on the DSR/CTS pin.

4.2 Initialization Block

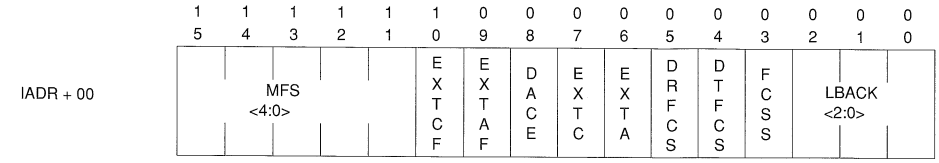
MK5029 initialization includes the reading of the Initialization Block in memory to obtain the operating parameters. The Initialization Block is defined below. Upon receiving an Init primitive, portions of the Initialization block are read by the MK5029. The remainder of the Initialization block will be read as needed by the MK5029.

Figure 4 : Initialization Block



4.2.1 Mode Register

The Mode Register allows alteration of the MK5029's operating parameters.



BIT	NAME	DESCRIPTION
15:11	MFS<4:0>	Minimum Frame Spacing defines the minimum number of flag sequences transmitted between adjacent frames transmitted by the MK5029. This only affects frames transmitted by the MK5029 and does not restrict the spacing of the frames received by the MK5029. When using RTS/CTS control this field defines the number of flags transmitted at the beginning of the frame after CTS is driven low (minus one for the trailing flag). See the following table for encoding of this field.
10	EXTCF	Extended Control Force. If set along with EXTC, the receiver will assume the control field to be two octets long regardless of the first two bits of the control field. See EXTC below.
09	EXTAF	Extended Address Force. If set along with EXTA, the receiver will assume the address to be two octets long regardless of the first bit of the address. See EXTA below.
08	DACE	Address and control field extraction are disabled when DACE is set Address and control fields are treated as data and placed in memory as such. DACE must be written with "1" for normal transparent data transfer operation, but can be set to "0" for doing address and control field filtering.

NUMBER OF FLAGS	MFS<4:0>	NUMBER OF FLAGS	MFS<4:0>
1	1	32	28
2	0	34	24
4	2	36	17
6	4	38	3
8	9	40	6
10	18	42	13
12	5	44	27
14	11	46	23
16	22	48	14
18	12	50	29
20	25	52	26
22	19	54	21
24	7	56	10
26	15	58	20
28	31	60	8
30	30	62	16

07	EXTC	Extended Control Field filtering is enabled when EXTC = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).
06	EXTA	Extended Address Field filtering is enabled when EXTA = 1 if DACE = 0 and PROM = 0 (PROM is in CSR2).
05	DRFCS	Disable Receiver FCS (CRC). When DRFCS = 0, the receiver will extract and check the FCS field at the end of each frame. When DRFCS = 1, the receiver continues to extract the last 16 or 32 bits of each frame, depending on FCSS, but no check is performed to determine whether the FCS is correct. If the received frame is an even number of bytes, the first 16 bits of the FCS will be appended to the end (as indicated by MCNT) of the receive Receive buffer data.
04	DTFCS	Disable Transmitter FCS. When DTFCS=0, the transmitter will generate and append the FCS to each signal unit. When DTFCS = 1, the FCS logic is disabled, and no FCS is generated with transmitted frames. Setting DTFCS = 1 is useful in loopback testing for checking the ability of the receiver to detect an incorrect FCS.
03	FCSS	FCS Select. When FCSS = 1, a 16-bit FCS is selected otherwise a 32-bit FCS is used.
02:00	LBACK	Loopback Control puts MK5029 into one of several loopback configurations.

LBACK	DESCRIPT
0	Normal operation. No loopback.
4	Simple loopback. Receive data and clock are driven internally by transmit data and clock. Transmit clock must be supplied externally.
5	Clockless loopback. Receive data is driven internally by transmit data. Transmit and receive clocks are driven by SYSCLK divided by 8.
6	Silent loopback. Same as simple loopback with TD pin forced to all ones.
7	Silent clockless loopback. Combination of Silent and Clockless loopbacks. Receive data is driven internally by transmit data, transmit and receive clocks are driven by SYSCLK divided by 8. The TD pin is forced to all ones.

4.2.2 Protocol Parameters Register

IADR+12

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	0	0	0	0	0	0	0	SIME	0	CFGRE	UPE	TESTE	0	0	0

The Protocol Parameters Register defines the MK5029 protocol options to be used.

BIT	NAME	DESCRIPTION
15:08	0	Reserved. Must be written as zeroes.
07	SIME	SIM frames are recognized only if this bit is set.
06	0	Reserved. Must be written as a zero.
05	CFGRE	CFGR frames are recognized only if this bit is set.
04	UPE	UP frames are recognized only if this bit is set.
03	TESTE	TEST frames are recognized only if this bit is set.
02:00	0	Reserved. Must be written as zeroes.

4.2.3 Station Address and Control Field Filtering

The Send and Receive frame addresses may be either one or two octets according to the EXTA control bit described in the MODE register. If extended address mode filtering is selected, bit zero of the address field should be set to a zero if adherening to HDLC standards. If extended address filtering is not selected, frame adresses should be located in the lower order byte of of their respective fields. The address filtering is a one octet compare if the extended address bit, EXTA is 0 (Mode register bit 06), or follows the HDLC rules for extended addressing if EXTA is 1. Frames not matching either address are ignored.

In the MK5029, address filtering and control field handling applies only to octet aligned frames received with good FCS. Any frame not meeting both of these conditions is discarded and the "Bad Frames Received" error counter (located at IADR + 44 of the Initialization Block) is incremented.

Extended control field filtering is also possible using the EXTC bit (Mode Register bit 07), as shown in Table 2 and Table 3. If EXTC is 0 then the C-field is one octet for all frames. If however EXTC is set to 1, the MK5029 will look to see if either of the two least significant bits of the C-field is 0. If so, the frame is said to have an extended control field which is two octets. In addition, bits EXTAF and EXTCF (Mode Register bit 09 & 10) are useful to force extended address and control. If EXTAF is set along with EXTA, the receiver will assume the address field to be two bytes long regardless of the first bit of the address field. If EXTCF is set along with EXTC, the receiver will assume the contol field to be two bytes long regardless of the first two bits of that field.

The following table shows the MK5029 address filtering options and handling of the received Address field.

In Transparent Mode, address filtering is supported if the PROM bit (CSR2 register, bit 10) is 0. In this case, frames are accepted if the received Address field matches either the Send Frame Address or the Receive Frame Address as specified in the Initialization Block. The Send and Receive addresses may be either one or two octets in length according to the EXTA control bit as described above. Frames not matching either address are ignored. Bit RADR in the Receive Message Descriptor (RMD0 <09>)indicates which of the two programmable adresses the frame matched. If address filtering is not used, these fields can just be written as zeroes. For global adresses, the XIDE bit is valid in transparent mode, depending upon the settings of the other bits in the CSR2 Mode Register, as shown in Table 3 below. If bit XIDE (CSR2 register, bit 08) is set to 1, then all frames with address "11111111" are accepted. This is true for both protocol and transparent modes.

Table 2. MK5029 Address Filtering Options

EXTA	EXTAF	XIDE	PROM	DACE	ADDRESS FILTERING
0	0	0	0	0	Single octet filtering S&R (Send & Receive frame addresses)
X	X	X	1	X	No address filtering, all frames accepted
0	0	1	0	0	Single octet filtering S&R and global
0	X	X	X	1	Not allowed
1	0	0	0	0	Double octet filtering S&R per HDLC rules
1	0	0	0	1	Double octet filtering S&R per HDLC rules
1	1	0	0	0	Double octet filtering S&R regardless of A-filed LSB
0	1	X	X	0	Not allowed

NOTES:

1. PROM is CSR2 register bit 10.
2. DACE, EXTA, EXTAF, EXTC, and EXTCF are as defined in the Mode register. X = Do not care.

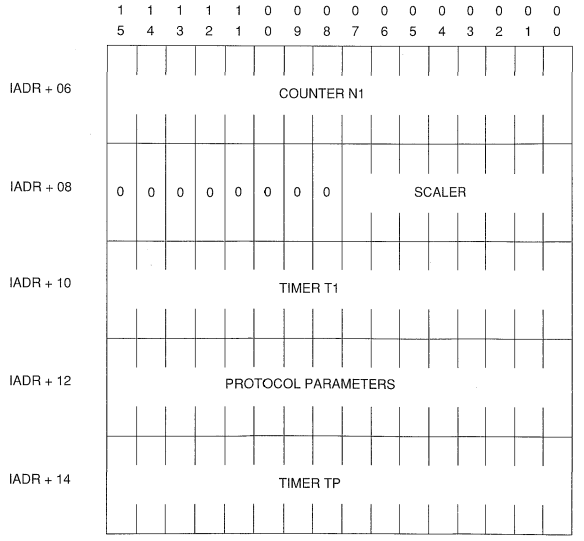
The following table shows the MK5029 address filtering options and the way in which it handles the received Address and Control fields in Transparent Mode.

4.2.4 Timers

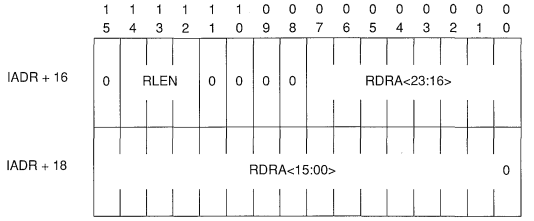
There are 3 independent counter-timers. The lower 8 bits of IADR+08 are used as a scaler for T1 and TP. The scaler is driven by a clock which is 1/32 of SYSCLK. N1 is a 16 bit counter and is used to count the number of bytes in a frame.

The Host will write the period of N1, T1 and TP into the Initialization Block.

TIMER	DESCRIPTION
N1	MAXIMUM FRAME LENGTH. This field must contain the two's complement of one less than the maximum allowable frame length, in bytes. Any frame that exceeds this count will be discarded.
SCALER	TIMER PRESCALER. Timers T1 and TP are scaled by this number. The prescaler is incremented once every 32 system clock pulses. When it reaches zero the timers are incremented and the prescaler is reset. This field s interpreted as the two's complement of the prescaler period. Note: a prescale value of one gives the smallest amount of scaling to the timers (64 clock pulses), zero gives the largest (8224 clock pulses).
T1	GENERAL PURPOSE TIMER. The T1 timer is started by issuing a Timer Start primitive 8, and is stopped by issuing a Timer Stop pimitive 9. A Timer Expiration provider primitive 8 indicates T1 has expired. This field must contain the two's complement of the period of Timer T1.
TP	TRANSMIT POLLING PERIOD. This scaled timer determines the length of time between transmit frame checks. Unless TDMD (see CSR0) is set or a frame is received, no attempt to transmit a frame in the transmit descriptor ring is made until TP expires. At TP expiration all transmit frames in the transmit descriptor ring will be sent. This field must contain the two's complement of the period of Timer T1.



4.2.5 Receive Descriptor Ring Pointer

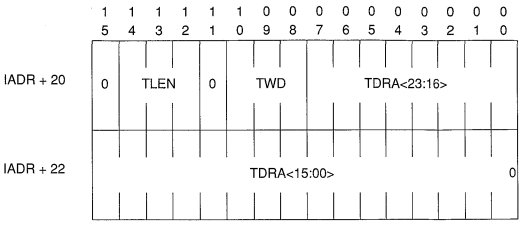


BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	RLEN	RECEIVE RING LENGTH is the number of entries in the Receive Ring expressed as a power of two.

RLEN	NUMBER OF ENTRIES
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

11:08	0	Reserved, must be written as zeroes.
07:00/ 15:00	RDRA	RECEIVE DESCRIPTOR RING ADDRESS isthe base address (lowest address) of the Receive Descriptor Ring. The Receive Descriptor Address must begin on a word boundary.

4.2.6 Transmit Descriptor Ring Pointer



BIT	NAME	DESCRIPTION
15	0	Reserved, must be written as a zero.
14:12	TLEN	TRANSMIT RING LENGTH is the number of entries in the Transmit Ring expressed as a power of two.

TLEN	NUMBER OF ENTRIES	TWD	WINDOW SIZE EXTC = 0	WINDOW SIZE EXTC = 1
0	1	0	NA	1
1	2	1	1	3
2	4	2	2	7
3	8	3	3	15
4	16	4	4	31
5	32	5	5	63
6	64	6	6	127
7	128	7	7	127

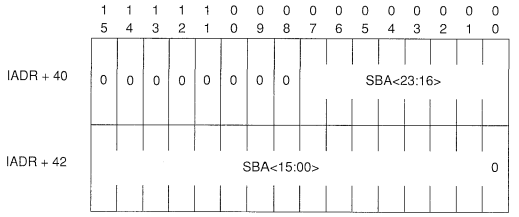
11	0	Reserved, must be written as a zero.
10:08	TWD	TRANSMIT WINDOW is the window size of the Transmitter expressed as a power of two less one. TWD is the maximum number of I frames which may be transmitted without an acknowledgement. TWD is not allowed to be greater than 127.
07:00/ 15:00	TDRA	TRANSMIT DESCRIPTOR RING ADDRESS is the base address (lowest address) of the Transmit Descriptor Ring. The Transmit Descriptor Ring Address must begin on a word boundary.

4.2.7 XID/TEST/CFGR Descriptors

The XID/TEST/CFGR Descriptors contain pointers to the buffers used to receive and transmit XID, TEST, and CFGR frames, as well as buffer lengths. The exact format of these descriptors can be seen in the following Receive and Transmit Message Descriptor Entry descriptions. They are used the same as other descriptors except that no data chaining is allowed (i.e., SLF and ELF must be set to 1).

4.2.8 Status Buffer Address

BIT	NAME	DESCRIPTION
15:08	0	Reserved, must be written as zeroes.
07:00/ 15:00	SBA	STATUS BUFFER ADDRESS points to a 7 word status buffer into which status information is placed upon the issuance of the Status Request primitive by the HOST. The status buffer must begin on a word boundary.



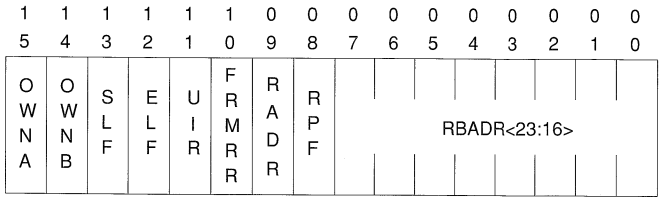
4.2.9 Error Counters Six locations in the Initialization buffer are reserved for use as error counters which the MK5029 will increment. These counters are intended for use by the host CPU for statistical analysis. The MK5029 will only increment the counters; it is up to the user to clear and preset them. The error counters are:

Memory Address	Error Counter
IADR + 44	Bad Frames Received - Bad FCS - Non-Octet Aligned - Aborted Frame
IADR + 46	Number of FRMR frames received.
IADR + 48	Number of FRMR frames transmitted.
IADR + 50	Number of REJ frames received.
IADR + 52	Number of REJ frames transmitted.
IADR + 54	Frames shorter than minimum length received.

4.3 Receive and Transmit Descriptor Rings

Each descriptor ring in memory is a 4 word entry. The following is the format of the receive and transmit descriptors.

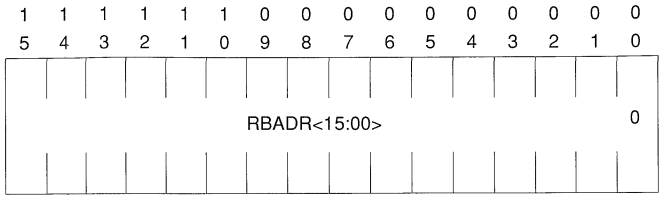
4.3.1 Receive Message Descriptor Entry



4.3.1.1 Receive Message Descriptor 0 (RMD0)

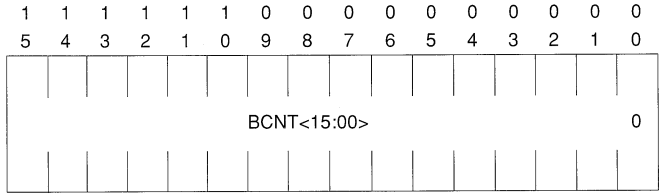
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the I/O ACCELERATION PROCESSOR owns this descriptor. When this bit is a one the MK5029 owns this descriptor. The chip clears the OWNA bit after filling the buffer pointed to by the descriptor entry provided a valid signal unit has been received. The Host sets the OWNA bit after emptying the buffer. Once the MK5029, Host, or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the SLAVE PROCESSOR owns the buffer when OWNA is a zero. The MK5029 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.
13	SLF	Start of Long Frame indicates that this is the first buffer used by MK5029 for this frame. It is used for data chaining buffers. SLF is set by the MK5029. NOTE: A "Long Frame" is any frame which needs data chaining.
12	ELF	End of Long Frame indicates that this the last buffer used by MK5029 for this frame. It is used for data chaining buffers. If both SLF and ELF were set, the frame would fit into one buffer and no data chaining would be required. ELF is set by the MK5029.
11	UIR	UI Received indicates a UI frame has been received and is in this buffer.
10	FRMRR	FRMR Received indicates the I-field of a FRMR is stored in this buffer.
09	RADR	With address filtering enabled, RADR indicates which of the 2 programmable addressses the frame matched. If set, the received address field matched the value in the Receive Frame address field of the Initialization buffer. Otherwise it matched the value in the Send Frame address field.
08	RPF	Valid only for UI, XID, TESTand CFGR frames. RPF equals the state of the P or F bit for the received frame.
07:00	RBADR	The High Order 8 address bits of the buffer pointed to by this descriptor.This field is written by the Host and unchanged by MK5029.

4.3.1.2 Receive Message Descriptor 1 (RMD1)



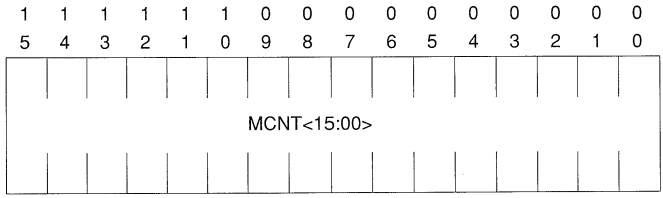
BIT	NAME	DESCRIPTION
15:01	RBADR	The low order 16 address bits of the receive buffer pointed to by this descriptor. RBADR is written by the Host CPU and unchanged by MK5029. The receive buffers must be word aligned.

4.3.1.3 Receive Message Descriptor 2 (RMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the length of the buffer pointed to by this descriptor expressed in two's complement. This field is written to by the Host and unchanged by MK5029. The value of BCNT must be an even number.

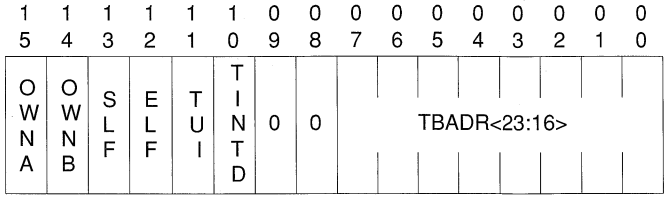
4.3.1.4 Receive Message Descriptor 3 (RMD3)



BBIT	NAME	DESCRIPTION
15:00	MCNT	Message Byte Count is the length, in bytes, of the received signal unit. MCNT is valid only when ELF is set to a one. MCNT is written by MK5029 and read by the Host. If ELF is set to a zero the entire buffer has been utilized and the message byte count is given in BCNT above. The value of this field is expressed in two's complement.

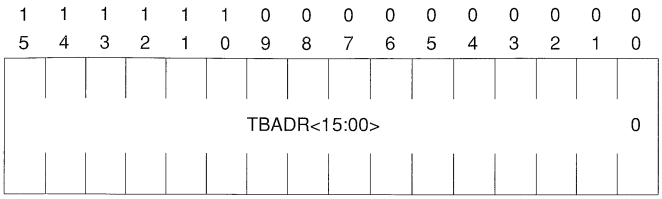
4.3.2 Transmit Message Descriptor Entry

4.3.2.1 Transmit Message Descriptor 0 (TMD0)



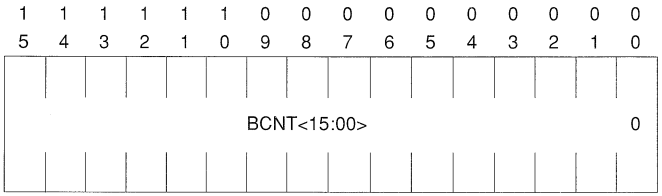
BIT	NAME	DESCRIPTION
15	OWNA	When this bit is a zero either the HOST or the SLAVE PROCESSOR owns this descriptor. When this bit is a one the MK5029 owns this descriptor. The host sets the OWNA bit after filling the buffer pointed to by the descriptor entry. The MK5029 releases the descriptor after transmitting the buffer and receiving the proper acknowledgement from the receiver. After the MK5029, Host,or I/O acceleration processor has relinquished ownership of a buffer, it may not change any field in the four words that comprise the descriptor entry.
14	OWNB	This bit determines whether the HOST or the I /O ACCELERATION PROCESSOR owns the buffer when OWNA is a zero. The MK5029 never uses this bit. This bit is provided to facilitate use of an I/O acceleration processor.
13	SLF	Start of Long Frame indicates that this is the first buffer used by the MK5029 for this frame. It is used for data chaining buffers. SLF is set by the Host. When not chaining, SLF should be set to a one. NOTE: A "Long Frame" is any frame which needs data chaining.
12	ELF	End of Long Frame indicates that this is the last buffer used by the MK5029 for this frame. It is used for data chaining buffers. If both SLF and ELF were set the frame would fit into one buffer and no data chaining would be required. ELF is set by the Host. When not chaining, ELF should be set to a one.
11	TUI	Transmit a UI frame indicates that a UI frame is to be transmitted from the transmit buffer instead of a normal I frame. This bit must be set for anything transmitted in Transparent Mode.
10	TINTD	Transmit Interrupt Disable. If this bit is set, no transmit interrupt is generated when ownership of this descriptor is released back to the host.
09:08	0	Reserved, must be written as zeroes.
07:00	TBADR	The High Order 8 address bits of the buffer pointed to by this descriptor. This field is written by the Host and unchanged by MK5029.

4.3.2.2 Transmit Message Descriptor 1 (TMD1)



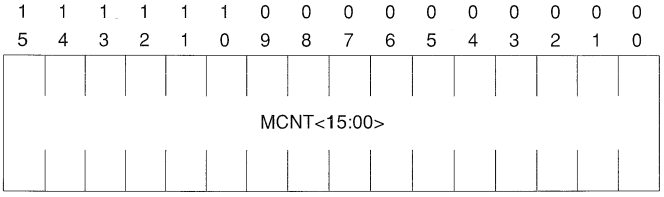
BIT	NAME	DESCRIPTION
15:00	TBADR	The Low Order 16 address bits of the buffer pointed to by this descriptor. TBADR is written by the Host and unchanged by MK5029. The least significant bit is zero since the descriptor must be word aligned.

4.3.2.3 Transmit Message Descriptor 2 (TMD2)



BIT	NAME	DESCRIPTION
15:00	BCNT	Buffer Byte Count is the usable length of the buffer pointed to by this descriptor expressed in two's complement. This field is not used by the MK5029.

4.3.2.4 Transmit Message Descriptor 3 (TMD3)

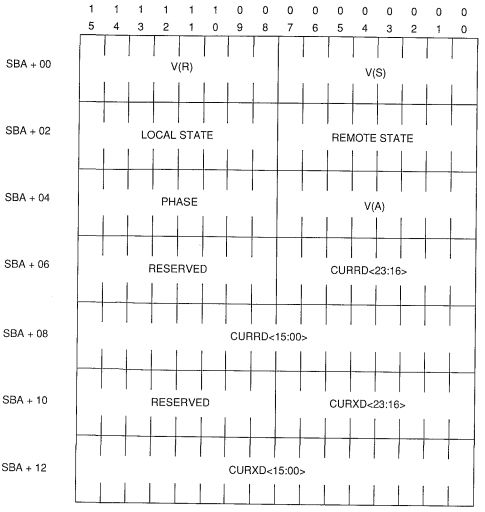


BIT	NAME	DESCRIPTION
15:00	MCNT	Message byte count is the length, in octets, of the data contained in the corresponding buffer. The value of this field is expressed in two's complement.

4.3.3 Status Buffer

FIELD	DESCRIPTION
V(R)	Current value of the Receive Count Variable. $0 \leq V(R) \leq 7$ ($0 \leq V(R) \leq 127$ for extended control).
V(S)	Current value of the Transmit Count Variable. $0 \leq V(S) \leq 7$ ($0 \leq V(S) \leq 127$ for extended control).
V(A)	Current value of Transmit Acknowledge Count. This field contains the value of the N(r) of the most recently received S or I frame. The modulo difference between V(A) and V(s) determines the number of outstanding I frames that have not been acknowledged by the remote station.
LOCAL STATE	Indicates the current state of operation for the local (secondary) station. 0: Normal Data Transfer State 1: Local Busy State 2: REJ Sent State 4: Normal Disconnected State 6: FRMR Sent State
REMOTE STATE	Indicates the current state of operation for the remote (primary)station. 0: Remote Not Busy 1: Remote Busy
PHASE	Indicates the current phase of operation for the local (secondary)station. -1: Stopped, TD is held at 1's, RD is ignored 0: Normal Response Mode 1: Normal Disconnected Mode, TD transmits flags 2: Initialization Mode (IM) 3: Transparent (Flexible) Mode
CURRD: <23:00>	Current Receive Descriptor. This pointer indicates the position of the discriptor for the next receive buffer to be filled.
CURXD: <23:00>	Current Transmit Descriptor. This pointer indicates the position of the discriptor for the next transmit buffer to be transmitted.

4.4 Detailed Programming Procedures



4.4.1 Initialization (Reading of Initialization Block)

The following procedure should be followed to initialize the MK5029:

1. Setup bus control information in CSR4.
2. Setup the Initialization Block and Desciptor Rings.
3. Load the address of the initialization block information into CSR's 2 and 3.
4. Issue the INIT primitive through CSR1 (write 4200H to CSR1) instructing the MK5029 to read the initialization block pointed to by CSR's 2 and 3.
5. Wait for the INIT confirmation primitive (CSR1 = 0242H) from the MK5029.
   Then clear the PAV bit in CSR1 (write 0040H to CSR1).
6. Issue the Start primitive through CSR1 (write 4300H to CSR1).
   Flags will now be continously transmitted.
7. Enable interrupts in CSR0 if desired.

4.4.2 Initialization Mode

1. Wait for IM Indication primitive from the MK5029.
2. If IM Indication primitive is received, issue a SIM Response primitive to indicate willingness to initialize the secondary station. If IM Confirmation primitive is issued by the MK5029, then the device is in Initialization Mode.
3. If no IM Indication primitive is received, the primary station is not trying to initialize the secondary station

4.4.3 Link Setup

The following procedure should be followed for establishing a link.

1. Wait for a Connect Indication primitive from the MK5029.
2. If a Connect Indication primitive is received (indicating SNRM frame has been received), issue a Connect Response primitive to indicate willingness to establish the link (causes MK5029 to respond with a UA frame). The link is now established.
3. If no Connect Indication primitive is received, the primary station is not trying to establish a link with the secondary station.

4.4.4 Refusing Link Setup

The following procedure should be followed when refusing link establishment.

1. A Connect Indication primitive will be received indicating a request by the primary station to establish the link
2. Issue a Disconnect Request primitive to refuse to establish the link (causes MK5029 to respond with a DM frame at the next poll opportunity).

4.4.5 Sending Data

Use the following procedure to send a frame:

1. Wait for the OWNA bit of the current transmit descriptor to be cleared, if it is not already.
2. Fill the buffer associated with the current transmit descriptor with the data to be sent, or set the descriptor buffer address to any already filled buffer.
3. Repeat steps 1 and 2 for the next buffer if chaining is necessary, setting SLF, ELF and MCNT appropriately.
4. Set the OWNA bit for each descriptor used.
5. Go on to next descriptor. These OWNA bits will be cleared when the data has been sent successfully and acknowledged. In Transparent Mode, OWNA bits are cleared immediately after frame transmission.

4.4.6 Receiving Data

The following procedure should be followed when receiving a frame:

1. Make sure the OWNA bit of the current receive descriptor is clear.
2. Read data out of the buffer associated with the current receive descriptor.
3. Set the OWNA bit of the current receive descriptor.

4. If the ELF bit of the current receive descriptor is clear, then go on to the next descriptor and repeat the above steps appending data from each buffer until a descriptor with the ELF bit set is reached.

4.4.7 Link Disconnect

The following procedure should be followed to disconnect an established link.

1. Issue the Disconnect Request primitive to the MK5029.
2. The MK5029 will go into Normal Disconnected state and sends a DM frame at its next poll opportunity.

4.4.8 Disabling the MK5029

The following procedure should be followed to disable the MK5029:

1. Issue the STOP primitive through CSR1. This will disable the MK5029 from receiving or transmitting. The TD pin will be held high while the MK5029 is in the Stopped mode. The STOP bit in CSR0 will be set and interrupts will be disabled.
   If reception or transmission of a frame is in progress, then received data may be lost, and the transmitted frame will be aborted.

4.4.9 Re-enabling the MK5029

The same procedure should be followed for re-enabling the MK5029 as was used to initalize upon power up. If the Initialization Block and the hardware configuration have not changed, then steps 1,2,3, 4 and 5 of the intialization sequence may be omitted.

4.4.10 Receiving Link Reset

The following procedure should be followed when receiving a request for link reset:

1. A Reset Indication primitive will be received from the MK5029 indicating the primary station has requested a resetting of the link.
2. If able to reset, issue a Reset Response primitive to indicate willingness to reset the link.
3. If unable to reset, issue a Disconnect Request to disconnect the link.

4.4.11 Receiving XID/TEST/CFGR Frames

The following procedure should be performed when receiving XID/TEST/CFGR frame:

1. A XID/TEST/CFGR Indication primitive will be received from the MK5029 to indicate the reception of a XID, TEST, or CFGR frame. The information field of the received XID, TEST, or CFGR frame will be located in the XID/TEST/CFGR receive buffer.
2. To respond, place the appropriate information in the XID/TEST/CFGR transmit buffer and issue a XID/TEST/CFGR Response Primitive. This frame will be transmitted at the next poll opportunity.
3. To refuse, issue a Disconnect Reques primitive.

Note: A XID/TEST/CFGR Indication primitive will only be issued if the corresponding XIDE/TESTE/CFGRE bit is set in either the CSR2 or the Protocol Parameters Register. Otherwise all XID/TEST/CFGR frames will automatically be refused and not recognized.

4.4.12 MK5029 Internal Self Test

The MK5029 contains an easy to use internal self test designed to test, with a high fault coverage, all of the major blocks of the device except the DMA controller. It is suggested that a loopback test also be performed to more completely test the DMA controller.

The following procedure should be followed to execute the internal self test:

1. Reset the device using the $\overline{\text{RESET}}$ pin.
2. Set bit 04 of CSR4.
3. Issue a Self Test Request through CSR1.
4. Poll CSR1, waiting for the PAV bit in CSR1 to be set by the MK5029.
5. After the PAV bit is set, read CSR1. The success or failure of the test is indicated in the PPRIM field as follows:

PPRIM	RESULT
00	Passed self test.
17 (11H)	Failed the reset test of the self test.
18 (12H)	Failed the self test in the micro controller RAM.
19 (13H)	Failed the self test in the ALU.
20 (14H)	Failed the self test in the timers.
21 (15H)	Failed the self test in the transmitter and/or receiver.
22 (16H)	Failed the self test in the CSR's and/or bus master.
Otherwise	Failed device.

6. If the PAV bit is not set within 75 msec (SYSCLK = 10MHZ), then the MK5029 is unable to respond to the Self Test Request and will not complete successfully.

If the self test passes, then it may be immediately re-executed from step 3, otherwise re-execution should proceed from step 1.

SECTION 5: ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS –25 °C to + 100 °C

Temperature Under Bias . . . . . –65 °C to + 150 °C

Storage Temperature . . . . . –65 °C to + 150 °C

Voltage on Any Pin with Respect to Ground . . . . . –0.5 V to V_{CC} + 0.5 V

Power Dissipation . . . . . 0.50 W

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the above device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

Symbol	Conditions	Min.	Typ.	Max.	Units
V_{IL}		–0.5		+0.8	V
V_{IH}		+2.0		V_{CC}+0.5	V
V_{OL}	@ I_{OL} = 3.2 mA			+0.5	V
V_{OH}	@ I_{OH} = –0.4 mA	+2.4			V
I_{IL}	@ V_{IN} = 0.4 to V_{IN} = 0.4 to V_{CC}			±	µA
I_{CC}	@ T_{SCT} = 100 ns		50		mA

CAPACITANCE

F = 1 MHz

Symbol	Parameter	Min.	Max.	Units
C_{IN}	Capacitance on Inputs pins		10	pf
C_{OUT}	Capacitance on Output Pins		10	pf
C_{IO}	Capacitance on I/O pins		20	pf

AC TIMING SPECIFICATIONS

T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
1	SYSCLK	T_{SCT}	SYSCLK period		100		2000
2	SYSCLK	T_{SCL}	SYSCLK low time		45		
3	SYSCLK	T_{SCH}	SYSCLK high time		45		
4	SYSCLK		Rise time of SYSCLK		0		8
5	SYSCLK	T_{SCF}	Fall time of SYSCLK		0		8
6	$\overline{TCLK}$	T_{TCT}	$\overline{TCLK}$ period		140		
7	$\overline{TCLK}$	T_{TCL}	$\overline{TCLK}$ low time		63		
8	TCLK	T_{TCH}	$\overline{TCLK}$ high time		63		
9	$\overline{TCLK}$	T_{TCR}	Rise time of $\overline{TCLK}$	CL = 50 pF	0		8
10	$\overline{TCLK}$	T_{TCF}	Fall time of $\overline{TCLK}$		0		8
11	TD	T_{TDP}	TD data propagation delay after the falling edge of $\overline{TCLK}$	CL = 50 pF			40
12	TD	T_{TDH}	TD data hold time after the falling edge of $\overline{TCLK}$		5		
13	$\overline{RCLK}$	T_{RCT}	$\overline{RCLK}$ period		140		

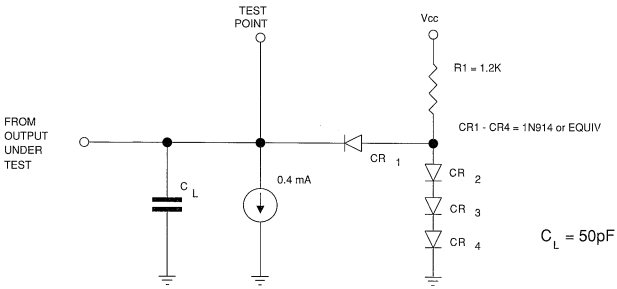
AC TIMING SPECIFICATIONS (Continued)
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
14	$\overline{RCLK}$	T_{RCH}	$\overline{RCLK}$ high time		63		
15	$\overline{RCLK}$	T_{RCL}	$\overline{RCLK}$ low time		63		
16	$\overline{RCLK}$	T_{RCR}	Rise time of $\overline{RCLK}$		0		8
17	$\overline{RCLK}$	T_{RCF}	Fall time of $\overline{RCLK}$		0		8
18	RD	T_{RDR}	RD data rise time		0		8
19	RD	T_{RDF}	RD data fall time		0		8
20	RD	T_{RDH}	RD hold time after rising edge of $\overline{RCLK}$		5		
21	RD	T_{RDS}	RD setup time prior to rising edge of $\overline{RCLK}$		30		
22	A/DAL	T_{DOFF}	Bus Master driver disable after rising edge of $\overline{HOLD}$		0		50
23	A/DAL	T_{DON}	Bus Master driver enable after falling edge of $\overline{HLDA}$	TSCT = 100 ns	0		200
24	$\overline{HLDA}$	T_{HHA}	Delay to falling edge of $\overline{HLDA}$ from falling edge of $\overline{HOLD}$ (Bus Master)		0		
25	$\overline{RESET}$	T_{RW}	$\overline{RESET}$ pulse width		30		
26	A/DAL	T_{CYCLE}	Read/write, address/data cycle time	TSCT = 100 ns	600		
27	A	T_{XAS}	Address setup time to falling edge of ALE		100		
28	A	T_{XAH}	Address hold time after the rising edge of $\overline{DAS}$		50		
29	DAL	T_{AS}	Address setup time to the falling edge of ALE		75		
30	DAL	T_{AH}	Address hold time after the falling edge of ALE		20		
31	DAL	T_{RDAS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus Master read)		55		
32	DAL	T_{RDAH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus Master read)		0		
33	DAL	T_{DDAS}	Data setup time to the falling edge of $\overline{DAS}$(Bus Master write)		0		
34	DAL	T_{WDS}	Data setup time to the rising edge of $\overline{DAS}$ (Bus Master write)		250		
35	DAL	T_{WDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus Master write)		35		
36	DAL	T_{SRDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave read)	TSCT = 100 ns	0		35
37	DAL	T_{SWDH}	Data hold time after the rising edge of $\overline{DAS}$ (Bus slave write)		0		
38	DAL	T_{SWDS}	Data setup time to the falling edge of $\overline{DAS}$ (Bus slave write)		0		
39	ALE	T_{ALEW}	ALE width high		110		
40	ALE	T_{DALE}	Delay from rising edge of $\overline{DAS}$ to the rising edge of ALE		70		
41	$\overline{DAS}$	T_{DSW}	$\overline{DAS}$ width low		200		
42	$\overline{DAS}$	T_{ADAS}	Delay from the falling edge of ALE to the falling edge of $\overline{DAS}$		80		

AC TIMING SPECIFICATIONS (Continued)
T_A = 0 °C to 70 °C, V_{CC} = +5 V ±5 percent, unless otherwise specified.

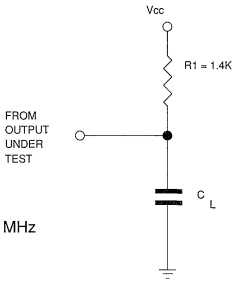
No.	Signal	Symbol	Parameter	Test Conditions	Min. (ns)	Typ. (ns)	Max. (ns)
43	$\overline{DAS}$	T_{RIDF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DAS}$ (Bus Master read)		35		
44	$\overline{DAS}$	T_{RDYS}	Delay from the falling edge of $\overline{READY}$ to the rising edge of $\overline{DAS}$	T_{ARYD} = 300 ns T_{SCT} = 100 ns	120		250
45	$\overline{DALI}$	T_{ROIF}	Delay from the rising edge of $\overline{DALO}$ to the falling edge of $\overline{DALI}$ (Bus Master read)		70		
46	$\overline{DALI}$	T_{RIS}	$\overline{DALI}$ setup time to the rising edge of $\overline{DAS}$ (Bus Master read)		150		
47	$\overline{DALI}$	T_{RIH}	$\overline{DALI}$ hold time after the rising edge of $\overline{DAS}$ (Bus Master read)		0		
48	$\overline{DALI}$	T_{RIOF}	Delay from the rising edge of $\overline{DALI}$ to the falling edge of $\overline{DALO}$ (Bus Master read)		70		
49	$\overline{DALO}$	T_{OS}	$\overline{DALO}$ setup time to the falling edge of ALE (Bus Master read)		110		
50	$\overline{DALO}$	T_{ROH}	$\overline{DALO}$ hold time after the falling edge of ALE (Bus Master read)		35		
51	$\overline{DALO}$	T_{WDSI}	Delay from the rising edge of $\overline{DAS}$ to the rising edge of $\overline{DALO}$ (Bus Master write)		50		
52	$\overline{CS}$	T_{CSH}	$\overline{CS}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
53	$\overline{CS}$	T_{CSS}	$\overline{CS}$ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
54	ADR	T_{SAH}	ADR hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
55	ADR	T_{SAS}	ADR setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
56	$\overline{READY}$	T_{ARYD}	Delay from the falling edge of ALE to the falling edge of $\overline{READY}$ to insure a minimum bus cycle time (600nS)	T_{SCT} = 100 ns			150
57	$\overline{READY}$	T_{SRDS}	Data setup time to the falling edge of $\overline{READY}$ (Bus slave read)		75		
58	$\overline{READY}$	T_{RDYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus Master)		0		
59	$\overline{READY}$	T_{SRYH}	$\overline{READY}$ hold time after the rising edge of $\overline{DAS}$ (Bus slave)	T_{SCT} = 100 ns			35
60	$\overline{READY}$	T_{RSH}	READ hold time after the rising edge of $\overline{DAS}$ (Bus slave)		0		
61	READ	T_{SRS}	READ setup time to the falling edge of $\overline{DAS}$ (Bus slave)		0		
62	$\overline{READY}$	T_{RDYD}	Delay from falling edge of $\overline{DAS}$ to falling edge of $\overline{READY}$ (Bus slave)	TSCT = 100 ns		200	

Figure 5a: TTL Output Load Diagram



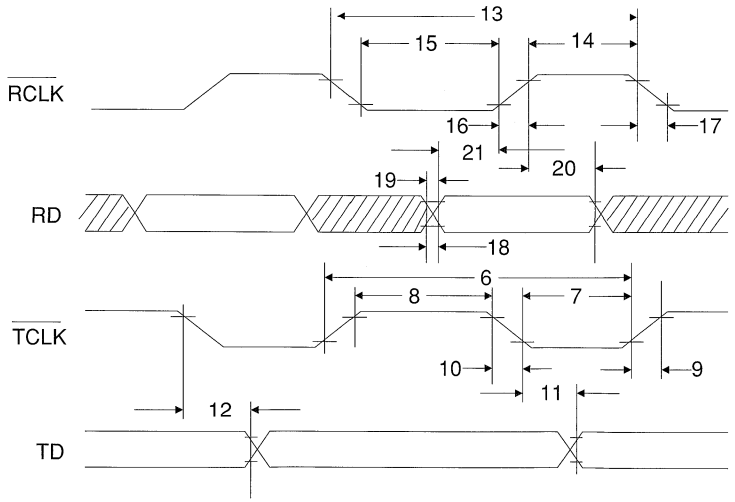
NOTE: This load is used on all outputs except INTR, HOLD, READY.

Figure 5B: Open Drain Output Load Diagram



NOTE: This load is used on open drain outputs INTR, HOLD, READY.

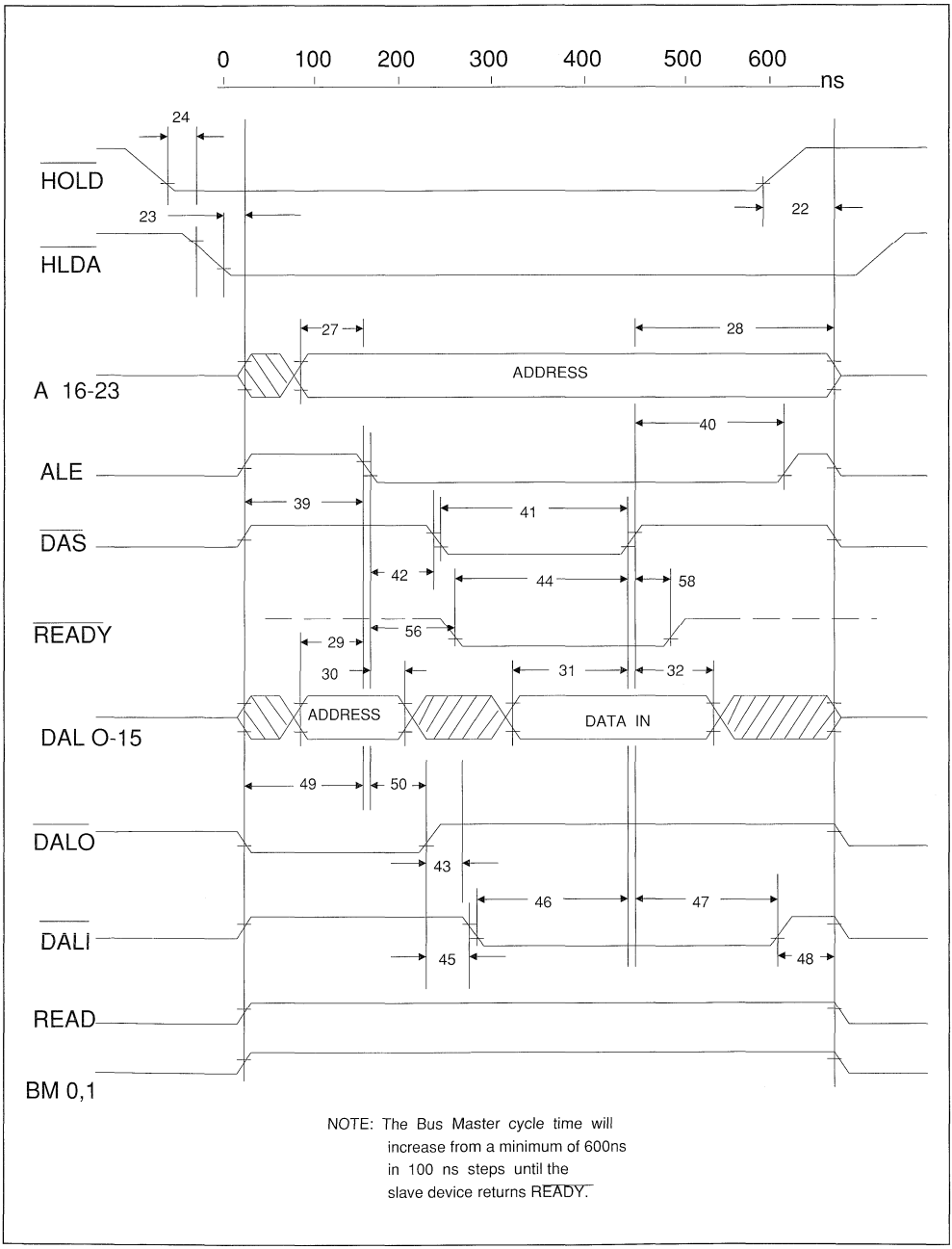
Figure 6: MK5029 Serial Link Timing Diagram



TIMING MEASUREMENTS ARE MADE AT THE FOLLOWING VOLTAGES, UNLESS OTHERWISE SPECIFIED:

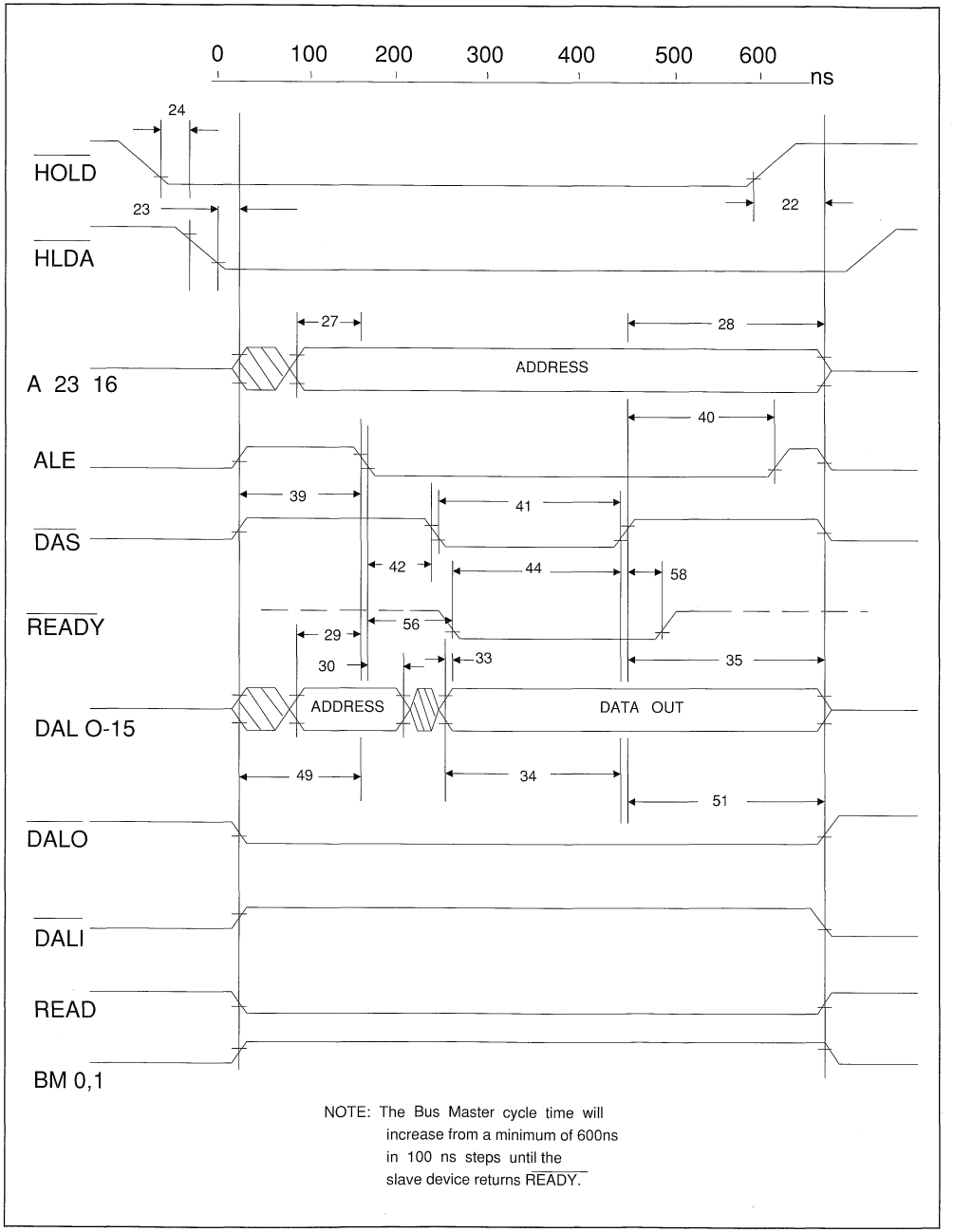
	"1"	"0"
OUTPUT	2.0 V	0.8 V
INPUT	2.0 V	0.8 V
FLOAT	10 %	90 %

Figure 7: MK5029 Bus Master Timing Diagram (Read)



NOTE: The Bus Master cycle time will increase from a minimum of 600ns in 100 ns steps until the slave device returns READY.

Figure 8: MK5029 Bus Master Timing Diagram (Write)



NOTE: The Bus Master cycle time will increase from a minimum of 600ns in 100 ns steps until the slave device returns $\overline{\text{READY}}$.

Figure 9: MK5029 Bus Slave Timing Diagram (Read)

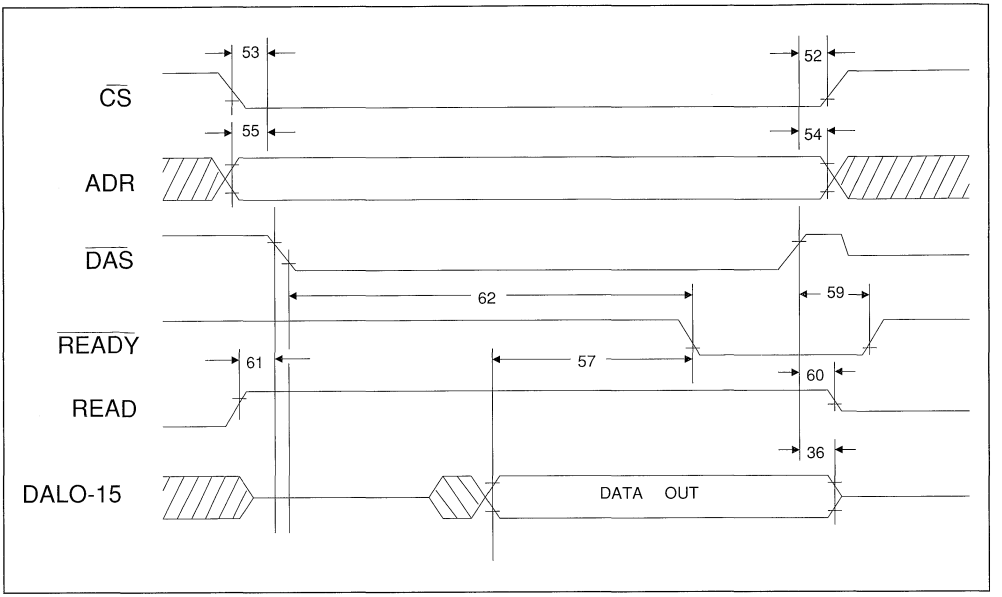
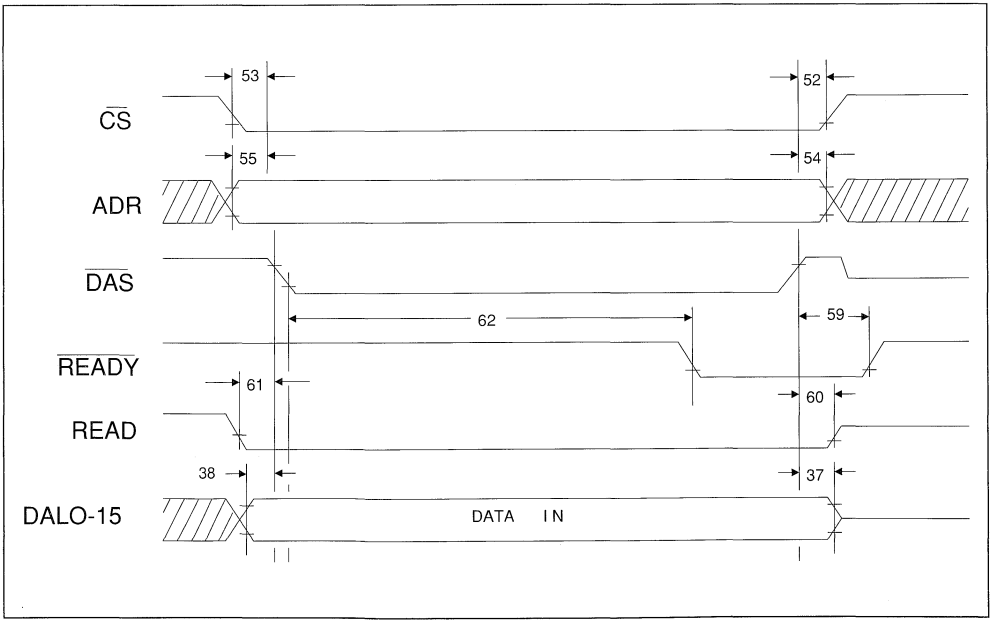


Figure 10: MK5029 Bus Slave Timing Diagram (Write)



APPLICATION NOTES

MK5025 SINGLE CHANNEL LAPD

INTRODUCTION

The SGS-Thomson X.25 Link Level Controller (MK5025) is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID frames) and X.75 as well as single channel LAPD (Link Access Procedure on the D-channel) for ISDN with its extended addressing capabilities and UI (Unnumbered Information) frames for TEI assignment.

One of the outstanding features of the MK5025 is its buffer managment which includes on-chip DMA. This feature allows users to handle multiple frames of receive and transmit data at a time. In order to utilize these buffer managment and DMA features with protocols not directly supported by the MK5025, a transparent mode is also available for customized protocols using HDLC framing.

PURPOSE

LAPD is a protocol operating at the data link layer, whose purpose is to convey information between layer 3 entities across the ISDN user-network interface using the D-channel. For further information on LAPD please consult CCITT Recommendations Q.920 and Q.921. The purpose of this application brief is to provide a detailed description for using the MK5025 in single channel LAPD applications. Please refer to the MK5025 Technical Manual for more detailed information concerning the overall operation of the MK5025.

USE OF MK5025 FOR LAPD VS LAPB

Since X.25 LAPB and LAPD are very similar, the operation of the MK5025 is very similar for both protocols. Differences include implementation of the T203 timer and support of UI frames for TEI assignment. However, the main difference between the two standards is in level 2 addressing of the frames.

The frame structure supported by the MK5025 conforms to HDLC rules and is as follows:

F	A	C	I	FCS	F

where:
F = Flag
A = Address field (A-field)
C = Control field (C-field)
I = Information field
FCS = Frame Check Sequence

For LAPD the Address field contains the SAPI and TEI in the following format.

0	C/R	SAPI	1	TEI

where:
C/R = Command/Response bit
SAPI = Service Access Point Identifier
TEI = Terminal Endpoint Identifier

The values for SAPI and TEI should be the same for both the Local and Remote Address fields, located in the MK5025 Initialization Block. The only difference between these fields will be in the setting of the C/R bit. According to CCITT Q.921, the setting of the C/R bit should be as follows:

	C/R Value	
	Network Side	User Side
Commands from	1	0
Responses to	1	0
Commands to	0	1
Responses from	0	1

The MK5025 sends commands with the Remote address in the A-field of the frame, and it sends responses with the Local address in the A-field of the frame. The setting of the Local and Remote address fields is dependent upon whether the MK5025 is used in the NT (Network side) or the TE (Terminal Equipment - user side), as shown in Figure 1.

CONTROL AND STATUS REGISTER OPERATION

For LAPD all the control and status register mechanisms still function the same, but there are some bits that pertain typically to LAPD. These are bits 09, 12, and 13 of CSR2.

CSR2<09> - UIE - This bit should be set to enable the recognition of UI frames, which are used for TEI assignment in LAPD.

CSR2<12> - T203E- This bit should be set to enable the MK5025 T3 timer to behave as specified for LAPD T203 timer. The difference between T3 and T203 is that T3 determines the amount of link idle (all "1's") time necessary to consider the link disconnected, while T203 determines the maximum amount of time allowed without frames being exhanged.

CSR2<13> - FRMRD - Setting this bit to a one

will disable the sending of FRMR frames in response to the conditions described in section 3.6.1 or 3.6.11 (items b, c, and d) of CCITT Q.921 (Blue Book). The MK5025 will issue an Error Indication primitive and allow for the re-establishment of the link rather than establishing a frame rejection condition. Setting of this bit allows compliance with CCITT Q.921 (Blue Book) section 5.8.5 which basically states that upon occurence of a frame rejection condition the data link layer entity shall initiate re-establishment of the link.

DESCRIPTOR RING OPERATION

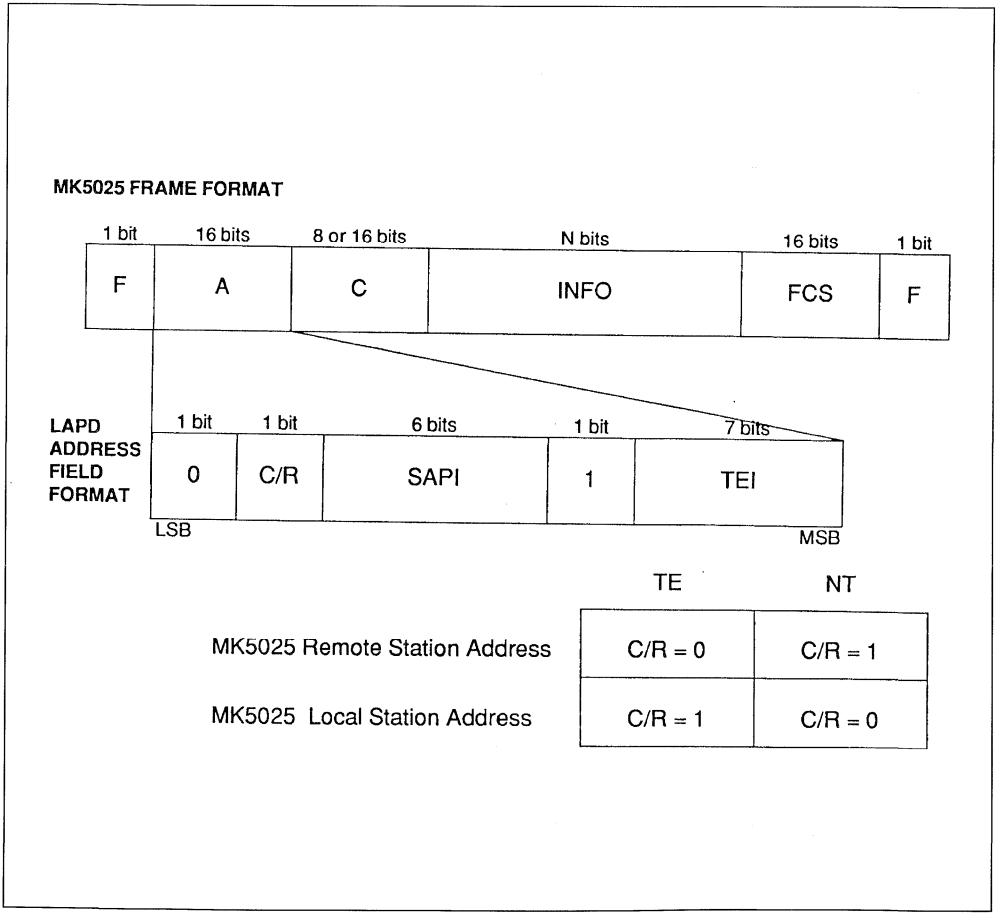
The buffer management and descriptor ring operation is the same for LAPD as for X.25 LAPB applications. It should be noted however that for the Transmit Message Descriptor, TUI (bit 11 of TMD0) should be set to 1 in order to transmit UI frames for TEI assignment.

In LAPD as in LAPB, the Transmit Window size (TWD) in the Transmit Descriptor Ring Pointer must be set to a value greater than 0 for any transmission to occur, if EXTC(bit 07 of Mode Register) = 0 .. In fact, if TWD=0 the MK5025 will not poll the Transmit Descriptor Ring.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, X.32, X.75, and LAPD for ISDN, while still allowing the flexibility of implementing alternate or customized HDLC based protocols using the MK5025's transparent mode.

Figure 1: MK5025 Addressing for LAPD



MK5025 NET 2 CONFORMANCE

INTRODUCTION

The MK5025 is a CMOS VLSI Link Level Controller which provides complete link level data communication control conforming to CCITT recommendation X.25. It also has additional features which allow it to support LAPD as well as X.32 and X.75. The MK5025 is currently in use in systems which have met conformance testing for Telenet, Tymenet, Datex-P, Iberpac, and DDN/DCA certification as well as approval for LAPD connection to AT&T and Norther Telecom ISDN. Most recently the MK5025 has undergone testing for conformance to NET 2.

NET 2 is a European technical recommendation that details the requirements (and interface tests for conformance to those requirements) of packet mode DTEs to dedicated circuit interfaces of X.25 public packet switched data networks (PSPDN). As of 30 June 1990, NET 2 became the applicable standard for X.25 interface in the majority of European countries.

PURPOSE

The current MK5025 can be implemented to meet the NET 2 requirements. The majority of the NET 2 tests can be met by the MK5025 using the standard LAPB operation and standard set of primitives. There are however some NET 2 tests that require the use of some options that were added to the revision C02 of the MK5025 which is the current production version. The purpose of this applications note is to list those tests and how they can be met using the MK5025.

NET 2 TESTS

The majority of NET 2 tests can be met by the MK5025 with very little intervention from the host other than the initial setup of MK5025 registers and memory data structures, reception and issuing of primitives for link set-up or disconnect, and transmission and reception of required I frames. There are however some tests that require intervention by the host to determine what action to take in the case of certain error conditions.

The following NET 2 tests are those that may require host interverntion and use of special features of the MK5025.

Test 9.1.4 DTE Initiated DISC Start

According to CCITT X.25, a DTE shall initiate link setup by polling with SABM/E, and the MK5025 does this in response to a Connect Request primitive issued by the host. However, once a Start primitive (writing 4100H to CSR1) has been issued to the MK5025, polling with DISC can be accomplished using another Start primitive, but with UPARM=1 (5100H to CSR1), immediately followed by a Disconnect Request primitive (4E00 to CSR1). Then, following the reception of a Disconnect Confirmation provider primitive, a Connect Request primitive can be issued by the host to complete the remainder of the test (requiring the standard transmission of SABM/E).

Test 9.5 Incorrect FCS

The MK5025 will ignore frames with bad FCS regardless of their content, even if they are greater in length than N1. The MK5025 will also ignore frames with bad FCS that cross multiple buffer boundaries. However, if the length of the frame exceeds N1 and crosses one more buffer boundary, the MK5025 will then generate a FRMR with Y=1 (indicating receipt of a frame that exceeds N1), regardless of good or bad FCS. The reason for this is that if the MK5025 were to continue to allow reception of an excessively large frame into additional multiple buffers once the frame length exceeds N1, all available memory could be consumed by the frame without yet receiving the FCS to determine if it be good or bad.

NET 2 test 9.5.4 does not specify how much longer the "Extra long frame with incorrect FCS" can be beyond N1. To conform this test, when data chaining is used, the buffer size should be slightly smaller than an integer division of N1, so that when a frame exceeds N1 it will have a large amount of one buffer remaining (so as not to cross a buffer boundary after exceeding

N1, which would cause transmission of FRMR). If chaining is not desired then the buffer size should be sufficiently larger than N1 to accomodate the reception of the entire "extra long frame" in one buffer.

Test 9.11 Miscellaneous Tests

The test conditions in tests 9.11.2 and 9.11.3 cause the MK5025 to go into the Error Indication state. From this state the MK5025 Technical Manual recommends issuing either a Reset Request primitive (which will initiate link set-up by sending SABM/E) or a Disconnect Request primitive (which will initiated link disconnection by sending a DISC).

In the Error Indication state the MK5025 will ignore the reception of any frames other than SABM/E or DISC. NET 2 tests 9.11.2 & 3 imply that the unit under test go directly into disconnected phase upon receiving a DM or FRMR while in information transfer phase. To acomplish this the host must, in response to an Error Indication primitive, issue a Stop primitive immediately followed by a Start primitive and then, if necessary, a Disconnect Request primitive to cause the MK5025 to send a DM (the alternate reaction for test 9.11.3). [Please note that this same reaction to Error Indication should be used in tests 9.7 if it is necessary to send the alternate reaction of DM/F=0 rather than SABM/P=1].

CONCLUSION

Since the MK5025 is a Link Level controller, the Packet Level must be implemented in software and written to meet the packet level requirements of NET 2. However, using the techniques mentioned in this app brief, the MK5025 can be used to meet the Link Level requirements of NET 2 and applicable annexes.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 DAISY CHAIN DMA

INTRODUCTION

The SGS-Thomson MK5025 X.25 Link Level Controller is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

PURPOSE

Although the MK5025 Data Sheet and Technical Manual provide detailed timing diagrams that specifiy the relationships of the host interface signals to one another for the sole requestor DMA configuration, the designer may find it helpful to know the timing for the MK5025 as an element in a DMA daisy chain. The purpose of this application brief is to provide a description of the MK5025 host interface in a daisy chain configuration, and some suggestions on how to implement the daisy chain.

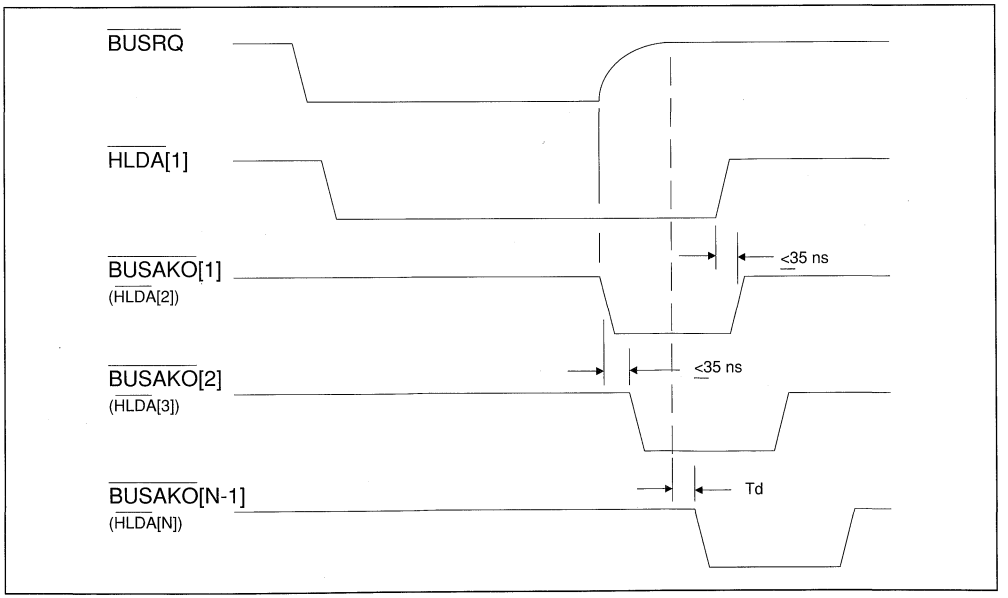
It should be also be noted that although the timing diagrams in this document are provided to facilitate the design process, the timing requirements in the Data Sheet must still be met to ensure proper operation.

DAISY CHAIN OPERATION

The daisy chain operation of the MK5025 is selected by setting the BCON bit of CSR4 so that pins 15, 16, and 17 are redefined as BYTE, BUSAKO, and BUSRQ respectively.

In the daisy chain mode the MK5025 DMA operation is still the same in that it still requests the bus by asserting HOLD/BUSRQ (pin 17), but it will not do so unless both BUSRQ and HLDA are inactive (de-asserted). Also, the granting of the bus to the MK5025 should still consist of asserting HLDA (pin 19) as indicated in the timing diagrams in the Technical Manual. However, if the MK5025 receives HLDA when it is not requesting the bus, the BUSAKO output (pin 16) will be driven low.

Figure 1: Daisy Chain Bus Master Timing



Additionally, if HLDA is still asserted after BUSRQ is deasserted by the MK5025, then the BUSAKO output will be driven low until HLDA is deasserted. Figure 1 provides the typical timing relationships for this mode of operation.

As can be seen in this diagram, there is a possibility of the BUSAKO output being asserted at the end of a DMA cycle from the time BUSRQ is deasserted until HLDA is deasserted. This pulse will not cause any problems unless it is delayed (by propagating through a large daisy chain) such that Td (shown in Figure 1) is sufficiently long to allow an oportunity to request the bus and see this pulse as a HLDA acknowledging the bus request.

SUGGESTED DAISY CHAIN CONFIGURATION

In order to resolve the possibility of a problem resulting from the propagation of the end of DMA cycle BUSAKO pulse, it is suggested that a daisy chain arragement such as that shown in Figure 2 or 3 be used for daisy chains of more than 2 MK5025 devices. In the arrangement shown in Figure 2, a latch is added to the end of the daisy chain for the purpose of latching BUSRQ low (asserted) until BUSAKO has propagated through the daisy chain. In this manner another MK5025 will not request the bus until BUSAKO has propagated through the entire chain, resetting the latch and allowing BUSRQ to go inactive. It should be noted that the output of the latch drives the enable of a tri-statable inverter to avoid contention on BUSRQ.

The solution suggested in Figure 2 could of course also be implemented with a PLD device such as an SGS-THOMSON GAL 20V8. The PLD device should be programmed such that it

Figure 2: Suggested Daisy Chain Configuration

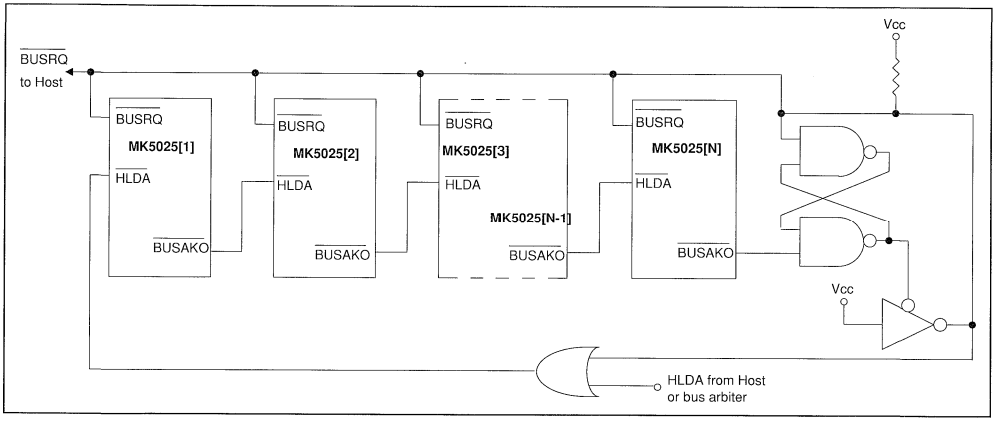
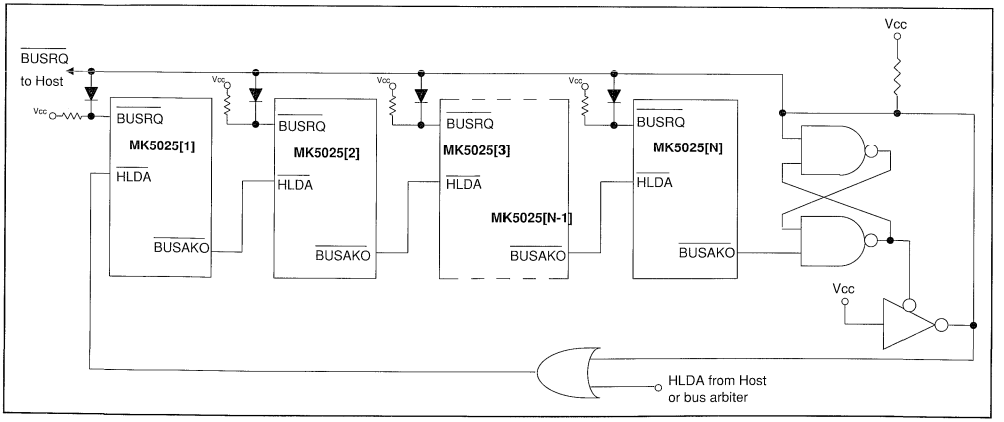


Figure 3: Round-Robin Daisy Chain Configuration



implements the following set of conditions:

IF $\overline{\text{BUSRQ}}$=0
LATCH BUSRQ=0 AND $\overline{\text{HLDA}}$=0
IF $\overline{\text{BUSAKO}}$[N]=0
RELEASE $\overline{\text{BUSRQ}}$

where $\overline{\text{BUSAKO}}$[N] is from the last device in the daisy chain.

With this configuration the bus will typically be relenquished by the daisy chain in between each MK5025 bus master cycle or burst. The exception to this is when two or more MK5025 devices request the bus simultaneously, in which case the devices would each obtain the bus in order of priority as bus acknowledgement (HLDA to $\overline{\text{BUSAKO}}$) propagates through the daisy chain.

A variation to the suggested daisy chain operation is shown in Figure 3. To each MK5025 there is added a pull-up resistor and a schottky diode in series with BUSRQ. This allows each MK5025 in the chain to request the bus regardless of whether or not another MK5025 has already requested or posseses the bus at the time. However, each device will not get the bus until the bus acknoledgement (HLDA) is passed on to the next device in the chain (through $\overline{\text{BUSAKO}}$). Thus, in a Round-Robin fashion, each MK5025 gets an equal opportunity to obtain the bus, whereas in Figure 2 the MK5025[1] has first priority, followed by MK5025[2], if both request the bus simultaneously.

The decision on which approach to use depends upon the task required of each MK5025 and the available bus bandwidth. If the Figure 2 scheme is used, it would be prudent to place the devices operating at the higher data rates in the higher priority positions in the daisy chain. If the Round-Robin approach is used it is important to realize that once bus mastership is granted by the host, it is possible that the bus may not be relinquished until all devices in the chain have had at least one DMA cycle of bus mastership.

BUS RELEASE OPERATION

In the daisy chain or sole requestor configuration the use of the Bus Release function may be useful to allow the designer to force the MK5025 to relinquish the bus prior to completeion of a DMA burst. The Bus Release function is programmed by setting bit BUSR in CSR4<06>. Setting this bit causes pin 15 to be defined as $\overline{\text{BUSREL}}$. The purpose of the $\overline{\text{BUSREL}}$ (pin 15) function is to allow an orderly abort to a MK5025 DMA burst after completion of the current bus transfer cycle.

It is important to note that the MK5025 has programmable burst size of 2 bytes, 16 bytes, or unlimited (typically 64-66 bytes), and that DMA bursting is only used for transfers of received and transmitted data. All buffer management functions are performed by the MK5025 using single word DMA cycles. This includes reading the Initialization Block, updating the Status Buffer, managing the descriptor rings, etc.

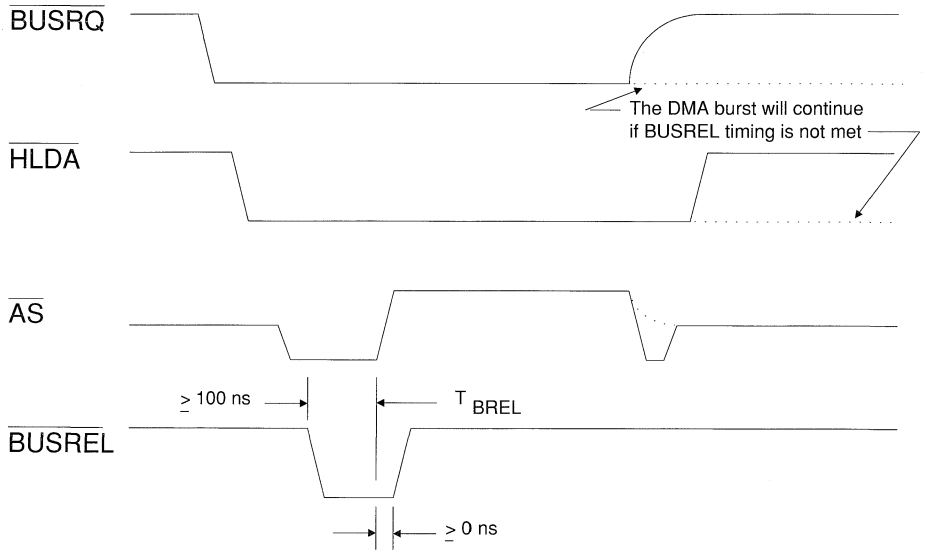
Although the MK5025 does support transmission and reception of odd-byte frames (MCNT, Message Byte Count may be odd), it is important to note that it does only word wide DMA transfers (no single byte transfers). It is because of this that the MK5025 requires that all data structures (including BCNT, Buffer Byte Count) and buffers be word aligned. Therefore the BYTE, BM0 and BM1 signals are never used by the MK5025 to indicate single upper or lower byte transfers. So there should be no concern about redefining these pins as $\overline{\text{BUSAKO}}$ and $\overline{\text{BUSREL}}$.

From the timing diagrams in Figure 4, it should be seen that $\overline{\text{BUSREL}}$ must be asserted at least 100 ns prior the rising edge of AS (or falling edge of ALE) in order for $\overline{\text{BUSREL}}$ to be recognized within that DMA cycle. $\overline{\text{BUSREL}}$ can be deasserted coincident with the rising edge of AS. If $\overline{\text{BUSREL}}$ is asserted too late to be recognized within in the current DMA cycle, then it should be held asserted (or be re-asserted at least 100 ns prior) to the rising edge of AS of the following DMA cycle, in order for that cycle to be the last in the burst.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, and the daisy chain information with associated timing diagrams are provided to further facilitate the design process.

Figure 4: Bus Release Timing



NOTE: The T_{BREL} setup time must be met in order for BUSREL to be recognized within that DMA cycle (causing the DMA burst to end on that cycle).

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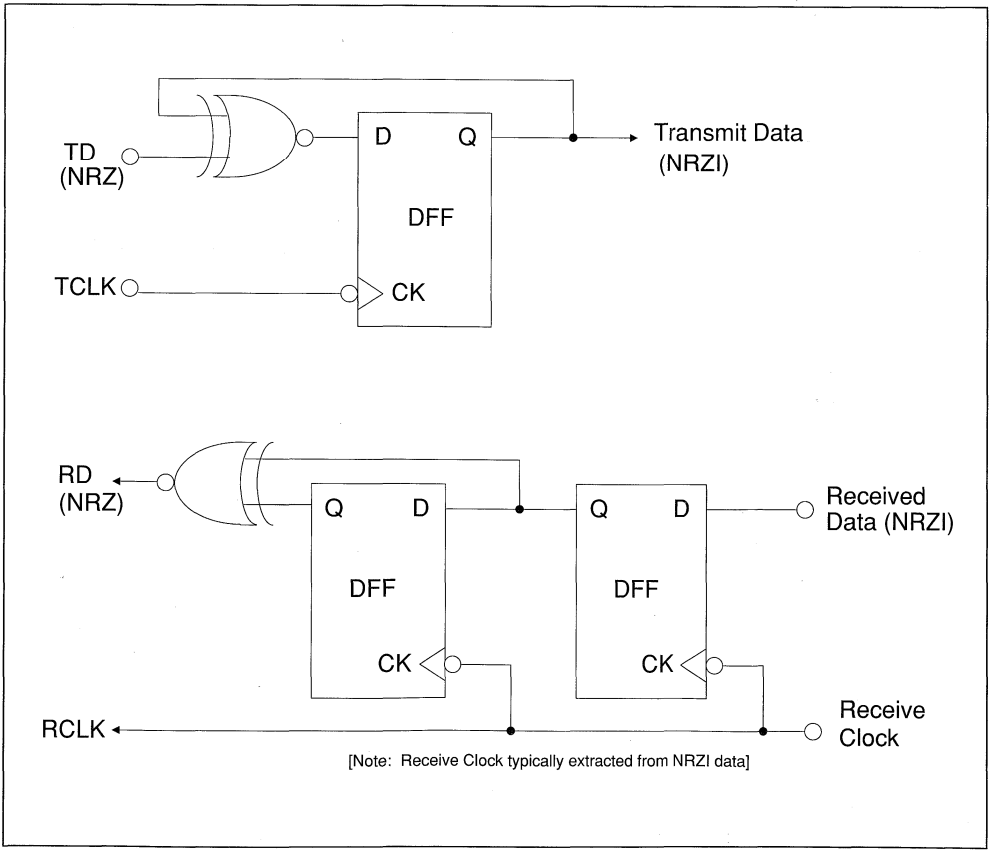
APPLICATION NOTE

MK5025
NRZ TO NRZI CONVERSION

The SGS-Thomson MK5025 link level controller is a versatile device providing complete link level data communication control conforming to the 1984 version of CCITT X.25. The MK5035 also supports X.32 and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities. The MK5025 also features a transparent mode of operation for implementation of customized protocols using HDLC framing.

The MK5025 serial interface consists of pins 25 - 27 and 29 - 31 (TCLK, DTR/RTS, RCLK, and TD, DSR/CTS, RD respectively). The transmit data (TD) is NRZ encoded and the receive data (RD) is NRZ decoded. To interface to other line code formats some conversion is necessary. The following figure shows one method for doing NRZ to NRZI conversion so that the MK5025 may be able to transmit and receive NRZI encoded data. It should be noted that the receive clock would typically be extracted from the received NRZI data, using a phase locked loop approach.

Figure 1: NRZ to NRZI Conversion



SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 TRANSPARENT MODE

INTRODUCTION

The SGS-Thomson X.25 Link Level Controller (MK5025) is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

One of the outstanding features of the MK5025 is its buffer managment which includes on-chip DMA. This feature allows users to handle multiple frames of receive and transmit data at a time. In order to utilize these buffer managment and DMA features with protocols not directly supported by the MK5025, a transparent mode is available for customized protocols using HDLC framing. This transparent mode provides an HDLC transport mechanism without link layer support. Extended addressing and control are optionally supported within transparent mode. Address filtering is also optional in this mode.

PURPOSE

The purpose of this application brief is to provide a detailed description of the MK5025 transparent mode and its options. Please refer to the MK5025 Technical Manual for more detailed information concerning the overall operation of the MK5025.

TRANSPARENT MODE ENTRY AND EXIT

To enter the transparent mode of operation, a user primitive *Trans* (UPRIM 3) is written to Control Status Register 1 (CSR1) after the completion of the first 4 steps of the *Initialization* procedure described in page 4-24 of the MK5025 Technical Manual. (The *Trans* Primitive is substituted for the *Start* primitive.) The transmitter then begins to output flags, and data frames are transmitted and received via the descriptor rings, but no protocol processing is done. Address and Control Fields are not prepended to the frames, and FCS (Frame Check Sequence) processing may be enabled or disabled by the DRFCS and DTFCS bits in the mode register, as described on page 4-12 of the Technical Manual. Transparent mode may be exited only with a *Stop* primitive (UPRIM 0) or by bus reset.

CONTROL AND STATUS REGISTER OPERATION

In transparent mode all the control and status register mechanisms are still functional, but there are several bits that pertain only to the protocols directly supported by the MK5025 and are not valid in transparent mode. The following is a list of the validity of the bits in each CSR and the mode register when in transparent mode.

CSR0 - All bits in this register are valid in Transparent mode. It should be noted that interrupts can only be set (by setting bit 09, INEA = 1) once the device is in start or transparent mode.

CSR1 - All bits except PPARM are valid, although only for a few non-protocol related conditions. Since in transparent mode only a Stop User Primitive would have been valid, User Primitives 8 and 9 have been redefined. When in transparent mode, issuing User Primitive 8 (UPRIM 8) will start T1 timer and User Primitive 9 (UPRIM 9) will stop it. In this case Provider Primitive 8 (PPRIM 8) has been redefined to indicate expiry of T1 timer.

CSR2 - Aside from the IADR bits, only the PROM and XIDE bits have valid meaning in transparent mode. The XIDE bit can be set to 1 to enable global address recognition, and the PROM bit is used to disable address filtering in transparent mode.

CSR3 - As in CSR2, the IADR bits contain the address of the first word in the Initialization Block. Bits 00 - 07 in CSR2 contain the high order 8 bits, and bits 00 - 15 of CSR3 contain the low order 16 bits of the address of the first word of the Initialization Block.

CSR4 - All bits in this register are valid in transparent mode, including the FIFO watermarks and bursting operations.

CSR5 - All bits are valid in transparent mode.

MODE REGISTER OPERATION

All bits in the Mode Register are valid including MFS (Minimum Frame Spacing) and LBACK (Loopback). However, bits 09 (EXTAF) and 10 (EXTCF) are useful mainly in transparent mode, for forcing extended address and control field filtering. The DACE bit also offers further flexibility in transparent mode by allowing address and con-

trol fields to be treated as normal data when DACE = 1, as shown in Table 2.

It should be noted that although DTFCS and DRFCS (bits 04 & 05) may be used to disable FCS generation and checking, the value in the FCS field of the received frame will not be stored in memory, even in transparent mode.

DESCRIPTOR RING OPERATION

The buffer management and descriptor ring operation is the same in transparent as non-transparent mode. It should be noted however that for the Transmit Message Descriptor, **TUI (bit 11 of TMD0) should be set to 1 for anything transmitted in transparent mode.** This is done because data transmitted in transparent mode is considered much the same as a UI frame rather than a normal I frame.

In transparent mode as in non-transparent mode, the Transmit Window size (TWD) in the Transmit Descriptor Ring Pointer must be set to a value greater than 0 for any transmission to occur. In fact, **if TWD=0 the MK5025 will not poll the Transmit Descriptor Ring.**

ADDRESS FIELD FILTERING AND CONTROL FIELD OPERATION

The frame structure for HDLC is as follows:

F	A	C	I	FCS	F

where:

F = Flag
A = Address field (A-field)
C = Control field (C-field)
FCS = Frame Check Sequence

According to HDLC rules, the A-field may be one or more octets in length. If the LSB of the first octet is 0, then the second octet is also part of the A-field. If the LSB of the second is 0, then the third octet is part of the A-field, and so on until an octet has an LSB = 1. The MK5025 allows the A-field to be one or two octets, depending upon the EXTA bit (Mode Register bit 10).

The C-field is one octet for modulo 8 for all frames. For modulo 128, the C-field is said to be extended, and is two octets for S (Supervisory) and I (Information) frames and one octet for U (Unnumbered) frames.

In the MK5025, address filtering and control field handling applies only to octet aligned frames received with good FCS. Any frame not meeting both of these conditions is discarded and the "Bad Frames Received" error counter (located at IADR + 44 of the Initialization Block) is incremented.

In the transparent mode, address filtering is supported if the PROM bit (CSR2, bit 10) is 0. In this case, frames are accepted if the received A-field matches either the Local Station Address or the Remote Station Address as specified in the Initialization Block. Bit RADR in the Receive Message Descriptor (RMD0 <09>)indicates which of the two programmable adresses the frame matched. This is a one octet compare if the extended address bit, EXTA is 0 (Mode register bit 06), or follows the HDLC rules for extended addressing if EXTA is 1. Frames not matching either address are ignored.

Extended control is also valid in transparent mode using the EXTC bit (Mode Register bit 07), as shown in Table 1 and Table 2. If EXTC is 0 then the C-field is one octet for all frames. If however EXTC is set to 1, the MK5025 will look to see if either of the two least significant bits of the C-field is 0. If so, the frame is said to have an extended control field which is two octets. In addition, bits EXTAF and EXTCF (Mode Register bit 09 & 10) are useful in transparent mode to force extended address and control. If EXTAF is set along with EXTA, the receiver will assume the ad-

Table 1: MK5025 Address Filtering Options

EXTA	EXTAF	XIDE	PROM	DACE	ADDRESS FILTERING
0	0	0	0	0	Single octet filtering L &R (Local & Remote adresses)
x	x	x	1	x	No address filtering, all frames accepted
0	0	1	0	0	Single octet filtering L & R and global
0	x	x	x	1	Not allowed
1	0	0	0	0	Double octet filtering L & R per HDLC rules
1	0	0	0	1	Double octet filtering L & R per HDLC rules
1	1	0	0	0	Double octet filtering L & R regardless of A-field LSB
0	1	x	x	0	Not allowed

Notes:
1) EXTA = Extended address, Mode register bit 06. EXTAF = Extended address Force, Mode register bit 09.

2) XIDE = XID enabled, CSR2 bit 08. PROM = Promiscuous mode, CSR2 bit 10.

3) DACE = Disable address and control field extraction for load to memory, Mode register bit 08.

4) L&R = Local and Remote addresses. X = Do not care.

Table 2: Address and Control Field Handling By the MK5025 Receiver

DACE	PROM	EXTA	EXTAF	EXTC	EXTCF	Address Field Handling	Control Field Handling
0	0	0	0	0	0	A filtered	CC ⇒ MEM1
0	0	0	0	1	0	A filtered	CC or EC ⇒ MEM1
0	0	1	0	0	0	A or EA filtered	CC ⇒ MEM1
0	0	1	1	0	0	EA filtered	CC ⇒ MEM1
0	0	1	0	1	0	A or EA filtered	CC or EC ⇒ MEM1
0	0	1	1	1	1	EA filtered	EC ⇒ MEM1
0	1	0	0	0	0	Not filtered, AA ⇒ MEM1	CC ⇒ MEM2
0	1	0	0	1	0	Not filtered, AA ⇒ MEM1	CC or EC ⇒ MEM2
0	1	1	0	0	0	Not filtered, AA or EA ⇒ MEM1	CC ⇒ MEM2
0	1	1	1	0	0	Not filtered, EA ⇒ MEM1	CC ⇒ MEM2
0	1	1	0	1	1	Not filtered, AA or EA ⇒ MEM1	EC ⇒ MEM2
1	0	X	X	X	X	First 2 octest always filtered	EC ⇒ MEM1
1	1	X	X	X	X	Total transparent mode	All data after opening flag & before FCS ⇒ memory

Notes:

1. MEM1 is the first location and MEM2 is the second location where received data is loaded. MEM1 and MEM2 are each 16 bits wide.

2. C is the received, single octet, control field. CC ⇒MEMx means the single octet control field C is loaded into both bytes of a 16 bit memory location. Similarly, A is a single octet address field, and AA ⇒ MEMx means the single octet address field A is loaded into both bytes of a 16 bit memory location.

3. EC is an extended control field (2 octets) for received S and I frames. For received U frames, the control field is not extended (1 octet). This determines whether CC or EC ⇒ MEMx. However, when EXTCF is set to 1, the control field is always extended (EC = 2 octets).

4. EA is an extended address field (2 octets). "A or EA filtered" means that one octet of the A-field is filtered if the LSB = 1, or two octets are filtered if the LSB = 0. Similarly "AA or EA ⇒ MEM1" means that AA is loaded into memory if the LSB = 0; else, EA is loaded. This conforms to HDLC rules for extended address. However, if EXTAF is set to 1, two octets are filtered regardless of the LSB, and EA will be loaded into memory.

5. EXTCF = Extended control force, Mode register bit 10.

6. DACE, PROM, EXTA, EXTAF, and EXTC are as defined in the notes for Table 1. X = Do not care.

dress field to be two bytes long regardless of the first bit of the address field. If EXTCF is set along with EXTC, the receiver will assume the contol field to be two bytes long regardless of the first two bits of that field.

For global adresses, the XIDE bit is valid in transparent mode, depending upon the settings of the other bits in the Mode Register, as shown in Table 1. If XID is enabled by setting bit XIDE (CSR2 bit 08) to 1, then all frames with address "11111111" are accepted. Even frames which are not XID are accepted. In this case, a global address is considered as a command frame. Additionally, frames may transmitted from the XID/TEST buffer, but neither an Address nor Control field will be pre-pended to the frame.

Address and control field extraction can be disabled in transparent mode, through use of the if PROM bit (CSR2, bit 10) and DACE bit (Mode Register bit 08), as shown in Table 2. If the PROM bit is 1, all frames are accepted. When both the PROM bit and the DACE bit are set to 1, the device is considered to be in total transparent mode. In this mode no protocol processing is done and all data after the opening flag and before the FCS is loaded into memory.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, while still allowing the flexibility of implementing alternate or customized HDLC based protocols using the MK5025's transparent mode.

SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

MK5025 SYNCHRONOUS TIMING

INTRODUCTION

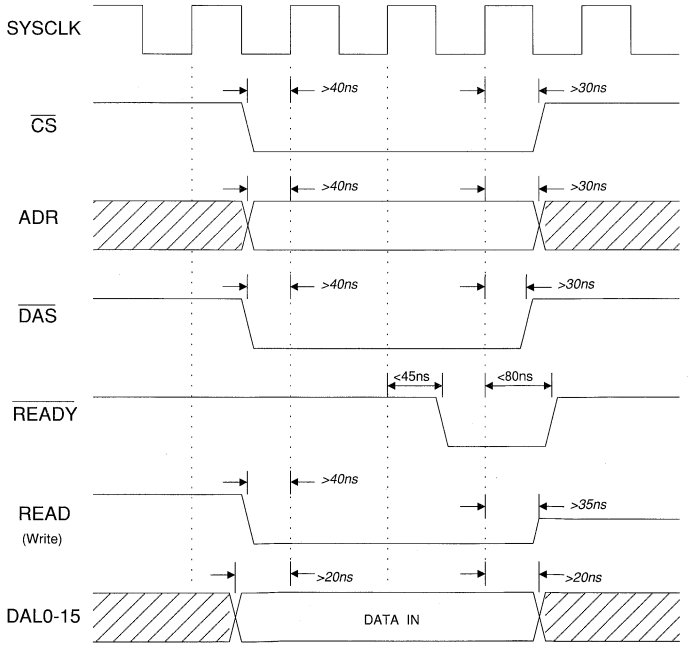
The SGS-Thomson MK5025 X.25 Link Level Controller is a VLSI device which provides a complete link level data communication control conforming to the 1984 CCITT version of X.25. The MK5025 also supports X.32 (XID) and X.75 as well as single channel LAPD for ISDN with its UI frames and extended addressing capabilities.

PURPOSE

Although the MK5025 Data Sheet and Technical Manual provide detailed asynchronous timing diagrams that specifiy the relationships of the host interface signals to one another, the designer may often find it helpful to know how these timing values relate to the system clock. The purpose of this application brief is to provide a description of the MK5025 host interface as related to SYSCLK (MK5025 pin 28).

Because of the asynchronous nature of the use of this device, the MK5025 production testing is performed to ensure compliance with the asynchronous timing specifications stated in the Data Sheet and Technical Manual. It should be noted that although the synchronous timing diagrams in this document are provided to facilitate the design process, **the timing requirements in the Data Sheet must still be met to ensure proper operation.**

Figure 1: MK5025 Bus Slave Write Cycle



NOTES:

1. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are the typical maximum delay from the specified edge to a valid output.

SYNCHRONOUS TIMING

The synchronous timing data contained within this document was derived from a sample of MK5025 devices and guard-banded to allow for process variations. Although these values are not guaranteed or tested in the manufacturing process, the typical MK5025 device performance should meet or exceed these timing values.

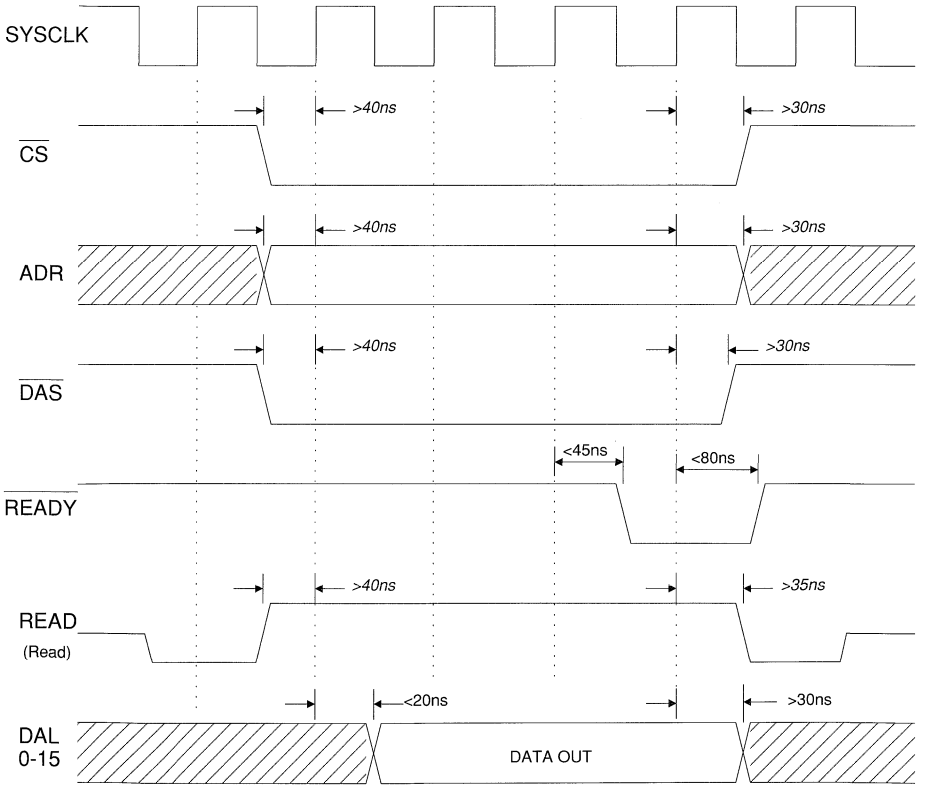
Figures 1 and 2 provide the typical timing relationships, with respect to SYSCLK, for the MK5025 operating as a bus slave. Figures 3 and 4 provide the typical timing relationships, with respect to SYSCLK, for the MK5025 operating as a bus master.

The input setup and hold times given in this document are typical minimum values required to or from the SYSCLK edge indicated in order to be recognized within that SYSCLK cycle. The output delay times are the typical maximum delay from the indicated edge to a valid output state.

CONCLUSION

The MK5025 offers great flexibility to the data communications system designer. The on-chip protocol processing may be used to save the designer much time in implementing standard protocols such as X.25, LAPB, ISDN LAPD, X.32, and X.75, and these synchronous timing diagrams are provided to further facilitate the design process.

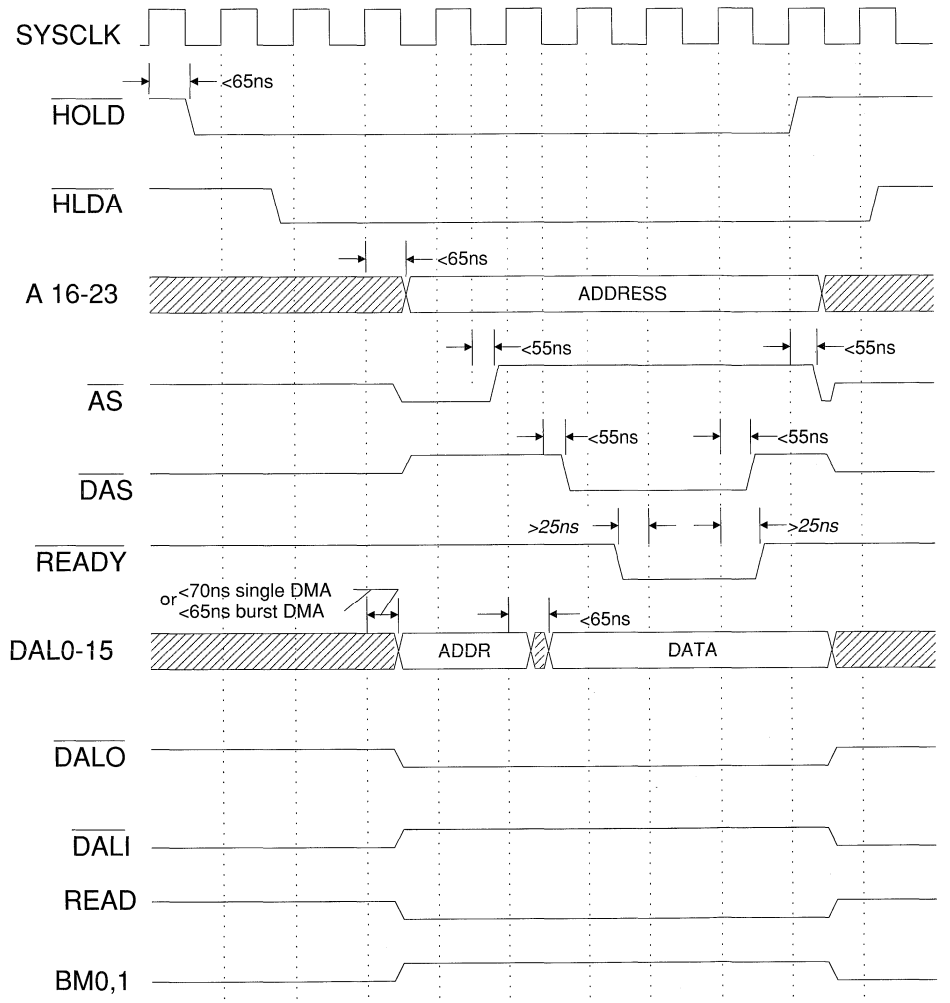
Figure 2: MK5025 Bus Slave Read Cycle



NOTES:

1. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
2. Output delay times are the typical maximum delay from the specified edge to a valid output.

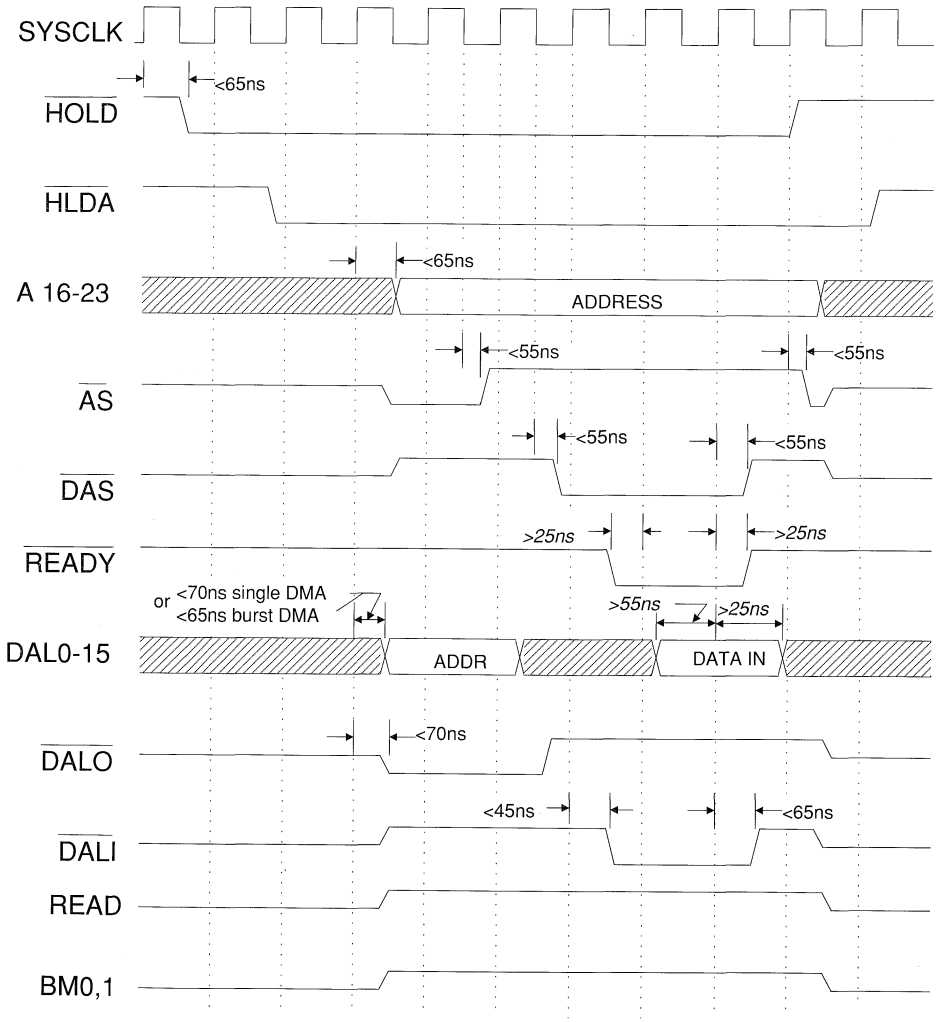
Figure 3: MK5025 Bus Master Write Cycle



NOTES:

1. The typical MK5025 device performance should meet or exceed the typical timing values given above. Asynchronous timing requirements given in the Technical Manual still apply.
2. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
3. Output delay times are the typical maximum delay from the specified edge to a valid output.

Figure 4: MK5025 Bus Master Read Cycle



NOTES:

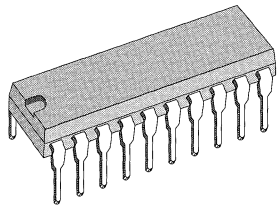
1. The typical MK5025 device performance should meet or exceed the typical timing values given above. Asynchronous timing requirements given in the Technical Manual still apply.
2. Input setup and hold times are in italics. These times are typical minimum values required to or from the particular edge specified in order to be recognized in that cycle.
3. Output delay times are the typical maximum delay from the specifed edge to a valid output.

PACKAGES

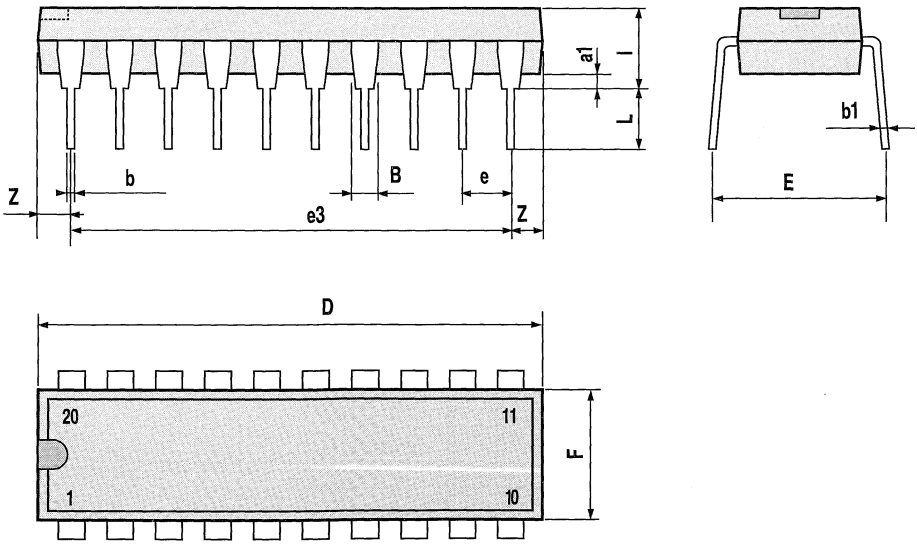
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP20 (0.25)

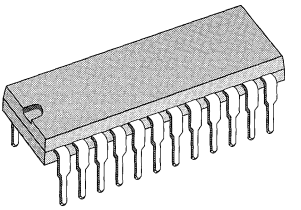


P001J

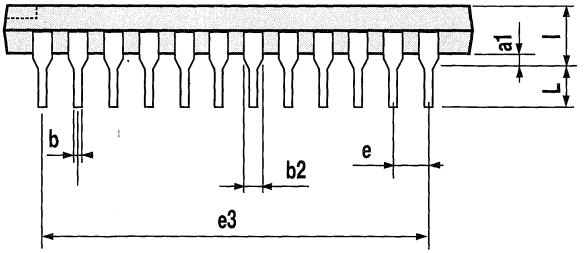
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	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
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b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

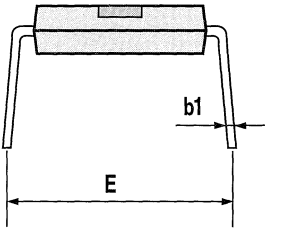
SGS-THOMSON MICROELECTRONICS

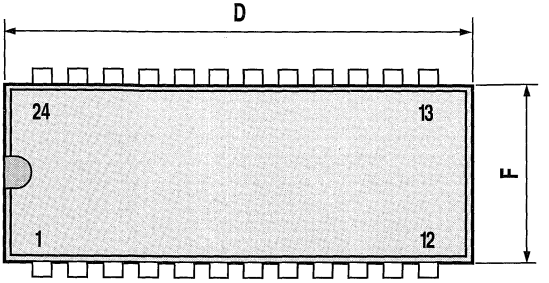
OUTLINE AND MECHANICAL DATA



DIP24 (0.25)





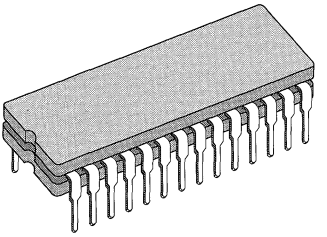


P043A

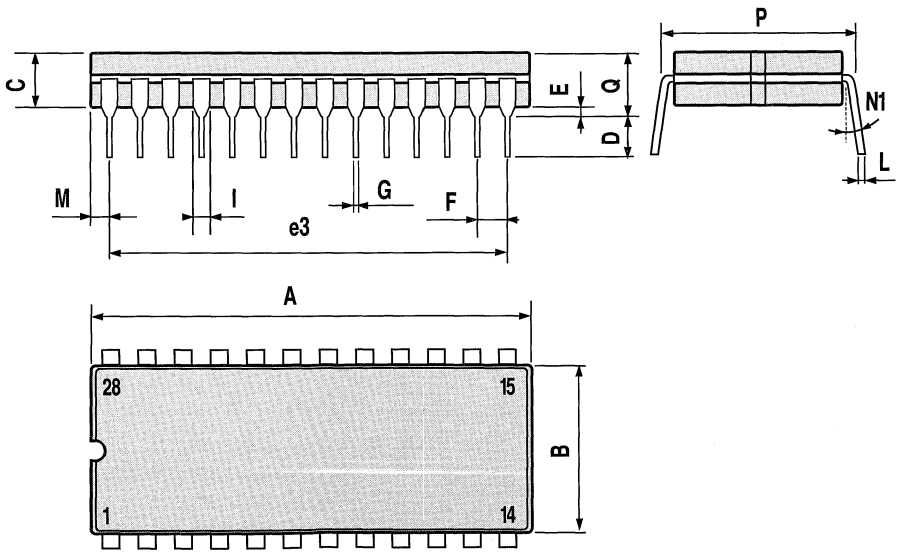
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			38.1			1.500
B	13.05		13.36	0.514		0.526
C	3.9		5.08	0.154		0.200
D	3			0.118		
E	0.5		1.78	0.020		0.070
e3		33.02			1.300	
F	2.29		2.79	0.090		0.110
G	0.4		0.55	0.016		0.022
I	1.17		1.42	0.046		0.056
L	0.22		0.31	0.009		0.012
M	1.52		2.49	0.060		0.098
N1	4°(min.), 15°(max.)					
P	15.4		15.8	0.606		0.622
Q			5.71			0.225

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic DIP28

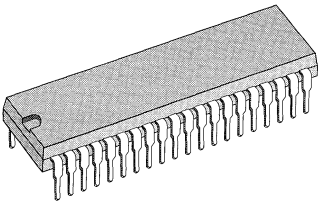


P058D

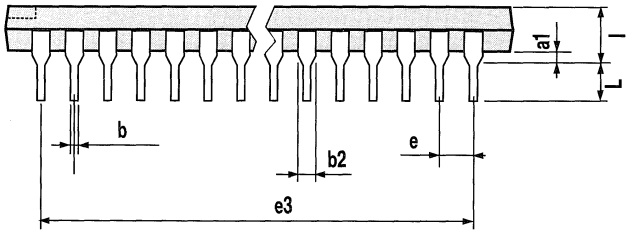
DIM.	mm			inch		
	MIN	TYP	MAX	MIN	TYP	MAX
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

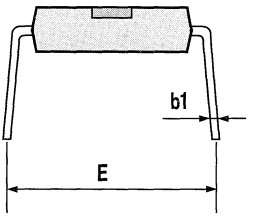
SGS-THOMSON MICROELECTRONICS

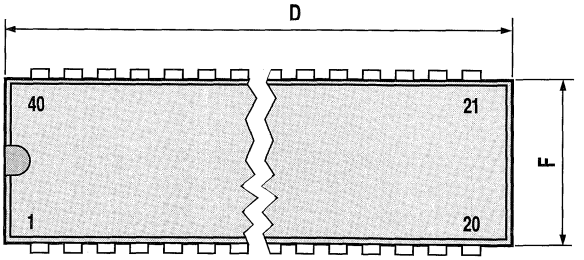
OUTLINE AND MECHANICAL DATA



DIP40





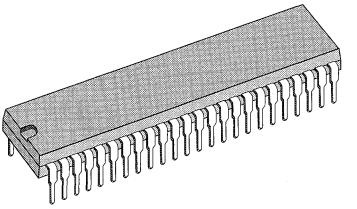


P043E

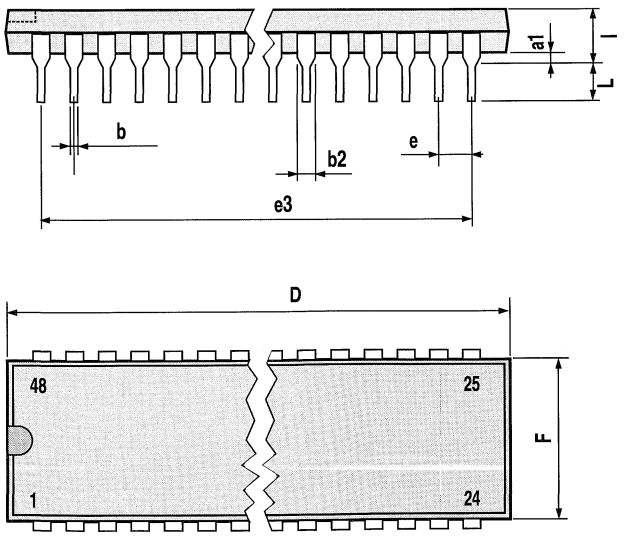
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			62.74			2.470
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		58.42			2.300	
F			14.1			0.555
I		4.445			0.175	
L		3.3			0.130	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



DIP48

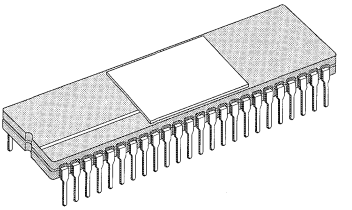


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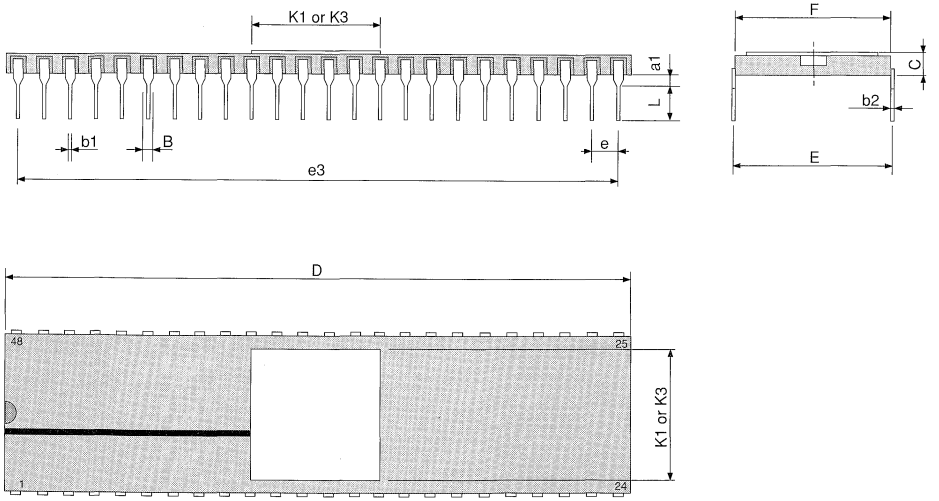
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		1.27			0.050	
B		1.27			0.050	
b1		0.45			0.018	
b2		0.25			0.010	
C		2.46			0.097	
D			61.59			2.425
E		15.24			0.600	
e		2.54			0.100	
e3		58.42			2.300	
F			15.34			0.604
L		3.3			0.130	
K1		13.46			0.530	
K3		11.43			0.450	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



Ceramic Side Brazed DIP48

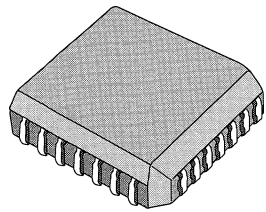


P065A

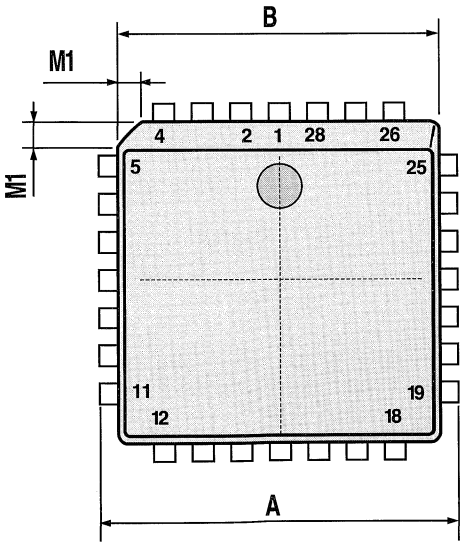
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	12.32		12.57	0.485		0.495
B	11.43		11.58	0.450		0.456
D	4.2		4.57	0.165		0.180
D1	2.29		3.04	0.090		0.120
D2	0.51			0.020		
E	9.91		10.92	0.390		0.430
e		1.27			0.050	
e3		7.62			0.300	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.24			0.049	
M1		1.143			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



PLCC28

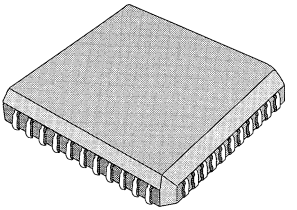


P027E

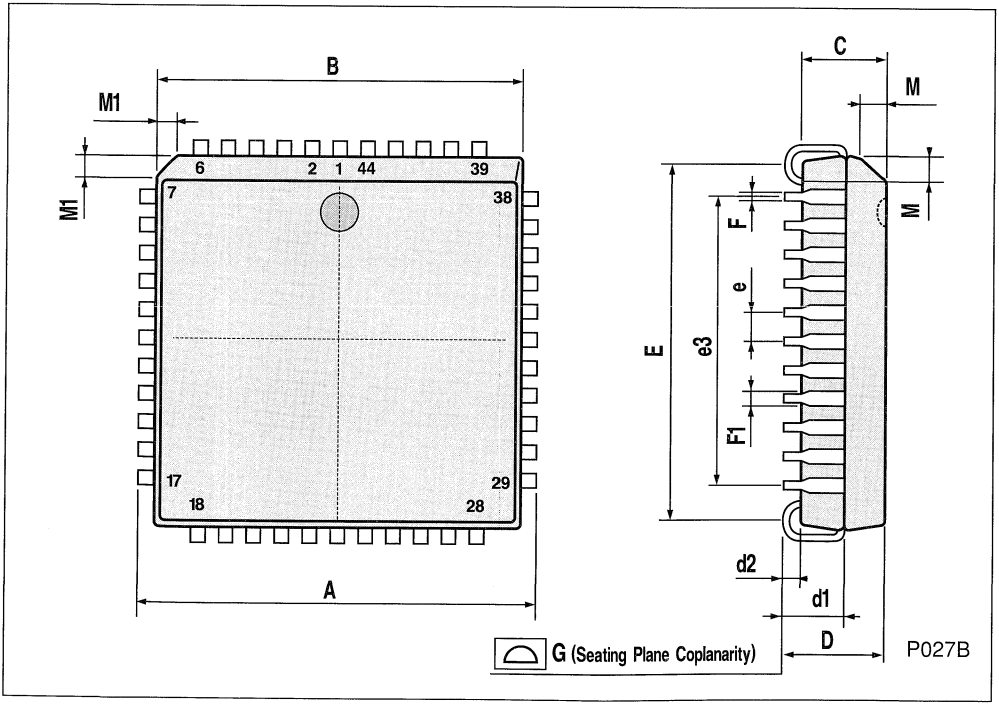
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



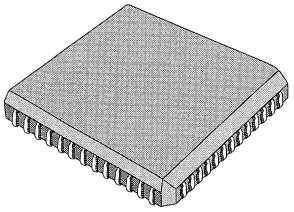
PLCC44



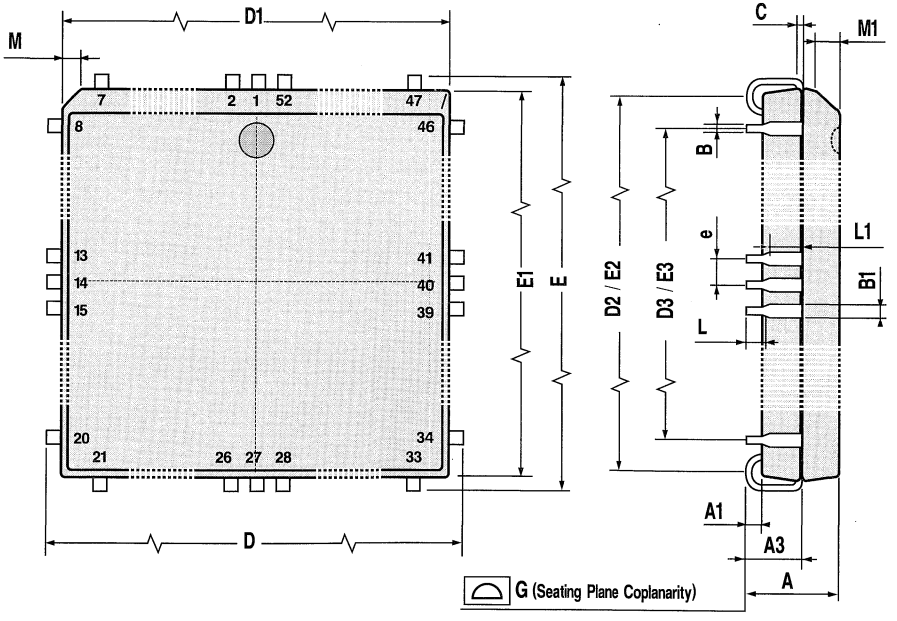
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		4.20	5.08		0.165	0.20
A1		0.51			0.020	
A3		2.29	3.30		0.090	0.13
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
C	0.25			0.01		
D		19.94	20.19		0.785	0.795
D1		19.05	19.20		0.750	0.756
D2		17.53	18.54		0.690	0.730
D3	15.24			0.60		
E		19.94	20.19		0.785	0.795
E1		19.05	19.20		0.750	0.756
E2		17.53	18.54		0.690	0.730
E3	15.24			0.60		
e	1.27			0.05		
L		0.64			0.025	
L1		1.53			0.060	
M		1.07	1.22		0.042	0.048
M1		1.07	1.42		0.042	0.056

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



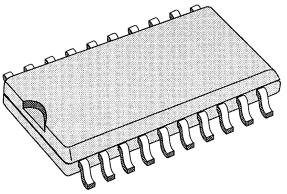
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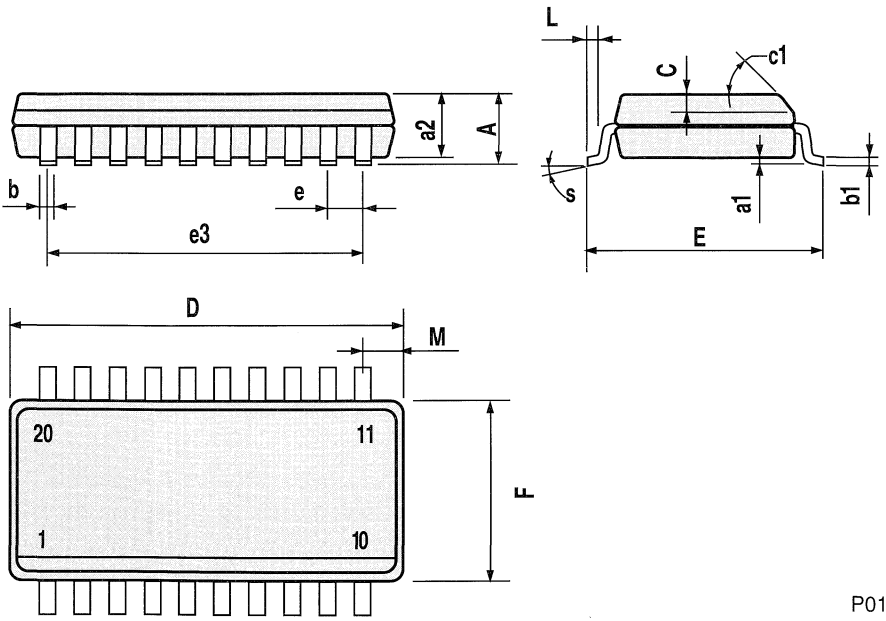
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.013
C		0.5			0.020	
c1	45° (typ.)					
D	12.6		13.0	0.496		0.510
E	10		10.65	0.394		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.4		7.6	0.291		0.300
L	0.5		1.27	0.020		0.050
M			0.75			0.030
S	8° (max.)					

SGS-THOMSON MICROELECTRONICS

OUTLINE AND MECHANICAL DATA



SO20



P013L

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